SPECIAL CIRCUITS

FOR

AN/FSQ-7 COMBAT DIRECTION CENTRAL

AND

AN/FSQ-8 COMBAT CONTROL CENTRAL

1 May 1959

MILITARY PRODUCTS DIVISION
INTERNATIONAL BUSINESS MACHINES CORPORATION
KINGSTON, NEW YORK

LIST OF REVISED PAGES

INSERT LATEST REVISED PAGES. DESTROY SUPERSEDED PAGES.

NOTE: The portion of the text affected by the current revision is indicated by a vertical rule in the left margin of a left-hand page and in the right margin of a right-hand page.

*The asterisk indicates pages revised, added or deleted by the current revision.

CONTENTS

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF TABLES

LIST OF TABLES (cont'd)

LIST OF TABLES (cont'd)

LIST OF TABLES (cont'd)

CONTENTS (cont'd)

CHAPTER 1
INTRODUCTION

1.1 SCOPE OF MANUAL

This manual presents the theory of operation of the special circuits utilized in the AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central. Electronically, these equipments are a complex combination of many circuits. Special circuits, by definition, are those circuits which serve special purposes in the equipment as opposed to basic circuits which are capable of many and varied applications. A special circuit may be used only once in the equipment or it may have a limited application in several elements. The theory of operation of each special circuit is covered without reference to any specialized application or to any other circuit.

1.2 ORGANIZATION OF MANUAL

1.2.1 General

This manual consists of four chapters. Chapter 1 introduces the manual. Chapter 2 discusses the functional requirements of circuit elements having a common function; the extensive repetition of these circuit elements throughout the AN/FSQ-7 and -8 systems permits a separate treatment of their function, thereby simplifying the special circuit theory discussion. Chapter 3 presents the theory of operation of the special circuits. Chapter 4 presents the theory of operation of circuits performing a special purpose but which are not represented by logic block symbols. These circuits are referred to as "other" circuits in this manual.

1.2.2 Chapter 1, Introduction

Chapter 1 explains the organization of the manual and defines the special circuit. In this chapter, table 1–1 lists all the special circuits in the AN/FSQ-7 and -8 equipments in alphabetical order and includes the logic abbreviations for each circuit and the system in which each is used. Table 1–2 lists all "other" circuits in the same manner.

1.2.3 Chapter 2, Common Circuit Characteristics

Mechanical and electrical information necessary to the understanding of special circuits is presented in this chapter. Common signals are identified and discussed. The physical characteristics of the special circuits are investigated, and the electrical limitations that result are noted. The compensation of these electrical limitations is resolved and parasitic suppression and resistance-capacitance (RC) decoupling are analyzed.

Common circuits employed in the clamping and coupling of levels are discussed and supported with mathematical calculations where such support is applicable. Finally, speedup circuits are analyzed with respect to their application in the special circuits.

1.2.4 Chapter 3, Special Circuits, Theory of Operation

Chapter 3 describes the theory of operation of the special circuits employed throughout the AN/FSQ-7 and -8 equipments. These circuits are arranged in alphabetical order and are discussed without reference to a specialized application or to any other circuit.

The schematic diagrams are presented in simplified form with parallel combinations of resistors, diodes, or tubes usually merged into a single resistor, diode, or tube. Parasitic suppressors and decoupling networks have been omitted from the schematics for reasons of clarity. It can be assumed that any components that appear in a schematic of an actual circuit but not in the simplified diagram are not essential to an understanding of the operation of the circuit. Where feasible, waveforms have been included on the schematic diagram as an aid in understanding the operation of the circuit. In some cases, waveforms are keyed by number to specific points on the schematic; in other cases, only input and output waveforms are shown.

Each circuit writeup follows the same format and, in general, comprises two paragraphs. The first paragraph (3.1.1, Definition and Description) identifies the circuit logic block symbol, describes circuit function, and enumerates the significant differences between the models in terms of capabilities, limitations, or operational characteristics. The next paragraph (3.1.2, Principles of Operation) discusses the operation of the circuit. The treatment of each circuit proceeds from basic considerations to specific functions of detail parts. Where circuit complexity requires it, each circuit is reduced to its simplest operating elements, and the fundamental principles of operation are explained in terms of this circuit. A detailed discussion follows in terms of a specific model of the circuit which consists of the simplified circuit and the added refinements used to adapt the latter to its operational environment.

1.2.5 Chapter 4, Other Circuits, Theory of Operation

Chapter 4 describes the theory of operation of the circuits which perform special functions and do not have logic block symbols assigned. These circuits include an activate circuit, high-voltage power supplies, high-voltage units, a low-voltage power supply, and a —150V memory alarm. The format in which these circuits are presented is identical with the special circuit theory of operation in Chapter 3.

TABLE 1–1. SPECIAL CIRCUITS IN AN/FSQ-7 AND -8 EQUIPMENTS

CIRCUIT	LOGIC SYMBOL	SYSTEM APPLICATION				
		CENTRAL COMPUTER	DISPLAY	INPUT	OUTPUT	DRUM
All-Channel Driver	ACD				✓	
All-Channel Driver	AC			✓		
Analog Line Driver	ALD		✓			
Area Discriminator	AD		✓			
Area Discriminator Amplifier	ADA		✓			
Automatic Gain Control	AGC			✓		
Binary Decoder	BD		✓	✓		
Buffer Amplifier	BU		✓			
Capacitor-Diode Gate	CDG		✓			
Cathode Follower Clamp	CFC	✓				
Complement Core Counter	CCC			✓		
Constant Voltage Amplifier	CVA				✓	
Contrast Gate Isolation Amplifier	CGA		✓			
Convergence Current Regulator	CCR		✓			
Core Current Driver	CCD				✓	
Core Delay Register	CDR			✓		
Core Memory Driver	CMD	✓				
Core Prime	CP			✓	✓	
Core Shift	CS			✓	✓	
Core Shift Driver	CSD			✓	✓	
Crystal Oscillator	OSC	✓	✓			
Current Regulator	CR	✓				
Data Conversion Receiver	DCR			✓	✓	
Decoder Simulator	DCS		✓			
Deflection Amplifier	DA		✓	✓		
Deflection Driver	DEF		✓			

TABLE 1-1. SPECIAL CIRCUITS IN AN/FSQ-7 AND -8 EQUIPMENTS (cont'd)

CIRCUIT	LOGIC SYMBOL	SYSTEM APPLICATION				
		CENTRAL COMPUTER	DISPLAY	INPUT	OUTPUT	DRUM
Digital Line Driver	DLD			✓		
Digit Plane Driver	DPD	✓				
Diode-Capacitor Gate	DCG		✓	✓		
Distribution Power Amplifier	DPA			✓		
Drum Field Driver	DFD					✓
Drum Read Amplifier	DRA					✓
Drum Read Driver	DRD					✓
Drum Writer	DW					✓
Drum Write Driver	DWD					✓
Flux Amplifier	FA				✓	
Frequency Doubler	FD			✓		
Input Amplifier	IA	✓				
Inverter	I		✓			
Isolation Circuit	IC			✓		
Level Amplifier	LEA			✓		
Level Originator	LO	✓				
Light Gun	LG		✓			
Light Gun Amplifier	LGA		✓			
Logic Driver	LD			✓	✓	
Logical Gate	LGT			✓	✓	
Mapper Intensification Circuit	MIC			✓		
Mapper Sweep Generator	MSG			✓		
Matching Amplifier	MA			✓	✓	
Matrix Output Amplifier	MOA	✓				
Memory Gate Generator	MGG	✓				
Mesh Level Control and Erasure Unit	MLC		✓			
Miller Integrator	MI			✓		
Missing Pulse Detector	MPD	✓				
Multiplier	MUL			✓		
Negative OR Circuit	—OR	✓				

TABLE 1–1. SPECIAL CIRCUITS IN AN/FSQ-7 AND -8 EQUIPMENTS (cont'd)

CIRCUIT	LOGIC SYMBOL	SYSTEM APPLICATION				
		CENTRAL COMPUTER	DISPLAY	INPUT	OUTPUT	DRUM
Optical Frequency Generator	OFG					✓
Phase Splitter	PS			✓		
Phototube Amplifier	FOA			✓		
Photomultiplier	FN			✓		
Power Amplifier Driver	PAD			✓		
Power Cathanode	PCA	✓				
Power Cathode Follower	PCF	✓	✓	✓	✓	✓
Power Inverter	PI			✓		
Power Output Amplifier	POA			✓		
Pulse Coupler	PC		✓			
Pulse Shaper	SH	✓	✓			
Read Head Amplifier	RHA			✓		
Reset Circuit	RS			✓		
Reset-Inhibit Driver	RID				✓	
Schmitt Trigger	ST	✓			✓	
Sense Amplifier	SA	✓				
Sense Amplifier Blocking Oscillator	SAB			✓		
Set Driver	STD				✓	
Sine-Cosine Approximator	SCA			✓		
Switch Driver	SWD	✓				
Tape Flip-Flop	TFF	✓				
Tape Inverter	TI	✓				
Thyratron Core Driver	TCD			✓	✓	
Thyratron Relay Driver	RYD			✓		
Timing Pulse Generator	TPG					✓
Tuning Fork Oscillator	TFO	✓		✓	✓	✓
Variable Gate Amplifier	VGA		✓			
Vector Generator	VG		✓			
Vector Intensity Generator	VIG		✓			
Voltage Regulator	VR			✓		

TABLE 1–1. SPECIAL CIRCUITS IN AN/FSQ-7 AND -8 EQUIPMENTS (cont'd)

CIRCUIT	LOGIC SYMBOL	SYSTEM APPLICATION				
		CENTRAL COMPUTER	DISPLAY	INPUT	OUTPUT	DRUM
Warning Light Relay Driver	WLD	✓				
Write Head Driver	WHD			✓		

TABLE 1–2. "OTHER" CIRCUITS IN AN/FSQ-7 AND -8 EQUIPMENTS

CIRCUIT	SYSTEM APPLICATION				
	CENTRAL COMPUTER	DISPLAY	INPUT	OUTPUT	DRUM
Activate Circuit			✓		
High-Voltage Power Supplies		✓			
High-Voltage Units		✓			
Low-Voltage Power Supply		✓			
—150V Memory Alarm	✓				

CHAPTER 2

FUNCTIONAL REQUIREMENTS AND COMMON CIRCUIT CHARACTERISTICS

2.1 FUNCTIONAL REQUIREMENTS

2.1.1 Introduction

Many of the special circuits in the AN/FSQ-7 and -8 equipments operate on analog inputs and/or outputs. The various circuits involved with these analog voltages are constructed to accomplish the required degree of linearity and stability.

2.1.2 Definitions of Linearity and Stability

Linearity, as applied to an amplifier, is the constant ratio of the amplifier to its input (fig. 2–1).

Stability, as applied to an amplifier, is the characteristic which enables the amplifier output to be independent of all variations (reference voltages, supply voltages, temperature, elapsed time, etc.) except the input variations.

2.1.3 Techniques Employed to Achieve Linearity

The linearity of an amplifier may be improved in several ways. The selection of the correct operating point of each vacuum tube, the introduction of degeneration by means of unbypassed cathode resistors, and the high-frequency compensation of voltage dividers are three of the design techniques employed.

Where linearity, within very close limits, is a prerequisite, the employment of inverse feedback is utilized. This technique involves returning a percentage of the output of an amplifier to its input. The phase of the output feedback opposes the phase of the input.

In figure 2–2, let A (the gain of the amplifier) equal 1,000 and B (the percentage of the output which

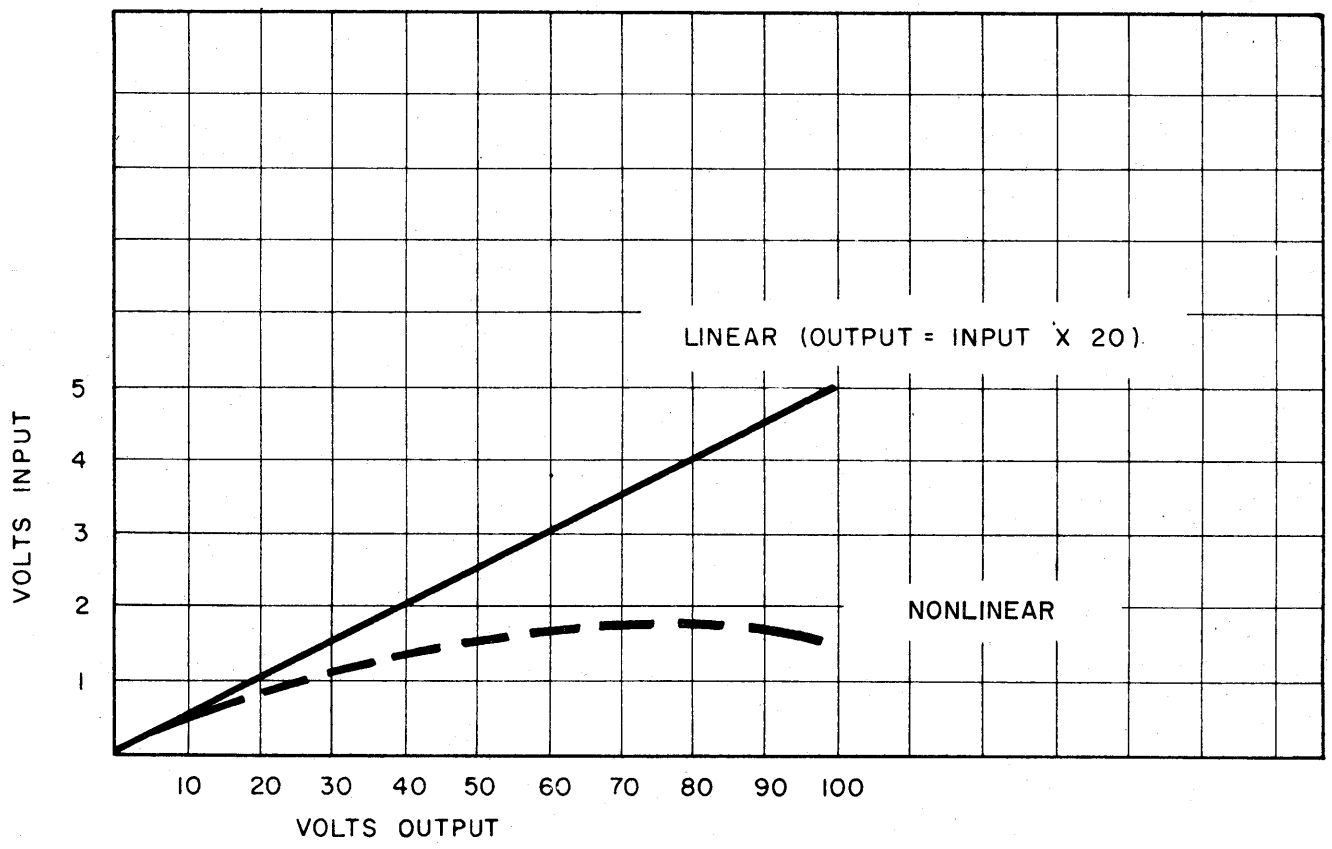


Figure 2–1. Amplifier IO Relationship

is inversely fed to the input) equal 25 percent. Then the gain of the system (amplifier with feedback) is relatively independent of the amplifier's characteristics and dependent only on the reciprocal of feedback ratio B. Note that, although the amplifier gain is 1,000, the output is equal to four times the input. The gain of the amplifier is reduced 250 times by the application of inverse feedback, and the gain of the system is $\frac{1}{B} = \frac{1}{0.25} = 4$. Feedback ratio B is independent of frequency, line variations, noise, etc. Therefore, although the gain of the system is greatly reduced, the output is linear with respect to the input. A degree of stability is also achieved by the inclusion of inverse feedback.

Further improvement in the stability of special circuits is accomplished by the employment of differential amplifiers which amplify only differences of input signals and are relatively independent of service voltage variations.

The techniques described above are further treated in the paragraphs concerning the circuits to which they apply.

2.2 COMMON CIRCUIT CHARACTERISTICS

2.2.1 Introduction

A thorough knowledge of signal inputs and outputs is a prerequisite in the understanding of special circuits. These inputs and outputs are pulses and levels which are further categorized as standard and nonstandard.

2.2.1.1 Standard Pulses

The standard pulse (fig. 2–3) is a +30V pulse (nominal) with a tolerance of ±10V. The pulse shape approaches that of the positive half of a sine wave, with a negative tail of indefinite value. The pulse width measured at the base has a nominal value of 0.1 μsec and a tolerance of ±0.02 μsec. It is evident that a standard pulse is defined by its amplitude, pulse width, and shape.

2.2.1.2 Standard Levels

There are two standard levels (fig. 2–4). The up level is a d-c potential of +10V (nominal); the other is the down level, a d-c potential of −30V (nominal). Rise time (T_R) is the period during which the potential climbs 40V from a down level to an up level. Fall time (T_F) is the period during which the potential drops 40V from an up level to a down level. The standard signals just discussed are represented as logic lines with characteristic terminating symbols (fig. 2–5). The standard pulse is indicated by a line terminated in a solid arrow head. The standard level, either up or down, is indicated by a line terminated in a solid diamond.

2.2.1.3 Nonstandard Signals

Any nonstandard pulse is indicated by a line terminated in an open arrowhead. Other nonstandard signals are indicated by a line terminated in an open diamond.

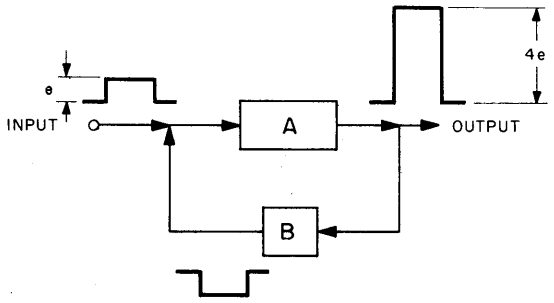


Figure 2–2. Amplifier with Inverse Feedback Loop, Block Diagram

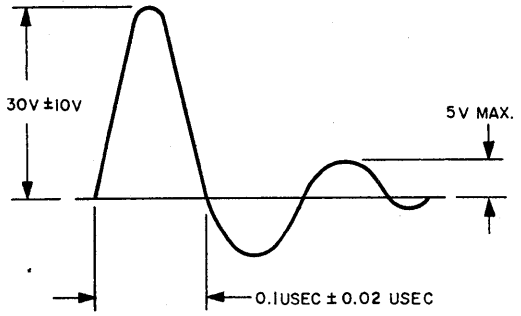


Figure 2–3. Standard Pulse

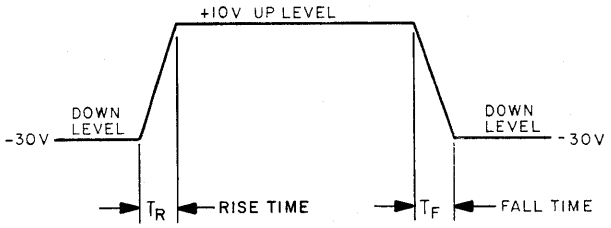


Figure 2–4. Standard Levels

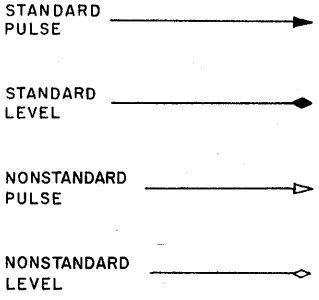


Figure 2–5. Standard Signal Symbols

2.2.2 Physical Characteristics

Several electrical circuit refinements are dictated by the physical layout and the techniques employed in the packaging of the special circuits. To appreciate the necessity for the electrical requirements peculiar to this equipment, it is advantageous to first become acquainted with the physical characteristics of the machine.

Special circuits generally consist of one or more card assemblies, together with other detail parts and wiring. The card assembly consists of detail parts which are automatically dip-soldered. Figure 2–6 presents a front and rear view of a typical card detail. The card is composed of a phenolic base which has been tooled as indicated in the figure. Both sides of the card detail contain printed circuitry which interconnects the appropriate lands. The typical card assembly, shown in figure 2–7, has the detail parts and lugs mounted. Several of these card assemblies are then mounted in a mechanical assembly and electrically connected to various detail parts such as vacuum tube sockets, individual resistors, capacitors, and electrical connectors. This complete assembly, called a pluggable unit (fig. 2–8), may consist of several basic and special circuits electrically connected.

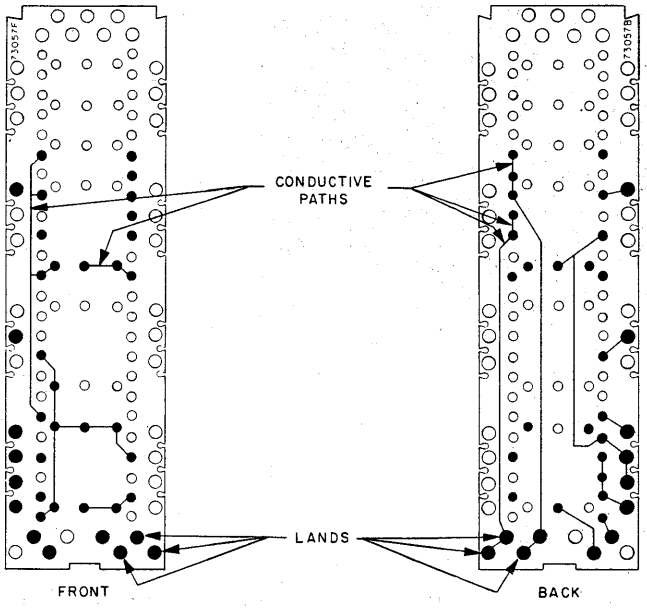


Figure 2–6. Typical Card Detail

This method of physical construction makes possible the automatic manufacture of the card assembly (which contains most of the detail parts employed) and the easy removal and replacement of the pluggable unit. There are two standard types of pluggable units, one which accommodates a maximum of nine vacuum tubes, seen in figure 2–8, and one with a maximum of six tubes (not shown). The electrical connectors mounted along the bottom of the pluggable unit provide a means of supplying service voltages and inputs to the unit. Outputs are also taken off at these points.

2.2.3 Parasitic Suppression

The manufacturing and packaging techniques just discussed result in lead lengths longer than those in common use.

Special circuits, for the most part, include vacuum tubes, and in circuits of this type where long leads are prevalent, parasitic oscillations usually result. Parasitic oscillations are undesirable, self-generated, cyclic voltages produced by unplanned resonant circuits appearing in the grid, plate, and screen circuits of a vacuum tube.

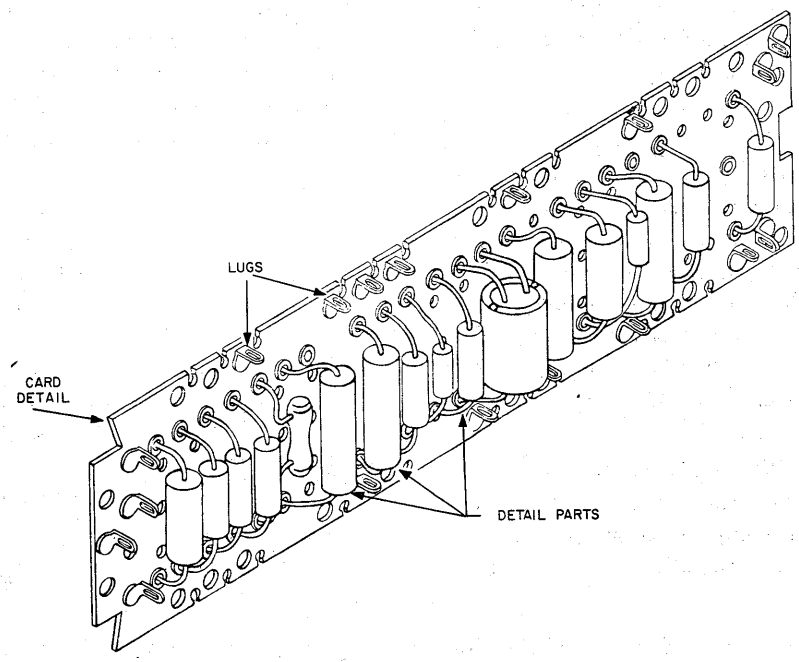


Figure 2–7. Typical Card Assembly

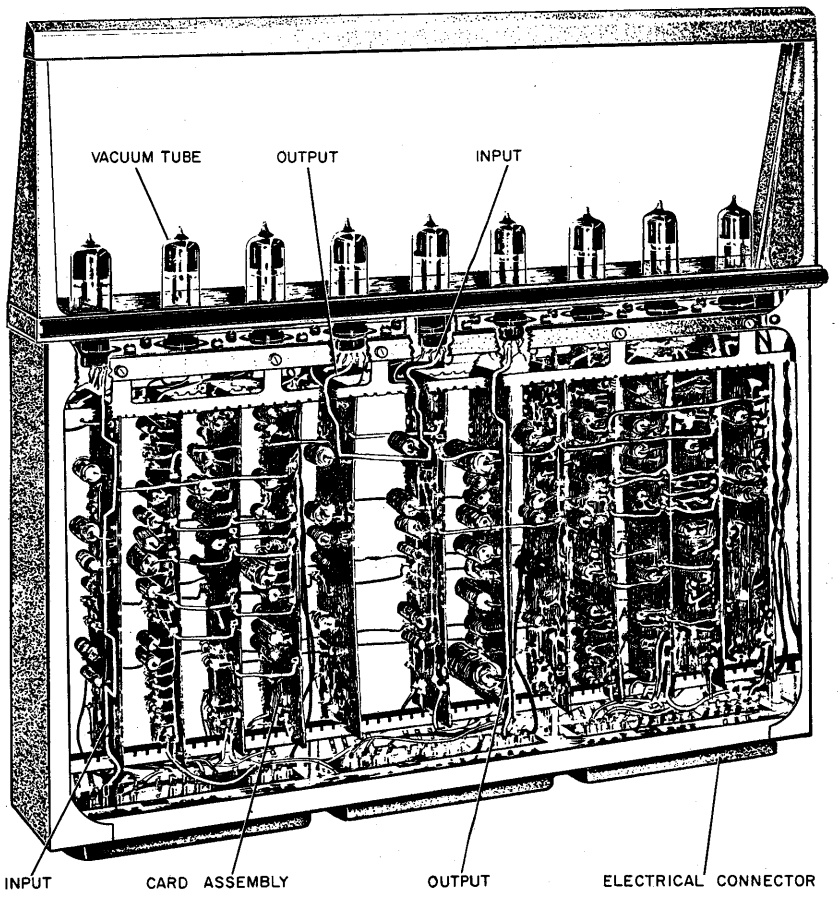


Figure 2–8. Typical Pluggable Unit

Figure 2–9 illustrates the effect of lumping long leads into equivalent inductances and lumping stray wiring and tube capacitances into equivalent capacitors. This circuit, which closely resembles a tuned-grid tuned-plate oscillator, could support oscillations.

To eliminate parasitic oscillations in this and in comparable circuits, parasitic suppressing resistors are used. Such resistors add loss into an undesirable resonant circuit, reducing the circuit's efficiency to such a degree that parasitic oscillation is no longer possible. Figure 2–10 shows circuitry of figure 2–9 with the parasitic suppressing resistors added. For maximum effectiveness, resistors are mounted at the vacuum tube socket. They will be found in a majority of the plate and control grid leads of vacuum tubes, and, where necessary, in vacuum tube cathode and screen leads.

In this manual, parasitic suppressors have been eliminated from the schematic drawings for simplification purposes. However these components appear, as mentioned above, in the actual schematic of each circuit.

2.2.4 RC Decoupling

The special circuits employed in the AN/FSQ-7 and -8 equipments derive their service voltages from common power supplies. For this reason, numerous vacuum tube circuits have their plate, control grid, cathode, and screen grid circuits returned through common leads (fig. 2–11). Long power leads and the sharing of a common return by many circuits contribute to the generation of undesired signals. Because these signals would affect machine dependability, RC decoupling circuits are em-

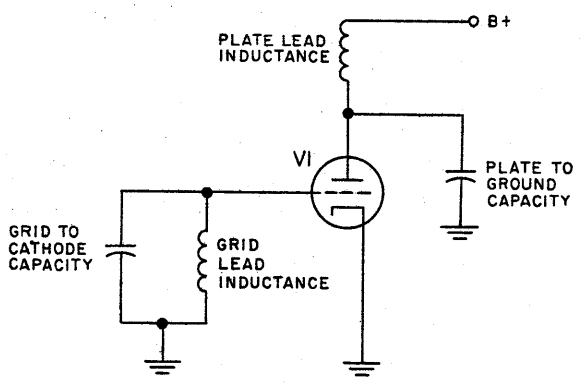


Figure 2–9. Lumped Constants, Equivalent Circuit, Simplified Schematic Diagram

ployed in all the vacuum tube return circuits to attenuate them. Figure 2–12 is the simplified schematic of one vacuum tube circuit employing an RC decoupling filter in each of its return paths. These RC filters attenuate undesirable signals appearing at the plate, cathode, control grid, and screen grid return circuits to such a degree that machine dependability is no longer threatened.

Figure 2–13 presents a typical RC decoupling circuit with the associated mathematics to explain its operation. It can be shown that if an RC decoupling filter functions satisfactorily at the lowest frequency (the frequency for which it was designed), its effectiveness will increase at higher frequencies. It should be noted that, although the attenuation of one of the RC filters has been calculated to be approximately 15, the attenuation between any two circuits, each employing one of these filters, is 15^2 or 225 (fig. 2–14).

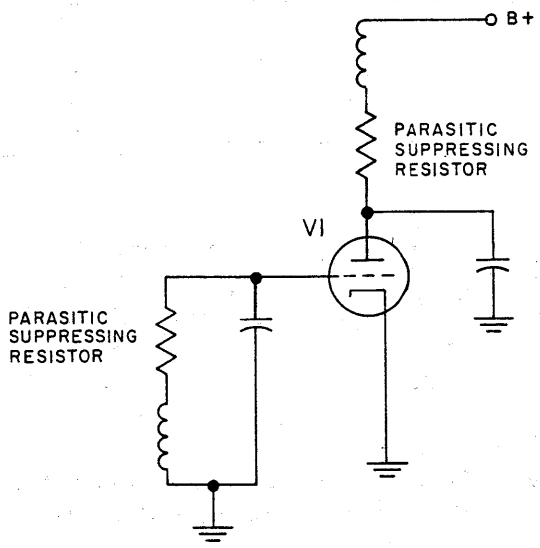


Figure 2–10. Lumped Constants, Equivalent Circuit with Parasitic Suppressing Resistors Added, Simplified Schematic Diagram

Note

The d-c potential at the output of the RC decoupling filter is assumed to be the same as the input or supply potential. The ohmic value of decoupling resistor R is small when compared with the resistance of the circuit returning at this point. For the same reason, this point is considered to be at a-c ground because of the extremely low value of reactance of decoupling capacitor C. As in the case of parasitic suppressors, the RC decoupling networks have been eliminated from the schematic drawings of each special circuit. As mentioned above, all service voltages are decoupled in the pluggable unit containing the actual circuits.

2.2.5 Common Circuits for Clamping and Coupling Levels

A number of circuit techniques are dictated by the functional requirements of the equipment. Two of these techniques, diode clamping and d-c coupling, are repeated in several of the special circuits and are therefore treated as a general circuit consideration.

2.2.5.1 Diode Clamping

Diode clamping is treated by considering this function as applied to a cathode follower (fig. 2–15).

The anode of crystal diode CR2 is biased at −30V. This diode will not conduct while the voltage at the output is more positive than −30V. When the voltage at the output falls below −30V, CR2 conducts, causing an increase in current through resistor R1 and raising the voltage at the output to the point where conduction through the diode ceases (−30V).

The cathode of crystal diode CR1 is biased at +10V. This diode will not conduct while the voltage at the output is less positive than +10V. If the voltage at the output rises slightly above +10V, CR1 conducts. Any

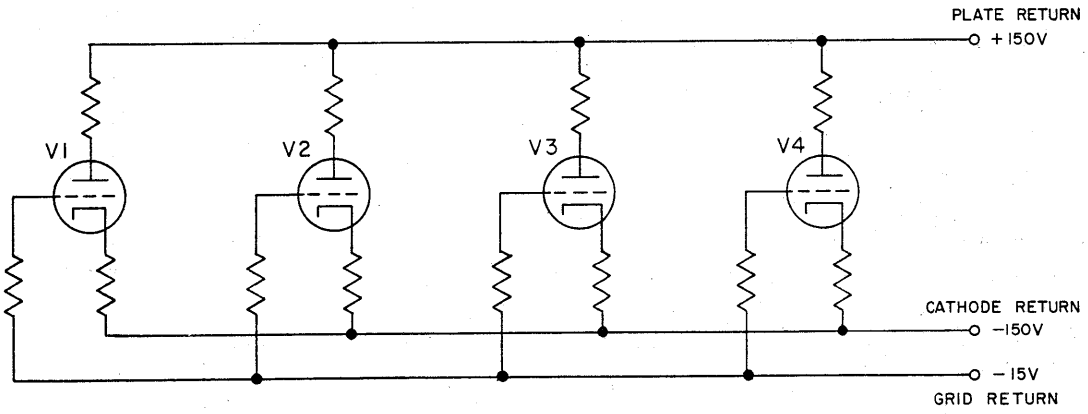


Figure 2–11. Common Return Paths, Simplified Schematic Diagram

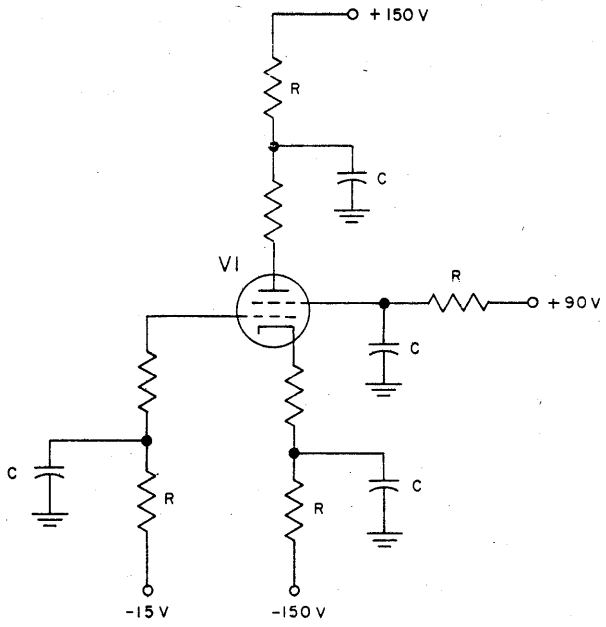
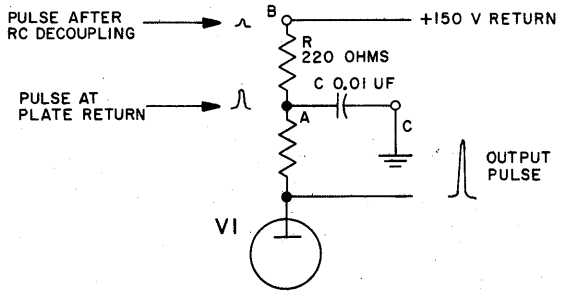


Figure 2–12. RC Decoupled Returns, Simplified Schematic Diagram



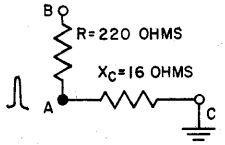
REACTANCE OF C IS $X_C = \frac{1}{2\pi FC}$

WHERE
$2\pi = 6.28$
$F = 10^6$ CPS (LOWEST FREQUENCY WHERE DECOUPLING OF THIS CIRCUIT IS REQUIRED)
C = 0.01 UF

THEN

$$X_C = \frac{1}{6.28 \times 10^6 \times 0.01 \times 10^{-6}} = 15.9 \text{ OHMS}$$

FOR SIMPLICITY, LET X_C = 16 OHMS AND CONSIDER IT TO BE RESISTIVE. THEN THE RC DECOUPLING CIRCUIT MAY BE REDRAWN



AN ALTERNATE VOLTAGE (PULSE) AT A, WILL CAUSE CURRENT TO FLOW IN TWO PATHS, A TO B AND A TO C

IT IS $\frac{220}{16}$ TIMES EASIER FOR CURRENT TO FLOW THROUGH A TO C THAN IT IS THROUGH A TO B, $\frac{220}{16}$ = 14 APPROX. THEREFORE, 14 TIMES MORE PULSE CURRENT WILL FLOW THROUGH A TO C THAN THROUGH A TO B, AND THE AMPLITUDE OF THE PULSE REMAINING AT B WILL BE ATTENUATED 15 TIMES.

Figure 2–13. RC Decoupling, Simplified Schematic Diagrams and Calculations

increase in current through vacuum tube V1 (which would produce a voltage increase across R1 at the output) is supplied by the +10V bias supply through CR1. In this manner, the output of the cathode follower in figure 2–15 is limited to an up level of +10V and a down level of −30V. Varying loads and aging of components could produce undesirable variations of levels at the output where they are not clamped as indicated.

2.2.5.2 D-C Coupling

In several of the special circuits it is necessary to dc-couple the plate of one stage to the control grid of another. This requirement will be found in the circuits either operating on or producing levels.

Figure 2–16 is a simplified schematic diagram illustrating a d-c coupling network. Assume (fig. 2–16,A) that the output levels required are −30V and +10V, alternately. This would require that the voltages at the control grid of V2 be d-c levels of approximately −30V

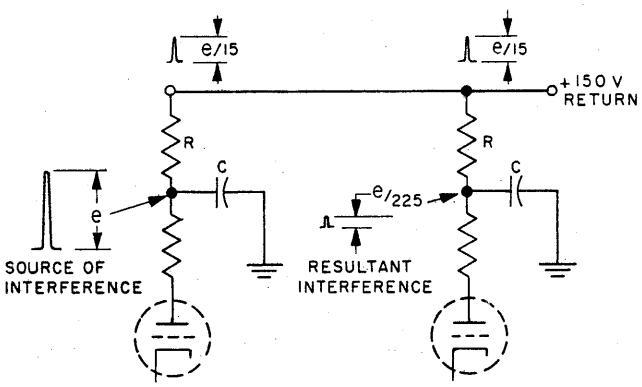


Figure 2–14. Attenuation of Interaction through RC, Simplified Schematic Diagram

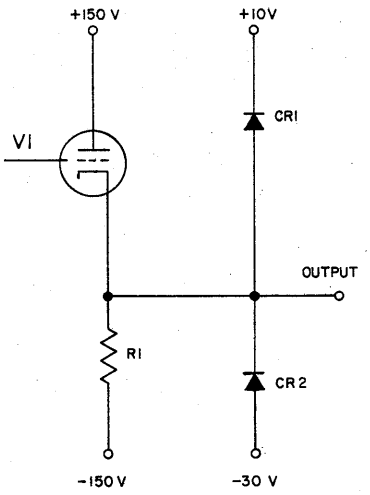
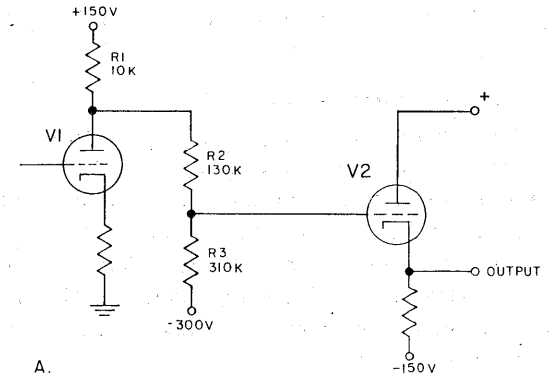
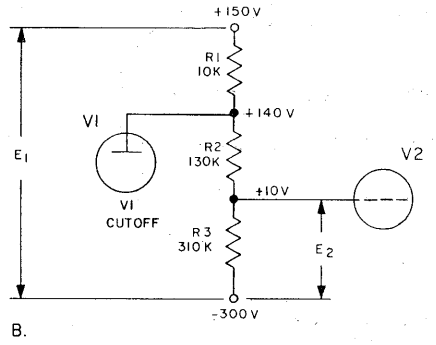


Figure 2–15. Diode-Clamped Cathode Follower, Simplified Schematic Diagram

and +10V, alternately. Since levels are being coupled, a d-c coupling is indicated (one that will pass direct current); therefore, neither a transformer nor a capacitor may be employed as the primary coupling device. The control grid, on the other hand, cannot be directly connected to the plate because the level conditions (+10V and −30V) could never be reached in this manner. The method of d-c coupling illustrated in figure 2–16,B, employs a voltage divider consisting of the plate resistor of V1 (R1), resistor R2, and resistor R3.

With vacuum tube V1 cut off, the current flowing through R1, R2, and R3 develops a +10V level (E2)





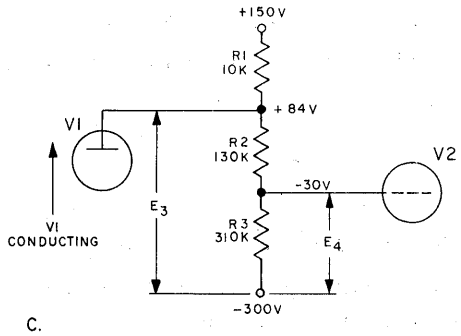


Figure 2–16. D-C Coupling Network, Simplified Schematic Diagram

at the control grid of vacuum tube V2. The mathematics supporting this conclusion follows. The voltage (E1) across R1, R2, and R3 is

$$E_1 = +150V - (-300V)$$
$$= 450V$$

and the current (I_1) through R1, R2, and R3 is

$$I_1 = \frac{E_1}{R_1 + R_2 + R_3}$$
$$= \frac{450}{10 \times 10^3 + 130 \times 10^3 + 310 \times 10^3}$$
$$= \frac{450}{450 \times 10^3}$$
$$= 1 \times 10^{-3} \text{ amperes}$$

Therefore, the voltage (E_2) developed across R_3 is

$$E_2 = I_1 R_3$$
$$= 1 \times 10^{-3} \times 310 \times 10^3$$
$$= 310V$$

and the voltage at the grid of V2 with respect to ground is

$$E_g = E_2 + (-300V)$$
$$= +310 - 300V$$
$$= +10V$$

where

E_g = voltage at control grid of V2 with respect to ground.

With V1 conducting, the additional current flowing through R1 drops the potential at the plate of V1 to +84V (fig. 2–16,C). As a result, the voltage (E_3) across R2 and R3 becomes

$$E_3 = +84V - (-300V)$$
$$= 384V$$

and the current (I_3) through R2 and R3 is reduced

$$I_3 = \frac{E_3}{R_2 + R_3}$$
$$= \frac{384}{130 \times 10^3 + 310 \times 10^3}$$
$$= 0.873 \times 10^{-3} \text{ amperes}$$

The voltage drop (E_4) across R3 now is

$$E_4 = I_3 \times R3$$
$$= 0.873 \times 10^{-3} \times 310 \times 10^3$$
$$= 270V$$

and the voltage (E_g) at the control grid of V2 with respect to ground is

$$E_g = E_4 + (-300V)$$
$$= 270V - 300V$$
$$= -30V$$

It can be seen that this method of returning the plate to a highly negative potential through a voltage divider enables the coupling of levels from a plate operating at a higher bias to a grid operating at a lower bias.

2.2.6 Speedup Circuits

System performance in AN/FSQ-7 and -8 is frequently dependent upon the speed at which levels shift. This makes rise and fall time an important characteristic of level outputs. The speedup of rise and fall time is a requirement satisfied by circuit configurations in certain of the special circuits which produce levels.

2.2.6.1 Voltage Divider Compensation

One of the most routine methods employed to effect the shortening of rise and fall time is voltage divider compensation. Figure 2–17 is the simplified schematic diagram of a compensated d-c coupling network. This schematic includes two capacitors not included in figure 2–16,A; i.e., C1 and C2. Capacitor C1 is a compensating capacitor and C2 is the input capacity of V2. This input capacity, which must be compensated for, consists of stray capacity plus the effective grid-to-ground capacity of V2. Were it not for compensation, the capacity of C2 would result in a slow rise and fall at the output of V2 (fig. 2–18). It can be seen that in the uncompensated output there is considerable curvature at the corners of the waveform. This is caused by the attenuation of the high-frequency components of which level shifts are composed. The level itself is not affected since it consists of low frequency and d-c components which are not attenuated by C2 capacitance.

Capacitor C1 bypasses R2 (fig. 2–17), increasing the amplitude of high-frequency components at the grid of V2 by the same amount that they are attenuated by capacity C2. This results in a compensated (speeded up) output seen in figure 2–18.

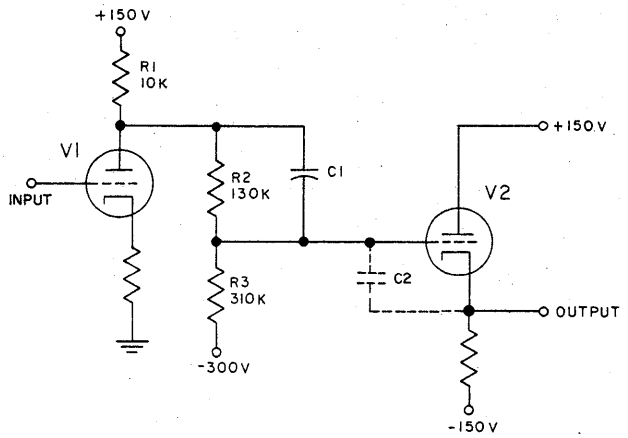


Figure 2–17. Compensated D-C Coupling Network, Simplified Schematic Diagram

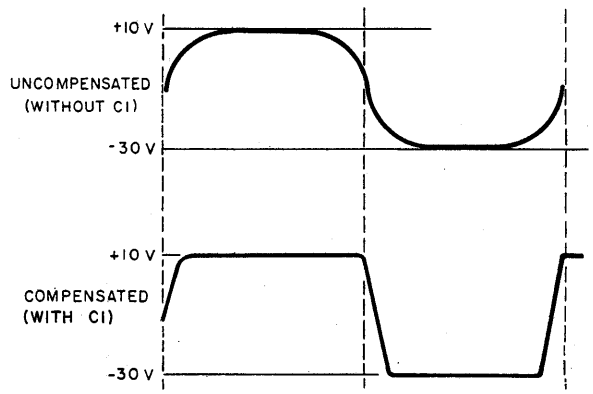


Figure 2–18. Output Waveform (V2 in Fig. 2–17)

2.2.6.2 Peaking Coils

Another method of speeding up rise and fall time entails the use of a peaking coil (fig. 2–19). The various capacities affecting the resultant output at the plate V1 are represented as C1. Without compensation, the high-frequency components of the output waveform would be attenuated by the bypassing effect of C1 and the resultant waveform would be that indicated by the broken line.

Including L1 in series with R1 produces an effective plate load

$$Z = R1 + X_L$$

where

Z = the plate load impedance

X_L = the inductive reactance of peaking coil L1.

$$X_L = 2\pi FL$$
$$= 6.28\,FL$$

where

F = frequency in cycles per second

L = inductance of peaking coil L1 in henries.

It is apparent that the load impedance (Z) is a function of frequency. The higher the frequency the larger X_L becomes and, hence, the larger Z becomes.

The gain of an amplifier is proportional to the expression

$$\frac{Z}{R_p + Z}$$

where

R_p = plate resistance of V1, a constant.

It follows that the greater Z becomes, the greater will become the gain of this stage.

As was previously stated, Z increases with frequency. Therefore, the gain and, eventually, the output of V1

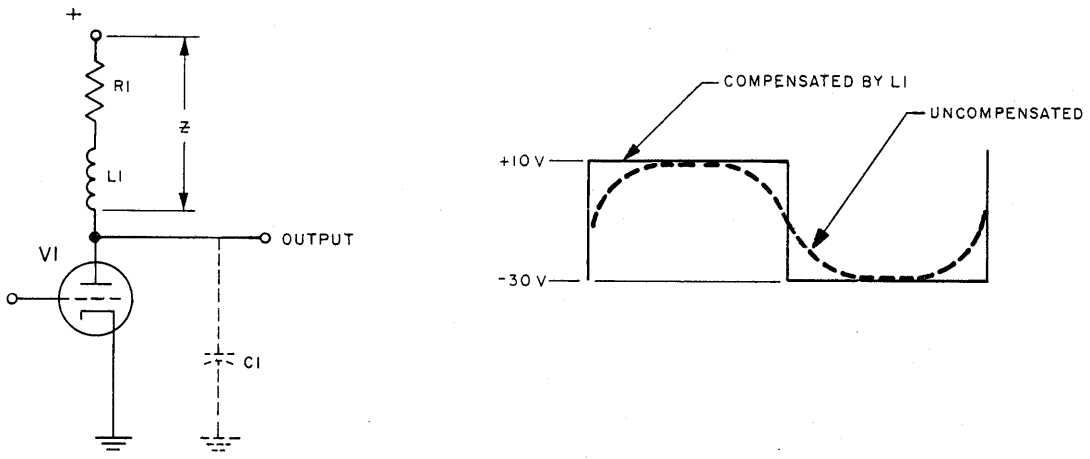


Figure 2–19. Peaking Coil Compensated Plate Circuit, Simplified Schematic Diagram with Waveform

will increase with frequency. This is opposite to the effect of C1, and the resultant waveform is compensated as indicated by the solid line.

At d-c and for low frequencies, the reactance (X_L) of peaking coil L1 is of an extremely small magnitude and therefore has no effect on the circuit. It can be seen that the level output is not affected by the inclusion of L1. On the other hand, the rise and fall times which include high-frequency components are effectively shortened (speeded up).

CHAPTER 3

SPECIAL CIRCUITS, THEORY OF OPERATION

3.1 ALL-CHANNEL DRIVER

3.1.1 Definition and Description

The all-channel driver (ACD) is a nonlogic circuit which produces a sine wave output. The logic block symbol for the ACD is shown in figure 3–1. In the Output System, the ACD supplies a sine wave output which drives a matching amplifier circuit and a logic driver for each of the channels supplying data to the telephone equipment.

3.1.2 Principles of Operation

Figure 3–2 is the schematic diagram for the ACD. The circuit consists of two model D cathode followers of standard design. For details of operation, refer to the cathode follower writeup in the basic circuits manual.

3.2 ANALOG COUNTERS

3.2.1 Definition and Description

Analog counters (AC's) are storage counters which produce outputs capable of energizing alarm relays. Table 3–1 lists the two models of AC circuits utilized in AN/FSQ-7 and -8 equipments. Each model is listed by logic symbol showing the characteristics which distinguish one from the other.

TABLE 3–1. ANALOG COUNTERS, MODEL-DISTINGUISHING FEATURES

MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A	AAC	Employed as an excessive target information alarm. The input is a pulse repetition frequency (PRF) of 1,600 pps. The output is a 10-ma relay pick current (9 to 12 pulses at a PRF of 1,600 pps).
B	BAC	Employed to detect the existence of missing or spurious azimuth pulses. The input is a pulse whose width is between 5 μsec and 120 ms; the PRF is 4 to 40 pps. The output is a 10-ma relay pick current (10 to 30 pulses at the same PRF as the input).

3.2.2 Principles of Operation

The electronic function of both AC's is identical; therefore, only the model A is described in detail below.

Figure 3–3 is the schematic diagram for the AAC. Table 3–2 lists the associated detail parts and their functions. The circuit consists of a cathode follower, an incremental storage bank, and a relay driver. The input signal to cathode follower V1A is a −30 +10V ampli-

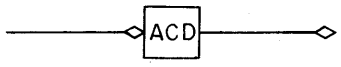


Figure 3–1. All-Channel Driver, Logic Block Symbol

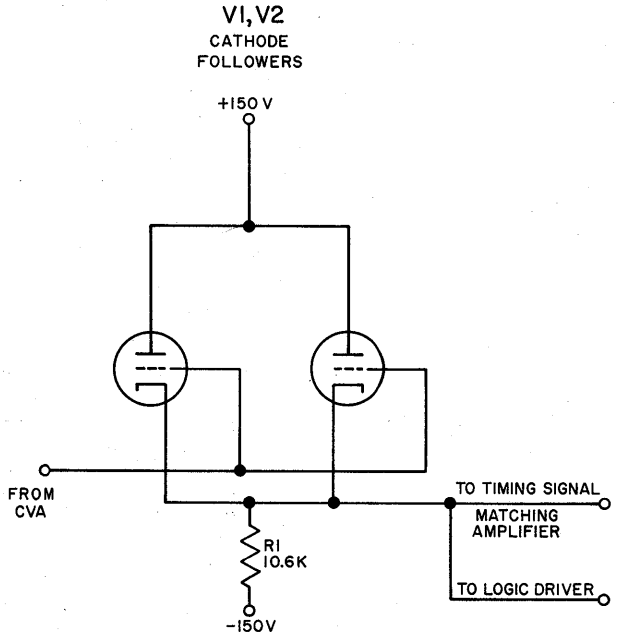


Figure 3–2. All-Channel Driver, Schematic Diagram

tude reintensification pulse whose duration is 180 μsec. This positive pulse appears at the output of the cathode follower and is coupled to the plate of V2A and the cathode of V2B through paralleled capacitors C1 and C2. The plate of V2B, being connected to the —30V source will not allow this diode to conduct. Tube V2A, on the other hand, having its cathode tied to the —30V source through R3 will conduct and will apply a charge to the capacitor bank designated C3, but consisting of four 1-μf capacitors in parallel. Considering the time constant in the RC network of C1, and C2 with R2, it can be concluded that, when the charges on the capacitor bank occur at a slow rate, the capacitor bank will discharge between successive pulses. However, when the reintensification pulses occur at a fast rate, the capacitor bank does not have sufficient time to discharge between pulses; therefore, successive pulses place an incremental charge on the capacitor bank. Incremental charges on the capacitor bank will eventually raise the voltage at the grid of tube V1B, which is normally maintained at cutoff, and will cause plate current in this tube to energize alarm relay K16, whose coil is connected in series with the plate supply line of V1B.

3.3 ANALOG LINE DRIVER

3.3.1 Definition and Description

The analog line driver (ALD) is a nonlogic circuit which amplifies the analog level outputs of a binary de-

TABLE 3–2. ANALOG COUNTER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1A
R2	Cathode load for V1A
R3	Capacitor bank load for C3
R4	Grid resistor for V1B
R5	Cathode bias for V1B
L1	Delays surge voltages
K16	Alarm relay
C1, C2	Coupling capacitors
C3	Capacitor bank consisting of four 1-μf capacitors in parallel

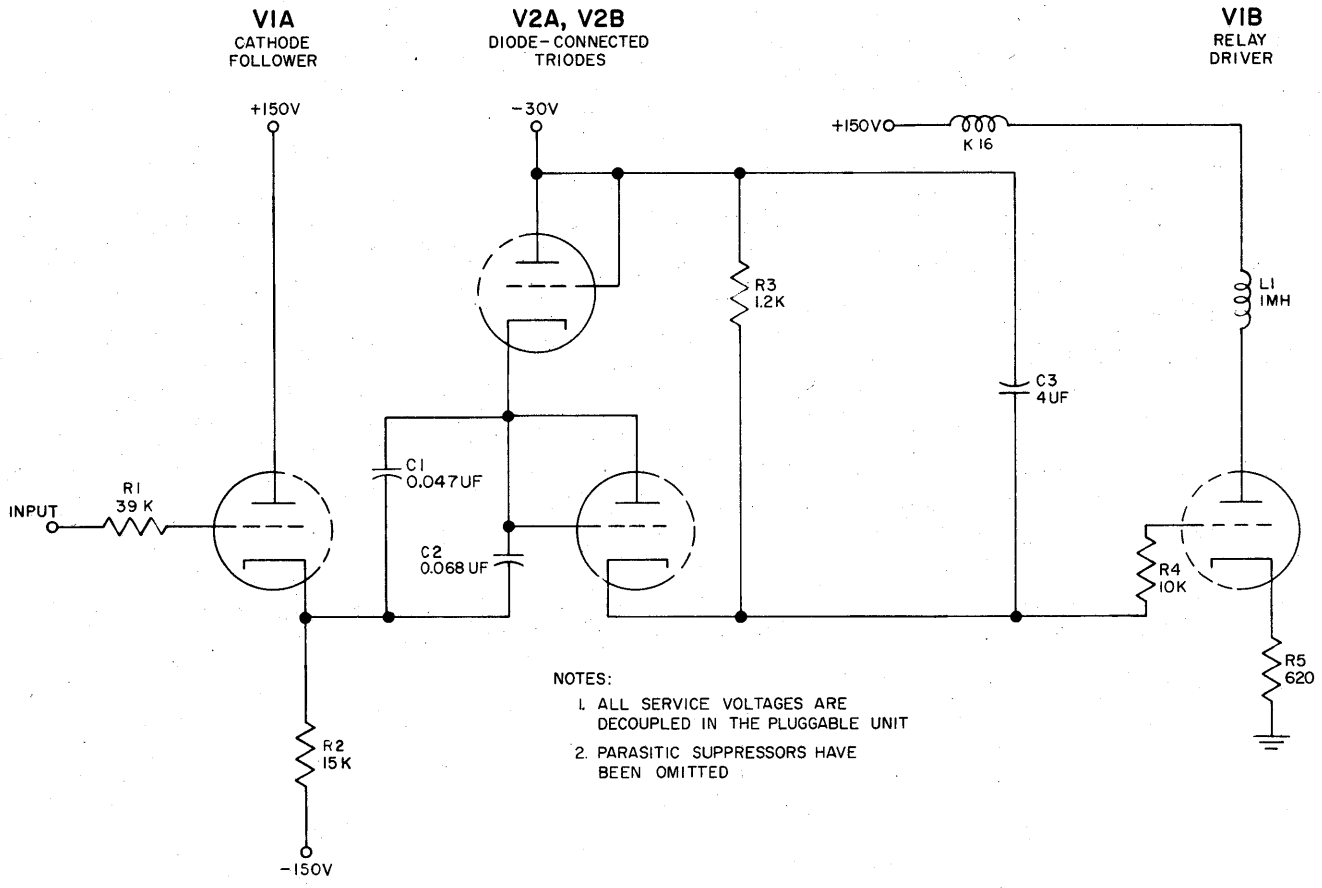


Figure 3–3. Analog Counter, Model A, Schematic Diagram

coder. The output of the ALD provides the power to drive the consoles and associated lines in the situation display (SD) system. The logic block symbol for the ALD is illustrated in figure 3–4.

3.3.2 Principles of Operation

3.3.2.1 Basic Operation

Figure 3–5 is the block diagram of the ALD. Analog levels are fed into the input terminals designated –X and +X. The output levels of the ALD are fed back to the input through a mixing network in reverse; that is, the +X output is fed to the –X input and the –X output is fed to the +X input. This is required to establish the phase reversal necessary in degenerative feedback. The table in figure 3–5 indicates the three input conditions for each of the three applications of the ALD.

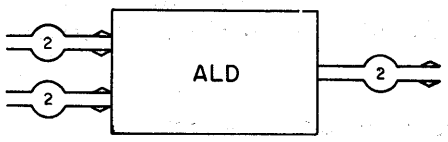
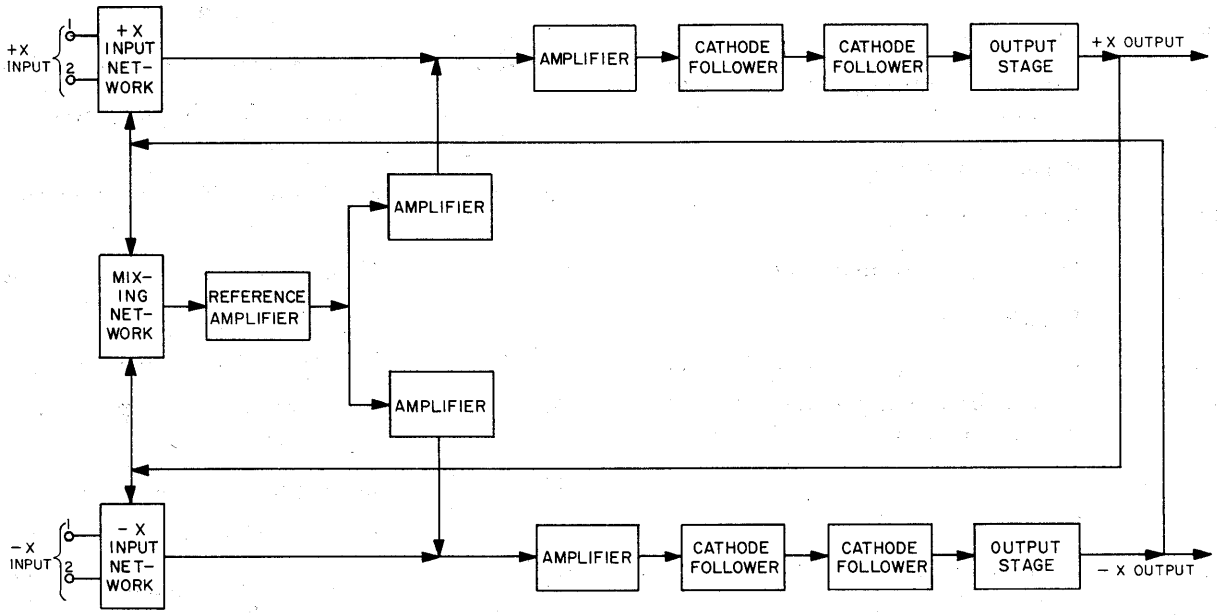


Figure 3–4. Analog Line Driver, Logic Block Symbol

3.3.2.2 Detailed Operation

Figure 3–6, foldout, is the schematic diagram of the ALD. Table 3–3 lists the associated detail parts and their functions.

An analog level applied at the +X input is divided across the input network and appears at the grid of vacumm tube V2. This level is amplified, inverted, and directly coupled to the grid of cathode follower V4A. A portion of the output of V4A is directly coupled to vacuum tube V5A, a triode cathode follower stage. The output of V5A is directly coupled from its cathode to the control grids of seven paralleled, power amplifier tubes (driver). The driving output is obtained at the



FED FROM	INPUTS			
	+X		–X	
	1	2	1	2
VECTOR GENERATOR DECODER	VECTOR SELECTION	VECTOR SWEEP	VECTOR SELECTION	VECTOR SWEEP
CHARACTER SELECTION DECODER	CHARACTER SELECTION		CHARACTER SELECTION	
CHARACTER POSITIONING DECODER	CHARACTER POSITIONING		CHARACTER POSITIONING	

Figure 3–5. Analog Line Driver, Block Diagram

plates of these tubes. The function of the —X channel is identical with that of the +X channel. The +X and —X feedback appears across resistors R10, R11, and R12 in series. The moving arm of potentiometer R11 samples the mean level and feeds the input of the regulator across constant current tubes V11A and V11B. This input is coupled to a reference amplifier (consisting of vacuum tubes V15 and V16) by cathode follower V12. Reference amplifier V15 compares the mean level applied to its cathode with a reference level manually set by potentiometer R50.

Assume that the mean level sampled at R11 has shifted in a positive direction. The potential difference between the cathode and grid of V15 increases. This positive increase at the cathode raises the voltage at the plate of V15 which is directly coupled to the grids of V1A and V1B. An increase in potential at this point results in a decrease in potential at the plates of V1A and V1B. These plates are directly coupled to the grids of V2 and V3. The decrease in potential on the control grids of these pentodes results in an increase in potential at the plates. This increase is cascaded through cathode followers (V4A, V5A and V4B, V5B) and appears as an increase in potential on the grids of the paralleled driver output tubes. This results in a decrease in potential at the parallel plates of the output tubes, correcting the initial condition which produced the positive shift of the mean level. A negative-shift mean level would produce an identical correction, but of the reverse polarity.

TABLE 3–3. ANALOG LINE DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1-C6	Speedup capacitors	R28, R29	Grid current-limiting resistors for V5A and V5B
C7, C8	Bypass capacitors	R30, R31	Cathode resistors for V5A and V5B
C9	Part of smoothing network (with R48)	R32	Common plate dropping resistor for V5A and V5B
C10	Bypass capacitor	R33	Plate load resistor for paralleled output stages
R1, R2	Isolating resistors	R34	Common cathode resistor for output tubes
R3, R4	Part of input mixing network	R35, R36	Balance decoupling resistors
R5, R6	Isolating resistors	R37	Plate load resistor for paralleled output stages
R7-R13	Part of input mixing network with R8 as balancing potentiometer and R11 as mean level coupling potentiometer	R38	Current-limiting resistor for V10
R14	Cathode resistor for V1A	R39, R40	Voltage divider
R15	Position control	R41	Common cathode resistor for V11A and V11B
R16	Cathode resistor for V1B	R42	Cathode load for V12
R17	Common cathode resistor for V2 and V3	R43	Ensures firing of V14
R18, R19	Plate load resistors for V2 and V3, respectively	R44, R45, R46	Voltage divider with R45 as mean level reference potentiometer and R46 as current-limiting resistor
R20, R21	Balancing network	R47	Plate load for V15
R22, R23	Grid returns for V4A and V4B	R48	Part of smoothing network (with C9)
R24, R25	Cathode load for V4A	R49, R50	Cathode load for V16
R26, R27	Cathode load for V4B		

3.4 AREA DISCRIMINATOR, MODEL B

3.4.1 Definition and Description

The model B area discriminator (BAD), a nonlogic circuit, is a photoelectric device employed to generate a pulse whose voltage is proportional to the light intensity falling on its photosensitive element. The output represents a timing index associated with the data displayed on the unmasked areas of the situation display cathode-ray tube (SD CRT). The logic block symbol for the BAD is shown is figure 3–7.

3.4.2 Principles of Operation

Figure 3–8 is the schematic diagram for the BAD. Table 3–4 lists the associated detail parts and their functions. The circuit consists of a photomultiplier tube, an optical system, and the associated circuits.

The cathode potential of V1 (photomultiplier) is —1,200V; by successive steps, potentials approaching the plate voltage (+600V) are applied to the dynodes of V1. Some dynodes are connected to fixed voltage terminals whereas others are supplied from voltage dividers. With the cathode operating at —1,200V and the plate at 600V, an 1,800V accelerating potential is achieved while still maintaining a degree of safety precaution (maximum voltage to ground is 1,200V). The dynodes in the photomultiplier are coated with an electron emissive substance. Each dynode emits slightly more than four times the number of electrons that strike it, effecting a current multiplication, from cathode to anode, of approximately 1,000,000.

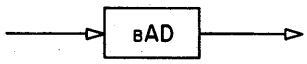


Figure 3–7. Area Discriminator, Model B, Logic Block Symbol

The output of the photomultiplier is proportional to the blue light emanated from the unmasked areas of the display screen. The output is a negative pulse the amplitude of which is adjusted with potentiometer R9. This pulse is fed from the moving arm of R9 through coupling capacitor C7 to the area discriminator amplifier.

3.5 AREA DISCRIMINATOR AMPLIFIER, MODEL A

3.5.1 Definition and Description

The model A area discriminator amplifier (AADA) is a nonlogic circuit employed to amplify and shape the electrical pulses from the area discriminator. The logic block symbol for the AADA is shown in figure 3–9.

3.5.2 Principles of Operation

3.5.2.1 Basic Operation

The schematic diagram for the AADA is shown in figure 3–10, foldout. Table 3–5 lists the associated detail parts and their functions.

TABLE 3–4. AREA DISCRIMINATOR, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1-C5	Form capacitor network which prevents voltage fluctuations caused by transients
C6	Output coupling capacitor
C7	Bypass capacitor
R1, R2, R3	Form voltage divider
R4, R5, R6, R7	Form voltage divider
R8	Plate load resistor for V1 and output amplitude control.

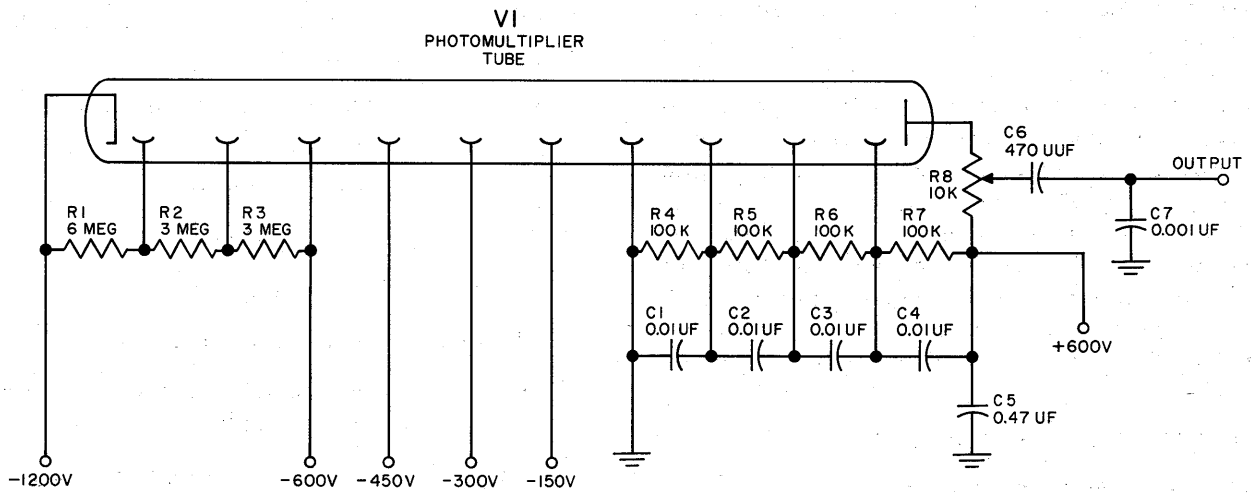


Figure 3–8. Area Discriminator, Model B, Schematic Diagram

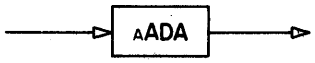


Figure 3–9. Area Discriminator Amplifier, Model A, Logic Block Symbol

The first three stages of the AADA amplify and invert the low level negative-going input pulse from the area discriminator. The amplified positive-going pulse at the plate of V3 is then applied to cathode follower V4, an interstage buffer. The positive pulse, at the cathode of V4, is capacitively coupled to six paralleled cathode followers. The grids of these cathode followers are clamped between +10 and −30V. The output is a positive-going pulse 40V in amplitude.

3.5.2.2 Detailed Operation

With no input, V1 conducts heavily. The negative-going input from the area discriminator reduces the plate current and increases the plate voltage of V1, producing a positive-going input to V2. This stage is biased past cutoff by −10.7V applied to the grid through the voltage divider consisting of R4 and R5. Triode V2 conducts when its bias is overcome by the positive pulse coupled through capacitor C2. Crystal diode CR1 clamps the grid side of C2 at −10.7V. The positive pulse input to V2 produces an increase in plate current and a resultant negative voltage pulse at the plate of V2.

Triode V3 is operated with grid and cathode at ground potential. The negative pulse output from V2, coupled through capacitor C6, produces a positive-going output at the plate of V3. This pulse is applied through coupling capacitor C8 to V4. This stage is biased at −30V and the operation of its grid current is identical with that of V2. Cathode follower V4 acts as a buffer between the voltage amplifier section of the AADA (V1, V2, and V3) and the paralleled power cathode followers.

The output of V4, a positive-going pulse, is capacitor-coupled to the grids of the six paralleled cathode followers through capacitor C12. The grid level of these tubes, with no input, is set at −30V by diode clamp CR4. Since the cathodes are returned to −150V through resistor R36, the cathode followers normally are conducting, resulting in a cathode potential that equals the grid voltage (−30V). The circuit output developed across R36 follows the input swing, which is clamped between −30V and +10V by crystal diodes CR4 and CR3. The resulting output is a positive-going pulse 40V in magnitude (−30 to +10V). Six paralleled cathode followers are employed to deliver the required power at the output terminal.

3.6 AUTOMATIC GAIN CONTROL

3.6.1 Definition and Description

The automatic gain control (AGC) is a nonlogic circuit that provides two clamping levels with a voltage spread that is determined by the amplitude of an input triangular wave. As the input signal amplitude increases, the voltage spread decreases. When the input signal amplitude decreases, the voltage spread increases. The logic block symbol for the AGC is shown in figure 3–11.

In Input System logic, the AGC is part of the triangular wave generator in the azimuth synchronizing circuit group. The heart of the triangular wave generator is the model A Miller integrator (AMI) (par. 3.54) which converts a square wave of varying frequency into a triangular wave. The amplitude of the triangular wave is a function of the input frequency; the lower the frequency, the greater the amplitude, and the higher the frequency, the smaller the amplitude. The AGC circuit is employed to ensure a constant amplitude output from

TABLE 3–5. AREA DISCRIMINATOR AMPLIFIER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	V1 grid return
R2	Plate load for V1
R3	Grid return for V2
R4, R5	Form voltage divider
R6	Grid limiting for V1
R7	Plate load resistor for V2
R8	Grid return for V3
R9	Plate load resistor for V3
R10	Grid return for V4
R11	Cathode load resistor for V4
R12	Grid return for paralleled cathode followers
R13	Cathode load resistor for paralleled cathode followers
C1	Coupling capacitor
C2	Bypass capacitor
C3-C5	Coupling capacitors
CR1, CR2	Crystal diode, clamp
CR3	Crystal diode, clamps grids of paralleled cathode followers at +10V
CR4	Crystal diode, clamps grids of paralleled cathode followers at −30V

the Miller integrator by monitoring the triangular wave output and regulating the amplitude of the square wave input to the Miller integrator as required. The AGC is fed by the level amplifier (LEA) (par. 3.42) and supplies clamping levels to the Miller integrator.

3.6.2 Principles of Operation

The AGC (fig. 3–12) consists of a cathode follower isolating stage, V1, two half-wave rectifiers, V2 and V3, and two output cathode follower stages, V4 and V5. Table 3–6 lists the associated detail parts and their functions.

The LEA output is assumed to be 80V peak to peak. Half this voltage is applied to the AGC through a voltage divider. The time constant of R1 and C1 (0.017 sec) is small compared to the period of the input voltage (0.12 sec). As a result, the voltage developed across C1 closely approximates the LEA triangular wave output. However, the voltage developed across the primary of T1 is the positive half of the input voltage. Tube V1 is cut off during the negative half cycle of input voltage, and with no current through the primary of T1, there is

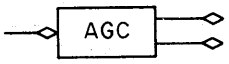


Figure 3–11. Automatic Gain Control, Logic Block Symbol

TABLE 3–6. AUTOMATIC GAIN CONTROL, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input integrating circuit (with R1)
C2-C7	Filter capacitors
CR1, CR2	Clamping diodes
R1	Input integrating circuit (with C1)
R2-R7	Filter resistors
R8, R9	Grid return for V4 and V5, respectively
R10, R11	Cathode load for V4 and V5, respectively
T1	Coupling transformer

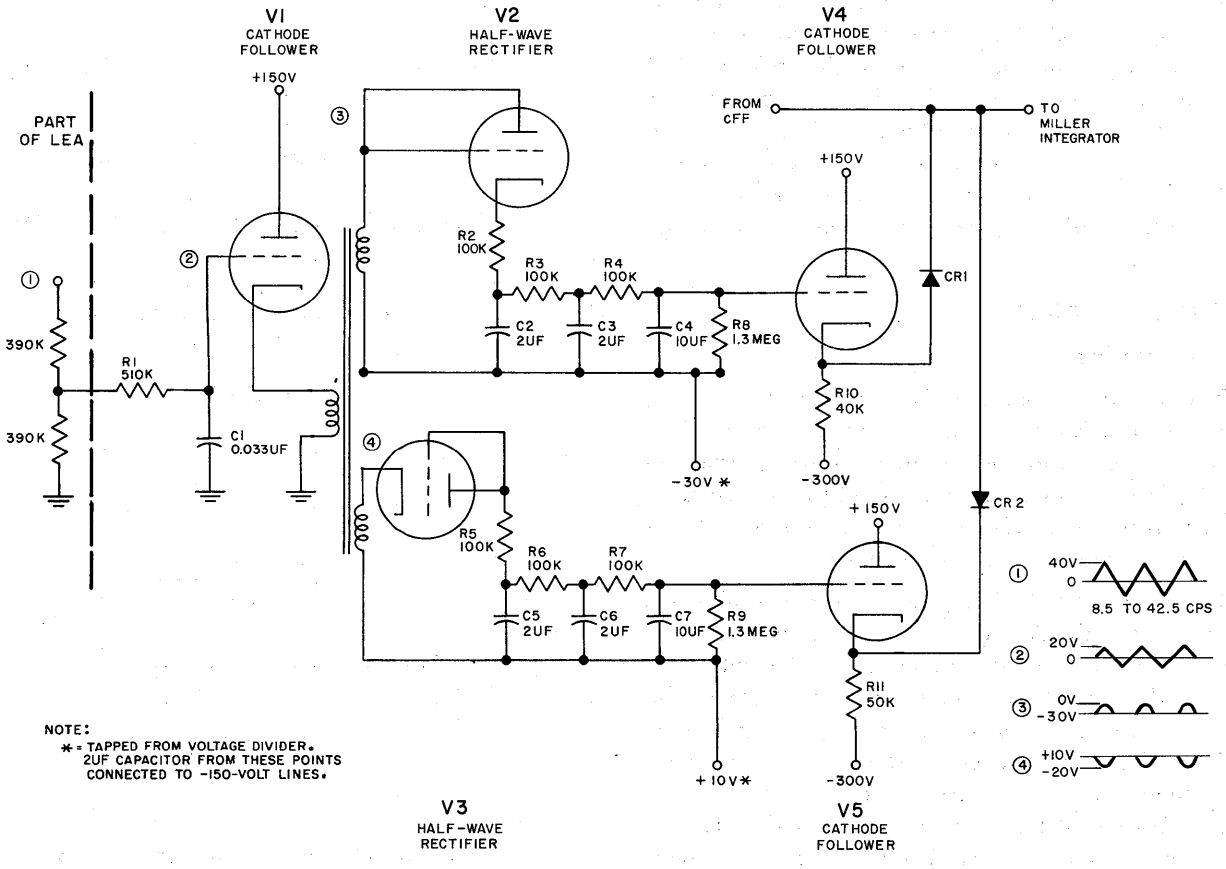


Figure 3–12. Automatic Gain Control, Schematic Diagram

no induced voltage. Dots are used to identify terminals of like polarity in T1. Thus, as terminal 2 becomes positive with respect to terminal 1, terminal 5 becomes positive with respect to terminal 6, and terminal 4 becomes negative with respect to terminal 3. Terminal 6 is referenced to —30V. Terminal 3 is referenced to +10V. The reference voltages are obtained from a voltage divider not shown in figure 3–12.

Consider the circuit associated with V2. The voltage developed across winding 5-6 is a series of positive half cycles of a triangular wave. Negative overshoots (terminal 5 becoming more negative than —30V) have no effect on the output developed across R8 because of the plate and cathode connections of V2. For each positive excursion of terminal 5, V2 conducts and current flows through winding 5-6, V2, R2, R3, R4, and R8. The current is pulsating and may be resolved into a d-c component and an a-c component called ripple.

Capacitors C2, C3, and C4 present a low impedance to the ripple and smooth out the pulsating current to leave a relatively constant direct current. This current is proportional to the amplitude of the input signal. Therefore, the voltage developed across R8 is proportional to the input voltage amplitude. Cathode follower V4 follows this d-c voltage and provides the clamping voltage between —30V and —10V for the negative level of the square wave being fed to the Miller integrator. Similarly, V3 and its associated detail parts develop the clamping voltage between +10V and —10V for the upper level of the square wave being fed to the Miller integrator. The voltage rise developed across R9 is equal in magnitude to the voltage fall developed across R8. The clamping levels, therefore, will approach —10V from maximums of +10V and —30V as the input voltage amplitude increases.

3.7 BINARY DECODERS

3.7.1 Introduction

The binary decoders (BD) are digital-to-analog voltage conversion circuits. Analog voltages are required to display data on cathode-ray tubes. However, the data to be displayed is processed and stored by the computer in binary form. The BD's translate these binary levels into the required display control voltages.

Five models (A, B, C, D, and F) of binary decoders are employed in the AN/FSQ-7 and -8; models A, B, C, and D in the Display System and model F in the Input System. All the binary decoders consist of three fundamental circuits: ladder section (LS), current gate tube (CGT), and constant current section (CUS). In combination, these three circuits constitute a decoder section. The combination of three or more of these decoder sections forms a binary decoder. The most important significant model-distinguishing features are the number of decoder sections employed and the type of ladder network (single or complementary) used. Differences of lesser importance involve the variation in component values.

The operation of the three circuits (LS, CGT, and CUS) common to the binary decoders is presented in paragraph 3.7.2. The operation of these circuits in a typical binary decoder is described in paragraph 3.7.3. The model B binary decoder was selected for this purpose. Binary decoders, models A, C, D, and F are then discussed in terms of their model-distinguishing features.

3.7.2 Circuits Common to Binary Decoders

3.7.2.1 Ladder Section

3.7.2.1.1 Definition and Description

The ladder section (LS) is a part of a ladder network in a binary decoder. Figure 3–13 is the logic block symbol for the LS. A ladder network is made up of three

Figure 3–13. Ladder Section, Logic Block Symbol

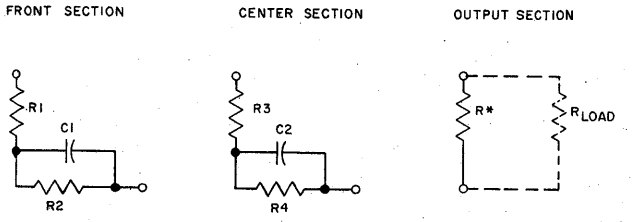


Figure 3–14. Binary Decoders, Ladder Sections, Schematic Diagram

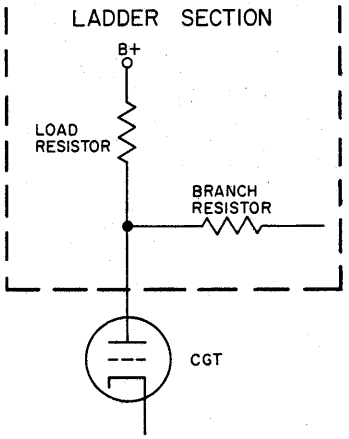


Figure 3–15. Ladder Section Resistors, Schematic Diagram

LS types: a front section, an output section, and one or more center sections. See figure 3–14.

3.7.2.1.2 Principles of Operation

The front and center LS's consist of a load resistor and a branch resistor (fig. 3–15); the output section contains only a load resistor. The value of this resistor is such that the equivalent resistance of the load in parallel with this resistor is equal to the load resistor (R1 in fig. 3–14) of the front LS. Capacitors C1 and C2 (fig. 3–14) bypass the branch resistors to speed up LS response. Speed-up capacitors are used only in model B, C, and D decoders.

The LS function is best described in relation to ladder network operation. Figure 3–16 illustrates the three types of LS's combined to form a ladder network. The current division performed by each LS is shown in B, C, and D. Each LS is associated with a current gate tube (CGT), which functions as a switch, and a constant current source (CUS). The CGT consists of a pair of triodes which channel CUS current into one of two paths (see A of fig. 3–16). For models B, C, and D, the two paths are either one of two LS's in complementary ladder networks; for models A and F, which employ only a single ladder network, current is fed to an LS or directly to B+.

For the purpose of this discussion, the constant current is assumed to be 3I for all CUS's and the control inputs to the CGT's are such that this current is channeled into the depicted ladder network. First, consider the output section. A current of $3I_2$ is passed by the switch tube to the output LS of the ladder network (D of fig. 3–16). The equivalent load resistance (solid line) of the output section is R (the parallel combination of R_{output} and R_{load}). The current ($3I_2$) applied to this LS is confronted by two resistive paths: the equivalent load resistance (R) and the equivalent branch resistance ($2R$) presented to the output section by the front and center sections.

Note

The equivalent branch resistance of the output section is determined in the following manner (see A of fig. 3–16). The equivalent resistance presented to the center section by the load and branch resistors of the front section is equal to $2R$. This resistance in parallel with the load resistor ($2R$) of the center section is equal to R. This resistance in series with branch resistor (R) of the center section presents an equivalent branch resistance of $2R$ to the output section (illustrated in D of fig. 3–16 with a broken line). Hence, CGT current entering the output LS is confronted by two resistive paths equal to $2R$ and R.

The current in the output section divides inversely through these resistances ($2I_2$ through equivalent load resistance R and I_2 through equivalent branch resistance $2R$), producing a voltage drop of $2I_2R$ across the output LS load resistor.

Current entering the center LS is confronted by three resistive paths, each equal to $2R$. (The resistances presented to the center section by the front and output sections are depicted by broken lines on C of fig. 3–16.) Hence, the current divides equally into thirds; I_1 flows through the center section load resistor and into each branch (C of fig. 3–16).

The front LS is similar in operation to the output section. The resistance presented to this LS by the center and output sections is shown by a broken line in B of figure 3–16.

The LS's shown in figure 3–16 are representative of all LS's employed in binary decoders. Therefore, current entering a center section always divides into three equal parts. Current entering a front or output section always divides into two parts in the ratio of 2:1 (two parts into the load resistor and one part into the branch resistor). It is now possible to discuss the weighting function of a ladder network.

The amplitude of the output voltage of a ladder network (B+ less the voltage developed across the load resistor of the output section) is a function of each LS in the network to which a constant current is fed. In figure 3–16,B, a curent of $3I_0$ fed to the front section is divided by the ladder network to produce a branch current of I_0. This branch current enters the center LS (fig. 3–16,C) and is halved to provide a branch current of $1/2I_0$. This branch current, in turn, flows through resistor R of the output LS to produce a voltage drop of $1/2I_0R$. The current entering the center section ($3I_1$) is divided by three, producing branch currents of I_1. This current enters the output section (fig. 3–16,D) and produces a voltage drop across R equal to I_{1R}. The current entering the output section ($3I_2$) is divided in the ratio of 2:1 to provide a load curent of $2I_2$ which, in turn, develops a voltage drop of $2I_2R$ across the load resistance. Thus, a current $3I_2$ entering the output section of a 3-section ladder network causes the network output voltage to fall by $2I_2R$. A current $3I_1$ entering at the center section causes the network output voltage to fall by I_1R. A current $3I_0R$ entering at the front section causes the network output voltage to fall by $1/2I_0R$.

Table 3–7 lists the individual LS's and their contribution to the ladder network output (entries 1, 2, and 3 in columns A, B, and C). The remaining entries (4 through 8) list each possible combination of conducting LS's and the resultant contributions to the ladder network output. Column D lists the total current in terms of IR where $I = I_0 = I_1 = I_2$. By definition, the output

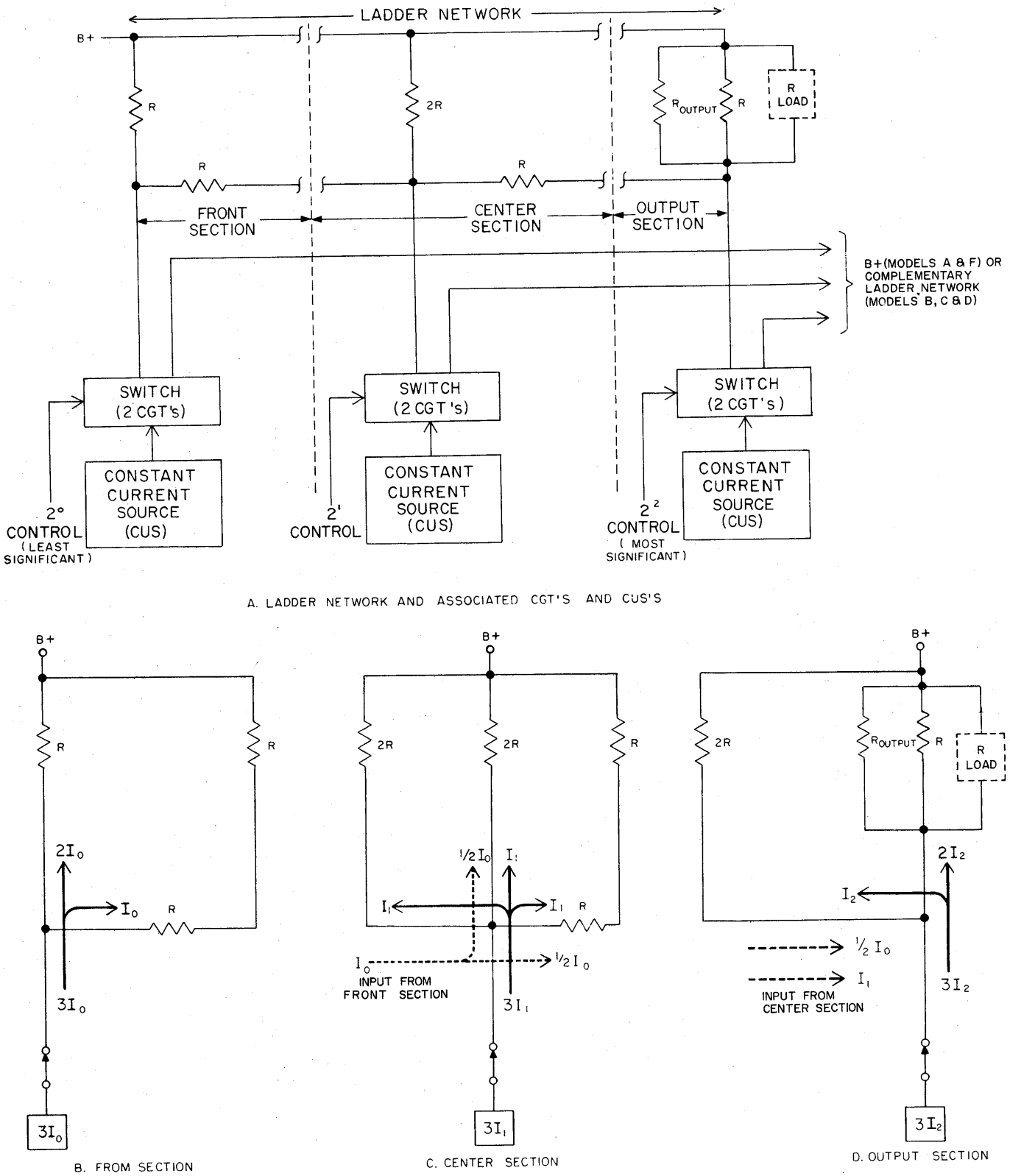


Figure 3–16. Principles of Decoder Operations

TABLE 3–7. LADDER NETWORK INPUTS AND OUTPUTS

A	B	C	D	E
ENTRY	CURRENT FED SECTION	RESULTANT FALLS IN OUTPUT VOLTAGE	RESULTANT TOTAL	RESULTANT CONVERTED $IR = \frac{E_o}{4}$
1	Front	$1/2I_oR$	$1/2IR$	$1/8E_o$
2	Center	I_1R	IR	$1/4E_o$
3	Output	$2I_2R$	$2IR$	$1/2E_o$
4	Front and center	$1/2I_oR + I_1R$	$\frac{3}{2}IR$	$3/8E_o$
5	Front and output	$1/2I_oR + 2I_2R$	$\frac{5}{2}IR$	$5/8E_o$
6	Center and output	$I_1R + 2I_2R$	$3IR$	$3/4E_o$
7	All sections	$1/2I_oR + I_1R + 2I_2R$	$\frac{7}{2}IR$	$7/8E_o$
8	No sections	0	0	0

voltage $E_o = 8\ (1/2\ IR)$, where $1/2I$ is the smallest possible increment of current change through R, capable of increasing through a maximum of eight such discrete steps. Reducing this equation to its simplest form, $E_o = 4IR$, column D, by substitution, becomes column E. The fall in the output voltage (E_o) is thus divisible into eight voltages (o through $7/8E_o$) which are a function of the point of entry of three equal currents in eight combinations (the output voltage is a function of the LS or LS's to which equal currents are channeled).

Current fed only to the output section (table 3–7, column E, entry 3) produces the greater contribution by an LS to a change in the output voltage. It is for this reason that the output section is designated the most significant section in a ladder network. Current fed only to the front section (entry 1, column E) produces the smallest contribution by an LS to a change in the output voltage and therefore is referred to as the least significant section in a ladder network. The center section contribution falls between these extremes and is termed an intermediate section. If the ladder network consists of a number of center sections, the intermediate sections then attain a significance that corresponds to their positions between the most significant and least significant sections.

Significance is indicated in terms of controls on logic diagrams, and these controls indicate the inputs to decoders. These controls are illustrated in figure 3–16 as input designations (2^0, 2^1, *and* 2^2) to the CGT's. The significance of the input is indicated by the exponent. The controls have two states, up and down. When a control is up, its CGT feeds the associated LS from its CUS. When a control is down, its CGT diverts the CUS output to either B+ (models A and F) or to a complementary ladder network (models B, C, and D).

The eight possible combinations of up and down control conditions for the ladder network illustrated in figure 3–16, with the binary address they satisfy, are presented in table 3–8. This table also includes the resultant ladder network output voltages. The table illustrates the digital-to-analog conversion function of a ladder network when employed in a decoder.

3.7.2.2 Current Gate Tube

3.7.2.2.1 Definition and Description

The current gate tube (CGT) is a circuit element of binary decoders. The CGT employs a triode section of a dual triode. The two sections of the triode (two CGT's) form a unit that functions as a switch. Such a unit diverts current from an LS in one ladder network to an LS in a second or complementary ladder network or from an LS in a ladder network to B+ (single network). Figure 3–17 is the logic block symbol for the CGT.

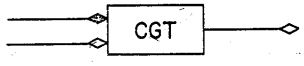


Figure 3–17. Current Gate Tube, Logic Block Symbol

3.7.2.2.2 Principles of Operation

Figure 3–18 is the schematic diagram of the CGT unit in its two applications as a switch in a complementary and in a single ladder network configuration. The single ladder network operation (switching from LS to B+) is illustrated in parts A, B, and C of figure 3–18; complementary network operation (switching from one LS to another LS) is shown in parts D, E, and F.

TABLE 3–8. LADDER NETWORK ANALOG OUTPUT AS A FUNCTION OF DIGITAL INPUT (BINARY ADDRESS)

BINARY ADDRESS	CONTROL	CONTROL CONDITION	FALL IN OUTPUT VOLTAGE
0	2^2	Down	
0	2^1	Down	*0*
0	2^0	Down	
0	2^2	Down	
0	2^1	Down	$1/8E_o$
1	2^0	Up	
0	2^2	Down	
1	2^1	Up	$2/8E_o$
0	2^0	Down	
0	2^2	Down	
1	2^1	Up	$3/8E_o$
1	2^0	Up	
1	2^2	Up	
0	2^1	Down	$4/8E_o$
0	2^0	Down	
1	2^2	Up	
0	2^1	Down	$5/8E_o$
1	2^0	Up	
1	2^2	Up	
1	2^1	Up	$6/8E_o$
0	2^0	Down	
1	2^2	Up	
1	2^1	Up	$7/8E_o$
1	2^0	Up	

Single network operation is employed in the models A and F binary decoders. As shown in figure 3–18,C, the CGT switch unit has two input grids, a common cathode, and two output plate circuits. One plate is connected to an LS; the other plate is returned to B+. One input grid receives the control levels (+10V or −30V); the other grid is connected to a −10V bias supply. The common cathode is returned to a constant current source which consists of either a triode and associated resistors or resistors only.

When an up control voltage (+10V) is applied to the grid of V1B, the common cathode of V1A and V1B rises to +10V. V1A is cut off (grid is 20V negative with respect to cathode) and V1B conducts. As a result, no current flows into the LS. Conversely, with a down control (−30V) applied to V1B, the common cathode falls toward −30V. However, as the common cathode approaches −10V, V1A conducts. The common cathode is caught at −10V and V1B is cut off (grid is 20V negative with respect to the cathode). Current is now diverted into the LS. To summarize, in a single network operation, −30V applied to the CGT input causes current to flow into the ladder network, producing a voltage drop in the output (fig. 3–18,A); +10V applied to the CGT input causes current to flow directly to B+ (fig. 3–18,B).

Complementary network operation is employed in models B, C, and D binary decoders. As illustrated in figure 3–18,F, two ladder networks, an upper and lower, are employed, and the common cathode is always returned to a constant current source. With input A at +10V and input B at −30V, the common cathode is at +10V; V1A conducts and V1B is cut off. As a result, current from the constant current source is channeled through V1A into the upper ladder network; no current enters the lower ladder network. With input A at −30V and input B at +10V, the common cathode is at +10V; V1B conducts and V1A is cut off. Current from the constant current source is now diverted, through V1B, into the lower ladder network. To summarize, with A at +10V (fig. 3–18,D), current flows into the upper ladder network, causing the upper output terminal to fall in voltage from B+. With input A at −30V (fig. 3–18,E), current flows in the lower ladder network, causing the lower output terminal to fall in voltage from B+. Whenever an up control is applied to one CGT, a down control is applied to the complementary CGT.

The magnitude of the fall in output voltage is the same regardless of the ladder network (upper or lower) to which the current is fed. However, the polarity of the fall in output voltage is a function of the ladder network to which the current is fed. See figure 3–18,D and E. The output of the LS to which current is fed is more negative than its complementary LS which is nonconductive.

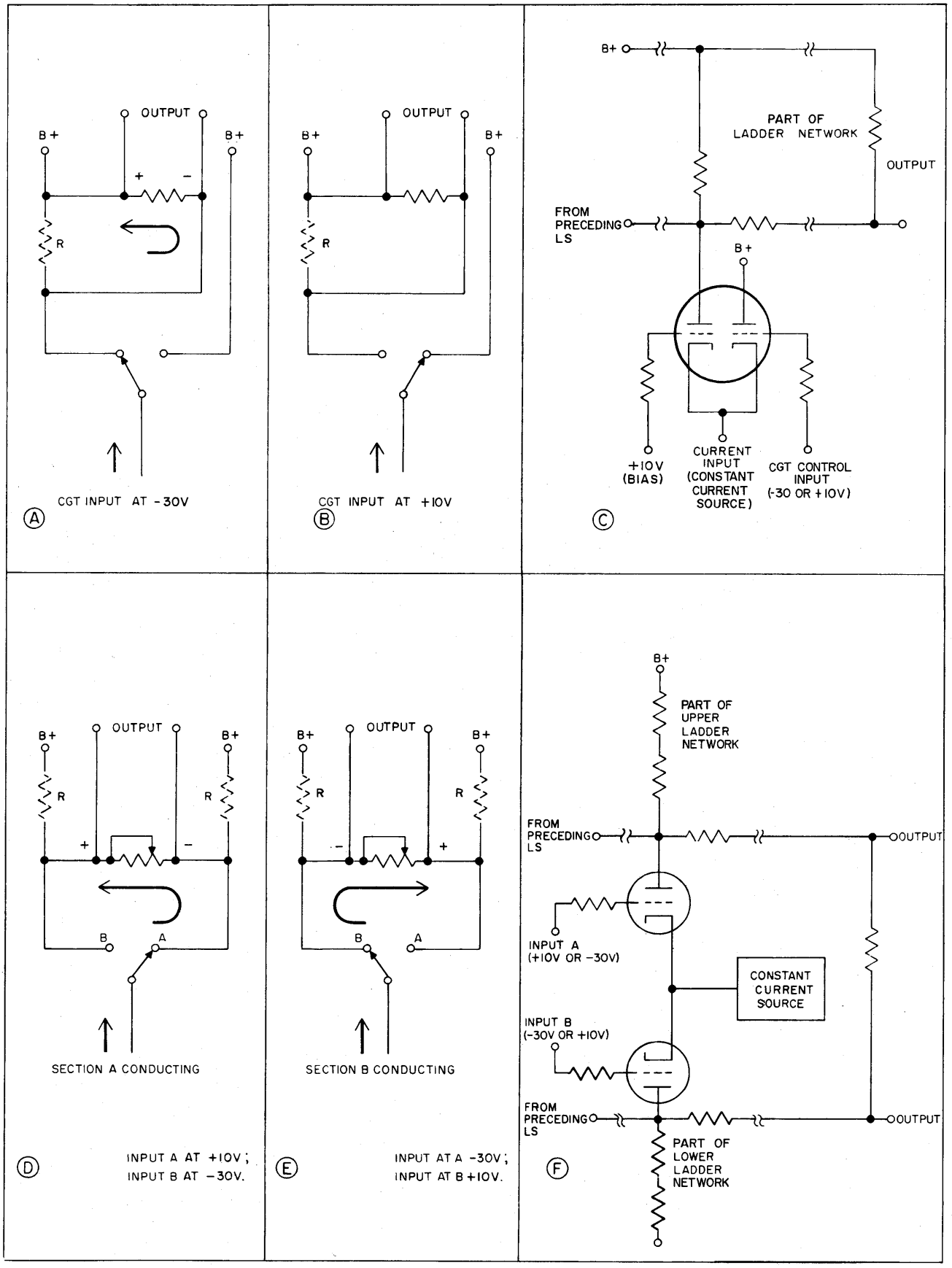


Figure 3-18. Current Gate Tube, Switching Schemes and Schematic Diagrams

3.7.2.3 Constant Current Source

3.7.2.3.1 Definition and Description

The constant current source (CUS) is a circuit element of binary decoders. The CUS is a source of constant current which is essential to the accuracy of the weighting function performed by the ladder network. The CUS consists of either a triode and an associated resistive network or resistors only. Where precise ladder current control is required (four most significant decoder sections of models A and F and all the decoder sections of the other models), the CUS employing a triode is used. Where current control is less important, the CUS containing only resistors is used. Figure 3–19 is the logic block symbol for the CUS.

3.7.2.3.2 Principles of Operation

Figure 3–20 is the schematic diagram for the CUS employing a triode; the triode is one section of a dual triode. The grid and cathode are returned to regulated reference voltages which determine the operating point of the triode. These regulated reference voltages, in conjunction with the degeneration introduced by the unbypassed cathode resistors, provide a constant current source for the associated LS. The variable cathode resistor (R2) included in the cathode circuit enables the precise adjustment of current through the CUS to compensate for CGT, LS and CUS variations. Resistor R1 in the grid circuit is employed as a parasitic suppressor.

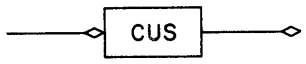


Figure 3–19. Constant Current Source, Logic Block Symbol

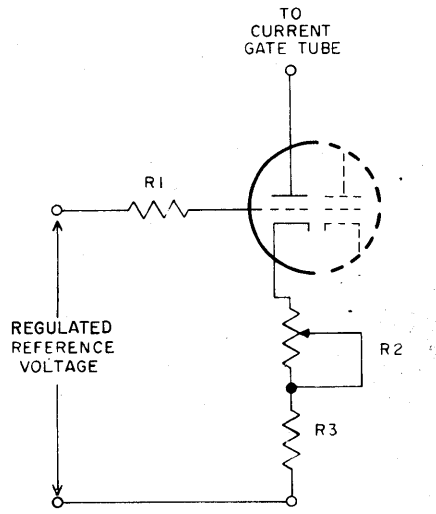


Figure 3–20. Constant Current Source, Schematic Diagram

3.7.3 Binary Decoder, Model B

3.7.3.1 Definition and Description

The model B binary decoder (BBD) employed in the Display System converts binary levels into analog levels that are used as character selection voltages for the SD CRT and digital display (DD) CRT. These analog levels are the deflection voltages which aim the electron beams at a character in the CRT character matrix. The logic block symbol for the BBD is shown in figure 3–21.

The BBD includes two decoders, one for the X axis and the other for the Y axis. Each decoder consists of three decoder sections employing complementary networks to produce character selection voltages. The inputs are fed from the X and Y selection registers. The output of each decoder is applied to an analog line driver.

3.7.3.2 Principles of Operation

Figure 3–22 is the schematic diagram for the X-axis portion of the BBD. Table 3–9 lists the associated detail parts and their functions. The Y-axis portion of the BBD differs from the X-axis portion in only one respect: fixed cathode resistor R15 of the constant current tube (V11) in the most significant decoder section is a variable resistor in the Y-axis decoder. System alignment is performed on the basis of X-axis decoder operation and the Y-axis decoder is then adjusted in the most significant stage with this variable resistor. Refer to T.O. 252, Schematics for Display System, for the binary controls (logic inputs) associated with the input terminals for the decoder.

The outputs of a flip-flop feed the $+X$ and $-X$ half of each decoder section. This results in two states of operation for each decoder section: $+X = 1$ and $-X = 0$ or $+X = 0$ and $-X = 1$. The contribution of each LS to the output voltage was discussed in paragraph 3.7.2.1 (front section: $1/8E_o$; center section: $2/8E_o$; output section: $4/8E_o$). In combination, the contribution of each LS is such that the decoder develops eight different outputs (four different amplitudes of opposite polarities). The manner in which these outputs are developed is illustrated in table 3–10. The input terminals listed in the table are keyed to figure 3–22; the eight possible binary controls applied to these terminals are also provided in this table. The voltage appearing at the output terminals of both upper and lower ladder networks for the eight different binary controls is listed in the column headed Ladder Network Output. The decoder output voltage developed across potentiometer R24 (voltage differential between terminals $+X$ and $-X$) is listed in the last column. Assume that the binary controls fed to the decoder are those listed in the third entry of the table. Decoder inputs *2*, *1'*, and *3'* are at $+10V$ and inputs *1*, *3*, and *2'* are at $-30V$. The output at the $+X$ terminal falls $2/8E_o$ and equals $250V - 2/8E_o$. The out-

put at the $-X$ terminal falls $1/8E_o + 4/8E_o$ and equals $250V - 5/8E_o$. Subtracting one from the other:

$$250V - 2/8E_o - (250V - 5/8E_o) = +3/8E_o$$

Thus, the output voltage developed across potentiometer R24 is $3/8E_o$. Since the greatest fall on potential occurs in the lower ladder network, terminal $+X$ is more positive than terminal $-X$. A similar analysis can be employed for the other binary controls listed in table 3–10.

The Y-axis decoder operation is identical with X-axis decoder operation and therefore produces any of eight different voltage outputs (four different amplitudes of opposite polarities). The combined outputs of both X- and Y-axis decoders permit the selection of any one of 64 locations on the 8×8 character-forming matrix.

Operating voltages are supplied to CUS's V10A, V10B, and V11 by the voltage regulator consisting of

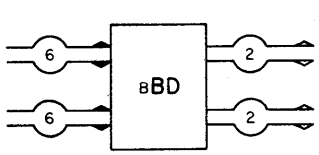
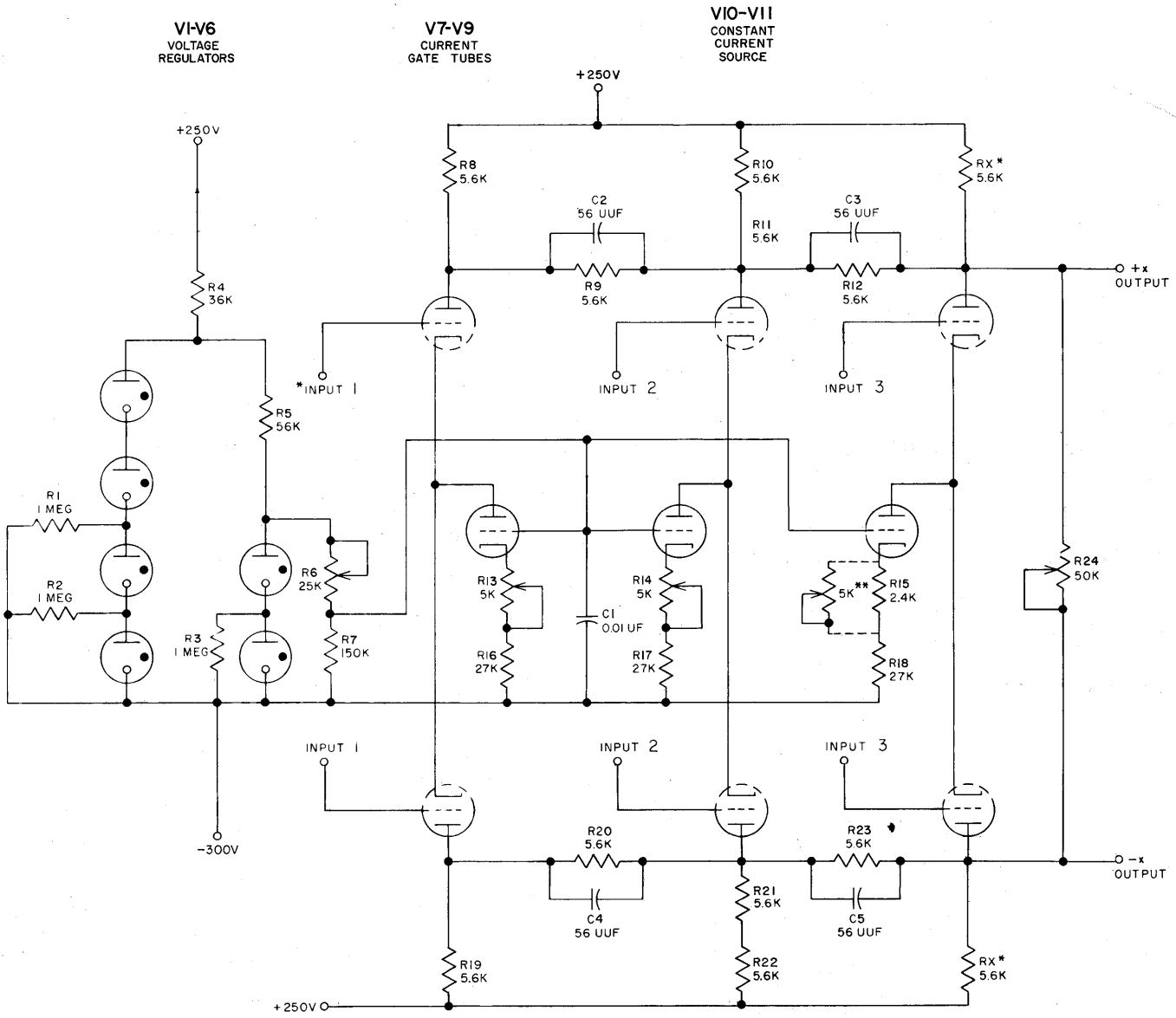


Figure 3–21. Binary Decoder, Model B, Logic Block Symbol



NOTES:
*Rx CONSISTS OF THE INPUT IMPEDANCE OF THE LOAD AND THAT TERMINATING RESISTOR CONNECTED IN PARALLEL WHICH MAKES Rx EQUAL TO 5.6K.
** y-AXIS CHARACTER SELECTION DECODER IDENTICAL TO THIS CIRCUIT EXCEPT FIXED RESISTOR R15 IS REPLACED BY A 5K POTENTIOMETER
*** PARASITIC SUPPRESSORS AND DECOUPLING NETWORKS HAVE BEEN OMITTED

Figure 3–22. Binary Decoder, Model B, X-Axis Portion, Schematic Diagram

TABLE 3–9. BINARY DECODER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1	Grid bypass for V10 and V11	R13, R14	Current adjust for V10A and V10B
C2-C5	Speedup capacitors	R15	Fixed cathode resistor for V11 (X-axis decoder); current adjust for V11 (Y-axis decoder)
R1, R2, R3	Voltage distribution resistors		
R4, R5	Voltage-dropping resistors	R16, R17, R18	Cathode resistors
R6	Bias adjust for V10 and V11	R19	Load resistor, part of ladder section (with R20)
R7	Bias voltage divider (with R6)	R20	Branch resistor, part of ladder section (with R19)
R8	Load resistor, part of ladder section (with R9)	R21	Load resistor, part of ladder section (with R22 and R23)
R9	Branch resistor, part of ladder section (with R8)	R22	Load resistor, part of ladder section (with R21 and R23)
R10	Load resistor, part of ladder section (with R11 and R12)	R23	Branch resistor, part of ladder section (with R21 and R22)
R11	Load resistor, part of ladder section (with R10 and R12)	R24	Output voltage gain adjust
R12	Branch resistor, part of ladder section (with R10 and R11)		

TABLE 3–10. BINARY DECODER, MODEL B, OUTPUT AS A FUNCTION OF BINARY CONTROLS

BINARY CONTROLS*						LADDER NETWORK OUTPUT		DECODER OUTPUT (VOLTAGE ACROSS R24)
Input Terminals Upper Ladder Network (+X)			Input Terminals Lower Ladder Network (−X)			+X	−X	
1	2	3	1′	2′	3′			
0	0	0	1	1	1	$250V\text{-}OE_o$	$250V\text{-}7/8E_o$	$+7/8E_o$
1	0	0	0	1	1	$250V\text{-}1/8E_o$	$250V\text{-}6/8E_o$	$+5/8E_o$
0	1	0	1	0	1	$250V\text{-}2/8E_o$	$250V\text{-}5/8E_o$	$+3/8E_o$
1	1	0	0	0	1	$250V\text{-}3/8E_o$	$250V\text{-}4/8E_o$	$+1/8E_o$
0	0	1	1	1	0	$250V\text{-}4/8E_o$	$250V\text{-}3/8E_o$	$-1/8E_o$
1	0	1	0	1	0	$250V\text{-}5/8E_o$	$250V\text{-}2/8E_o$	$-3/8E_o$
0	1	1	1	0	0	$250V\text{-}6/8E_o$	$250V\text{-}1/8E_o$	$-5/8E_o$
1	1	1	0	0	0	$250V\text{-}7/8E_o$	$250V\text{-}OE_o$	$-7/8E_o$

**Inputs 1 and 1′, least significant digit*
Inputs 2 and 2′, intermediate digit
Inputs 2 and 3′, most significant digit

V1 through V6 and the associated circuit element. Voltage regulators V1 through V4 maintain the voltage across resistor R5 and regulators V5 and V6 at a constant level, independent of variations in the +250V supply. Resistors R5, R6, and R7 form a voltage divider to provide the required grid bias for the CUS's. Potentiometer R6 is used to adjust for this proper bias level. Regulators V5 and V6 maintain the voltage across R6 and R7 constant, compensating for variations in the −300V supply. The constant voltage difference between the grid of each CUS and the cathode return is developed across R7. A variable cathode resistor in the cathode circuit of each CUS permits the precise adjustment of grid bias and, hence, current supplied by each CUS.

3.7.4 Binary Decoder, Model C

3.7.4.1 Definition and Description

The model C binary decoder (cBD), employed in the Display System, converts binary levels into analog levels that are used as character-positioning voltages for the DD CRT. These analog levels are the deflection voltages which position successively selected characters in a DD message on the face of the DD CRT. The logic block symbol for the cBD is shown in table 3–11.

The cBD consists of two decoders, one for the X axis and the other for the Y axis. Each decoder consists of four decoder sections employing complementary networks to produce character-positioning voltages. The inputs are supplied by character position counters; outputs are applied to the DD character deflection plates through analog line drivers.

3.7.4.2 Principles of Operation

The cBD is essentially the same as the model B binary decoder discussed in paragraph 3.7.3, with one major difference; an additional decoder section is added. As a result, the weighted output of the least significant decoder section is $1/16E_o$ instead of $1/8E_o$. The maximum number of input binary controls with four binary digits is 16. Therefore, the output of each decoder (X- and Y-axis) will be any one of 16 different voltages, eight different amplitudes of opposite polarities. In the Y-axis decoder, these 16 levels are associated with positioning the 16 horizontal rows of characters in a DD message; in the X-axis decoder, these levels are associated with the positioning of characters within a horizontal row of characters. Refer to T.O. 252, Schematics For Display System, for the binary controls associated with the cBD.

3.7.5 Binary Decoder, Model D

3.7.5.1 Definition and Description

The model D binary decoder (dBD), employed in the Display System, converts binary levels into equivalent analog levels that are used as character compensation and positioning voltages for the SD CRT. In effect, the outputs of the dBD perform three functions. They compensate for the electron beam deflection caused by the character selection voltages, position the A character with respect to the E character in a track data (TD) message, and successively position each selected character with an SD message. These outputs are a function of the binary controls (refer to T.O. 252, Schematics for Display System) applied to the dBD. The logic block symbol is shown in table 3–11.

The dBD consists of two identical decoders; one for the X axis and the other for the Y axis. Each decoder consists of four decoder sections employing complementary ladder networks. The number of current gate tubes (CGT's) differs for each decoder section. The least significant decoder section employs three pairs of CGT's. The next two significant stages (center sections) contain two pairs of CGT's. The most significant section employs one pair of CGT's. Doubling and tripling the number of CGT's is necessitated by the threefold function of the decoder output voltage. The inputs to the decoder, because of its multiple function, are supplied by several sources. The outputs are fed through analog line drivers to the character compensation and positioning plates of the SD CRT.

3.7.5.2 Principles of Operation

The operation of the dBD is essentially the same as the model B binary decoder discussed in paragraph 3.7.3, with the exception of the added decoder section. The effect of this added section on the weighted output is identical with that of the cBD (par. 3.7.4), which also employs four decoder sections. As in the case of all binary decoders, the outputs are a function of the binary controls applied to the decoder. Once these controls are known, an analysis similar to that used for the bBD (refer to 3.7.3) can be used to determine the equivalent output voltages.

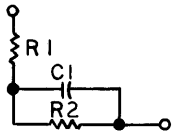
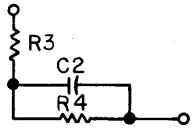
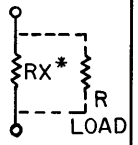
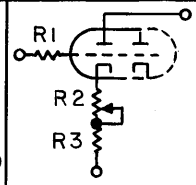
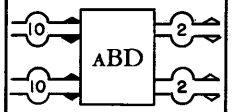
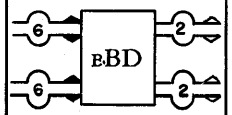
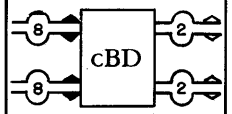
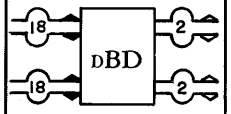
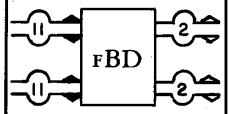
3.7.6 Binary Decoder, Model A

3.7.6.1 Definition and Description

The model A binary decoder (aBD), employed in the Display System, converts binary levels into equivalent analog levels that are used as message-positioning voltages for the SD CRT. These analog levels are used to position the SD message format on the face of the CRT. The logic block symbol for the aBD is shown in table 3–11.

The aBD contains two decoders; one for the X axis and one for the Y axis. Each decoder consists of 10 decoder sections employing single ladder networks to produce the required analog voltages. The decoder inputs are derived from the word storage portion of the SD generator element (SDGE). The decoder outputs are fed through associated deflection amplifiers and drivers to the windings of the SD CRT deflection yoke as analog currents.

TABLE 3–11. BINARY DECODER MODEL – DISTINGUISHING FEATURES

MODEL	LOGIC BLOCK SYMBOL	FUNCTION	NUMBER OF DECODER SECTIONS	COMPONENT VALUES									
				LADDER SECTIONS							CONSTANT CURRENT SOURCES**		
				FRONT 			CENTER 			OUTPUT 			
				R1	R2	C1	R3	R4	C2	RX*	R1	R2	R3
A		Provides analog levels for SD CRT message positioning	10	15K	15K	—	30K	15K	—	15K	47	1K	56K
				Single Ladder Network									
B		Provides analog levels for SD CRT and DD CRT character positioning	3	5.6K	5.6K	56μμ	11.2K	5.6K	56μμ	5.6K	100	5K	27K
				Complementary Ladder Network									
C		Provides analog levels for DD CRT character positioning	4	5.6K	5.6K	56μμ	11.2K	5.6K	56μμ	5.6K	100	5K	27K
				Complementary Ladder Network									
D		Provides analog levels for SD CRT character positioning and compensation	4	5.6K	5.6K	56μμ	11.2K	5.6K	56μμ	5.6K	39	5K	27K
				Complementary Ladder Network									
F		Provides analog levels for LRI monitor range information and azimuth sine and cosine approximation	11	15K	15K	—	30K	15K	—	15K	47	1K	56K
				Complementary Ladder Network									

**RX consists of the input impedance of the load and that terminating resistor connected in parallel which makes RX equal to the value listed.*

***The triode of the constant current source in ABD and FBD is used only in the four most significant stages. It is replaced with a 56K resistor in the next three significant stages, and R2 is replaced with a 10K pot. The pot is removed in the remaining decoder sections, employing only the two fixed resistors.*

3.7.6.2 Principles of Operation

All ABD decoder sections are identical with the exception of the CUS's (refer to table 3–11). The four most significant stages employ the same type of CUS used in the previously discussed decoders. In the next three significant stages, the CUS triode is replaced with a fixed resistor. The three least significant stages use only two fixed desistors. The relative effect of current through each decoder section on the output voltage permits these circuit variations. Precise adjustment of CUS current is a function of decoder section significance. The most significant decoder section requires a more precise control of LS current because small variations in these currents produce relatively large variations in output voltage.

The output voltage of the decoder, as for all other decoders, is a function of the binary controls applied to the decoder. The inputs to each decoder consist of 10 binary levels (+10 or −30V). The greatest number of combinations possible with 10 binary inputs is 1,024; therefore, the decoder output is any one of 1,024 discrete levels. The effect of the controls on a decoder section employing a single LS was discussed in paragraph 3.7.2.2. A +10V input (binary) inhibits current flow to the associated LS; a −30V input (binary 0) diverts current into the associated LS. When a binary control 0 is applied to the most significant stage (1's applied to the remaining nine stages), the voltage drop at the output of the decoder equals 25V. This voltage, as seen from the output, is halved for each succeeding decoder section when the control bit to the respective stages is 0 (remaining sections contain 1's). This result is illustrated in table 3–12. The output voltage change for any binary number is the sum of the voltage drops for each bit corresponding to a 0. For example, with a binary output of 0000000000, the voltage drop at the output equals 49.954V. This value may be considered to be 50V, representing the maximum voltage drop developed at the decoder output. The number 1111111111 corresponds to 0V (minimum value); the number 1100001111 equals 11.720V. A further examination of table 3–12 will show that the decoder output voltage linearly reflects the binary input.

3.7.7 Binary Decoder, Model F

3.7.7.1 Definition and Description

The model F binary decoder (FBD) is used in the LRI monitor (Input System). Three such decoders are used to convert binary levels representing LRI information and approximation of the sine and cosine functions of the azimuth into corresponding analog levels. These analog levels are then converted to two analog voltages which correspond to the X and Y co-ordinates of the LRI target and are used to display the target on an LRI monitor. The logic block symbol of the FBD is shown in table 3–11.

The three decoders are identical, each consisting of 11 decoder sections employing single ladder networks. The inputs to the sine and cosine binary decoders are supplied by the sine and cosine registers in an 11-bit binary code. Information to the third decoder represents target range and is supplied by the range storage register in a 10-bit binary code. The sine and cosine analog levels are further processed by shaping networks into almost pure sine and cosine functions of azimuth. The sine and range analog levels are then multiplied to provide the CRT of the LRI monitor with X-positioning voltages; the cosine and range analog levels are multiplied to provide the Y-positioning voltages.

3.7.7.2 Principles of Operation

The FBD is essentially the same as the model A binary decoder discussed in paragraph 3.7.6, with one major difference; an additional decoder section is added. As a result, the output of the FBD is any one of 2,048 discrete levels. The sine and cosine decoders employ all 11 sections of the decoder (11-bit binary input code). The input to the range decoder consists of a 10-bit binary code, utilizing only the 10 most significant decoder sections. The least significant stage remains at binary 0. The error introduced into the decoder output by the contribution of this decoder section is within the allowable output tolerance and therefore can be disregarded. In all other respects, the three decoders operate in the same manner as the ABD (refer to 3.7.6).

TABLE 3–12. BINARY DECODER, MODEL A, OUTPUT AS A FUNCTION OF BINARY CONTROL INPUT

DECODER* SECTION	OUTPUT VOLTAGE DROP WHEN BIT IS 0
2^9	25.000
2^8	12.500
2^7	6.250
2^6	3.125
2^5	1.563
2^4	0.782
2^3	0.391
2^2	0.196
2^1	0.098
2^0	0.049

**Exponent designates decoder section significance; i.e., 2^9 is the most significant.*

3.8 BUFFER AMPLIFIER

3.8.1 Definition and Description

The buffer amplifier (BU) is a nonlogic circuit designed to correct both an impedance mismatch and a difference in d-c levels between the binary decoders and the shaping networks and multipliers. The logic block symbol for the BU is shown in figure 3–23.

3.8.2 Principles of Operation

Figure 3–24 is the schematic diagram for the BU. Table 3–13 lists the associated detail parts and their functions. The input signal is fed into a level-shifting network consisting of a resistor network in series with the input level and a reregulated —87V reference. The level shift obtained from this network is applied to the grid of V1A. The grid of V1B is connected through a resistor to a gain-setting network. The difference in levels between the grids of V1A and V1B (differential amplifier) is amplified in V1A. This amplified difference signal is direct-coupled through a resistor to the grid of pentode amplifier V2 where it is amplified considerably due to the high gain of the pentode. The signal is then coupled to the grids of paralleled output triode V3A and V3B.

3.8.3 Circuit Refinements

In tube V2, the suppressor and cathode are tied together and returned through resistor R14 to the connected cathodes of V3A and V3B and through the gain-setting network to the grid of V1B. This means of compensating for the instability of direct-coupling effects is carried still further by supplying regulated voltages to critical points in the circuit. The tied cathodes of the differential amplifier are connected to the regulated —250V supply through cathode resistor R6. The plate of V1A is connected through plate load resistor R5 to a regulated +150V supply. The screen grid of V2 is connected directly to that supply. The plate of tube V1B is tied to a regulated +100V supply. The voltage-dropping network, consisting of resistors R9, R10, and zero-adjust potentiometer R11, is returned to a reregulated —86V supply.

The percentage of output potential that is fed back to the grid of V1B, through resistor R17 and capacitor C3, is determined by the ratio of resistors R3 and R4. These resistors form the gain-setting network.

Triode tube sections V3A and V3B are paralleled, in a cathode follower circuit, to increase the current-handling capacity of the output stage. The buffer amplifier output is taken from the cathodes of this tube. The negative feedback and reference voltage stability contribute to the reliability of the buffer amplifier as a matching device. The level shift effected at the input to the differential amplifier results in a loss of gain which is more than offset by the operational gain of the impedance-converting amplifier.

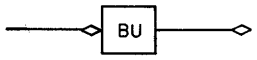


Figure 3–23. Buffer Amplifier, Logic Block Symbol

The values of level-shifting network resistors R1 and R2, and the gain-setting network resistors R3 and R4, depend on whether the buffer amplifiers are used as sine, cosine, or range buffer.

3.9 CAPACITOR-DIODE GATES, MODELS A, B, C, AND E

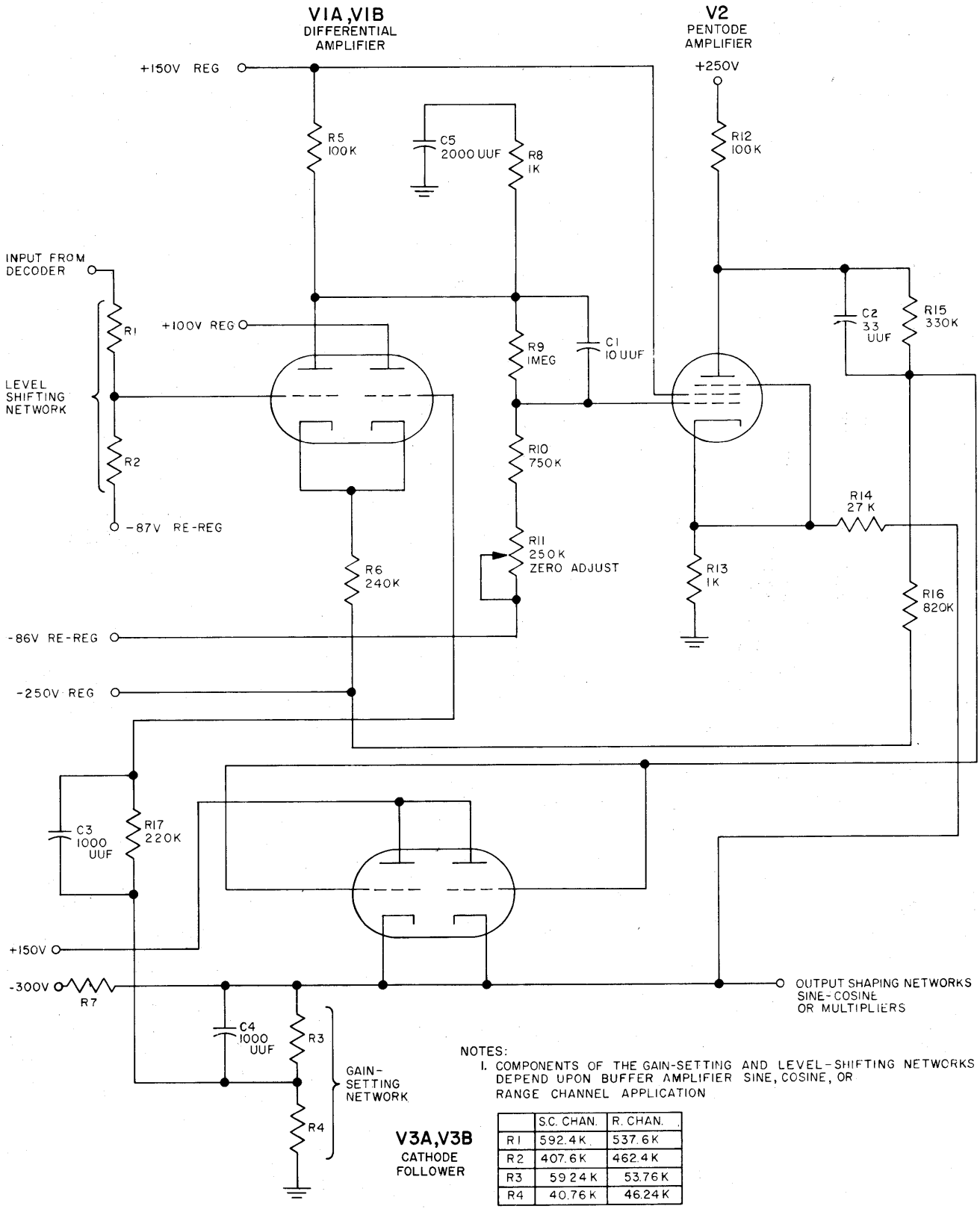
3.9.1 Definition and Description

The capacitor-diode gates (CDG) are logic circuits which pass a standard pulse when conditioned by a +10V standard level. Figure 3–25 shows the logic block symbol for these circuits.

There are four models of the CDG. Three models (A, B, and C) are identical in form. Changes, in value

TABLE 3–13. BUFFER AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Level-shifting network resistors
R3, R4	Part of gain-setting network (with R7 and R17)
R5	Plate load resistor, V1A
R6	Cathode resistor
R7	Part of gain-setting network (with R3, R4, and R17)
R8	Part of damping network (with C5)
R9, R10, R11	Form voltage-dropping network with R11 as zero adjust
R12	Plate load resistor for V2
R13	Cathode resistor for V2
R14	Compensates for instability of d-c effects
R15	D-c coupling between V2 and V3
R16	Feedback resistor from V2 to V1
R17	Grid return for V1B and part of gain-setting network (with R3 and R4)
C1, C2, C3	Rise time compensating capacitors
C4	Compensation capacitor
C5	Part of damping network (with R8)



NOTES:

1. COMPONENTS OF THE GAIN-SETTING AND LEVEL-SHIFTING NETWORKS DEPEND UPON BUFFER AMPLIFIER SINE, COSINE, OR RANGE CHANNEL APPLICATION

	S.C. CHAN.	R. CHAN.
R1	592.4K	537.6K
R2	407.6K	462.4K
R3	59.24K	53.76K
R4	40.76K	46.24K

R 7 = 150K IN RANGE BUFFER CHANNEL
R 7 = 17K IN SINE-COSINE BUFFER CHANNEL

2. ALL SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
3. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

Figure 3-24. Buffer Amplifier, Schematic Diagram

or type, of several detail parts in the circuit account for the differences between the three models. Model E is a combination of a pulse coupler and a CDG.

3.9.2 Principles of Operation

Figure 3–26 shows the schematic diagrams of the four models of the CDG. Table 3–14 lists the associated detail parts and their functions.

Consider the ACDG (fig. 3–26,A). The output terminal of CR1 is returned to +10V in the circuit it feeds. With −30V applied to the D-C IN terminal, CR1 is biased beyond cutoff by 40V. A standard pulse (40V) applied to the PULSE IN terminal raises the plate of CR1 a maximum of 40V to +10V. As a result, no pulse appears at the PULSE OUT terminal. With D-C IN voltage at +10V, the diode anode and cathode are at the same potential. A standard pulse applied to the PULSE IN terminal appears as a standard pulse at the PULSE OUT terminal. Inductor L1 presents a high impedance to the input pulse, ensuring relatively unloaded coupling to the succeeding circuit. Inductor L1 also presents a low d-c impedance for the discharge of C1 and prevents a bias buildup at the anode of CR1.

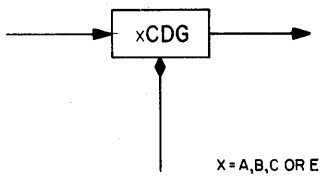


Figure 3–25. Capacitor-Diode Gate, Logic Block Symbol

TABLE 3–14. CAPACITOR-DIODE GATES, MODELS A, B, C, AND E, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	USED ON MODEL	FUNCTION
C1	All	Coupling capacitor
CR1	All	Gating diode
L1	All	Peaking coil
L2	E	Peaking coil
R1	All	Load resistor
R2	E	Damping resistor

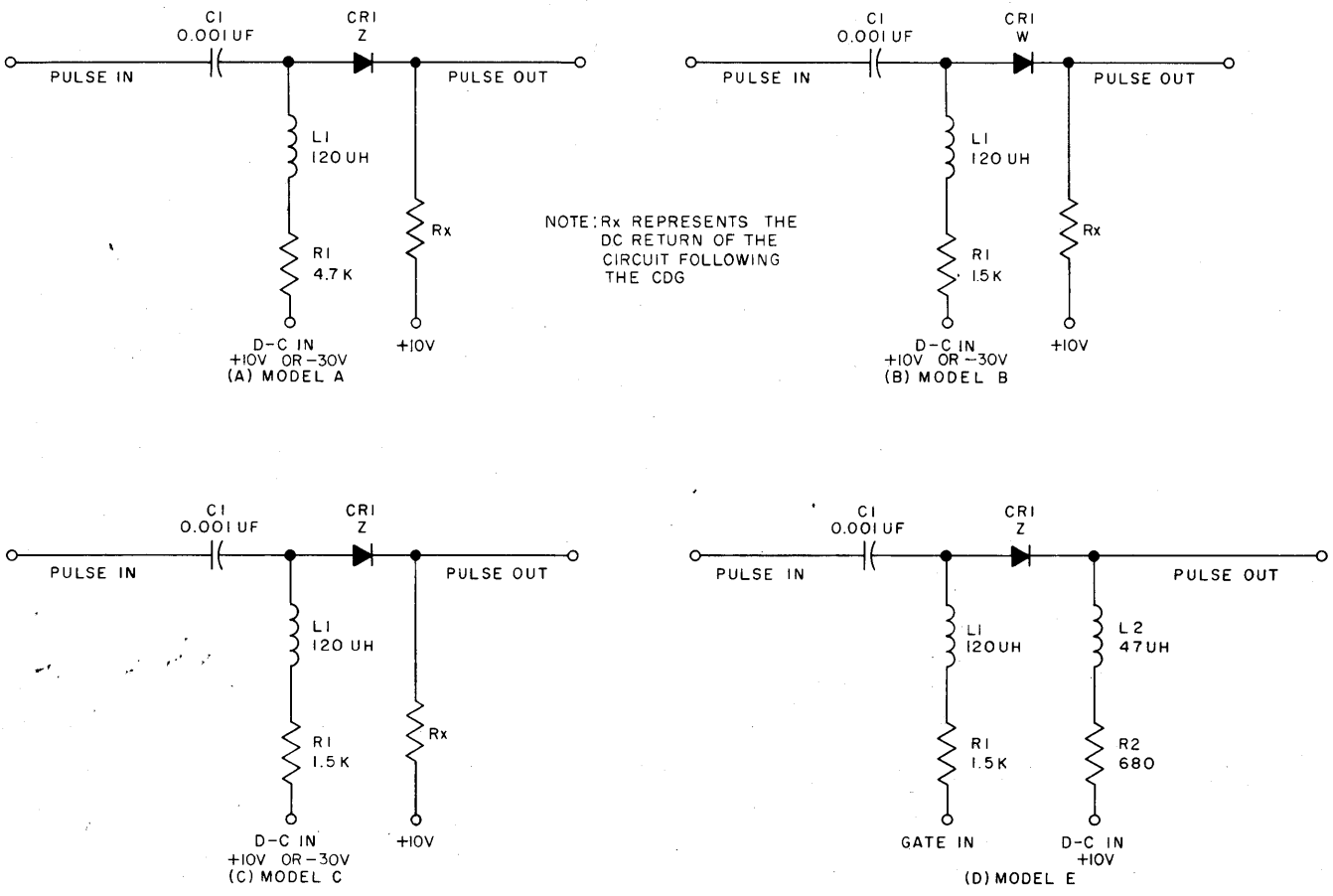


Figure 3–26. Capacitor-Diode Gate, Models A, B, C, and E, Schematic Diagrams

The BCDG and CCDG operate in a similar manner. In model B, the type of diode (CR1) is changed to adapt the model C to specific application requirements. In models B and C, R1 is changed in value to reduce the input impedance (d-c) of the CDG to meet specific application requirements.

The ECDG has a pulse coupler segment which provides the +10V cathode bias voltage for CR1. This arrangement permits pulse gating into circuits lacking a +10V return in their inputs.

3.10 CATHODE FOLLOWER CLAMP, MODEL T

3.10.1 Definition and Description

The model T cathode follower clamp (TCFC) is a nonlogic circuit which provides a steady −12V bias to the tape flip-flop. The logic block symbol for the CFC is shown in figure 3–27.

3.10.2 Principles of Operation

3.10.2.1 Basic Operation

The TCFC is basically a cathode follower with a fixed grid voltage, hence, a fixed output. The circuit operates to readjust itself and maintain the output voltage at the −12V level regardless of the load current. This comes about because of the low output impedance of the cathode follower, which is the result of the feedback inherent in the circuit.

3.10.2.2 Detailed Operation

Figure 3–28 is the schematic diagram of the TCFC. Table 3–15 lists the associated detail parts and their functions.

The grid of V1A is always maintained at a voltage of −15V by the voltage divider composed of R1 and R2. When there is no load attached to the cathode follower, the current through the tube is about 3.2 ma and the output voltage taken from the cathode is −12V. Thus, the net grid bias of the tube is −3V.

When the output is connected to a signal which is more negative than −12V, the crystal diode in the tape flip-flop conducts, and the effective cathode resistance is lowered by the diode conduction. This causes a decrease in grid bias, which causes an increased plate current to flow, thereby restoring the voltage across the cathode resistance to −12V.

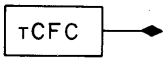


Figure 3–27. Cathode Follower Clamp, Model T, Logic Block Symbol

TABLE 3–15. CATHODE FOLLOWER CLAMP, MODEL T, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Voltage divider
R3	Cathode resistor
C1, C2	Filter capacitors

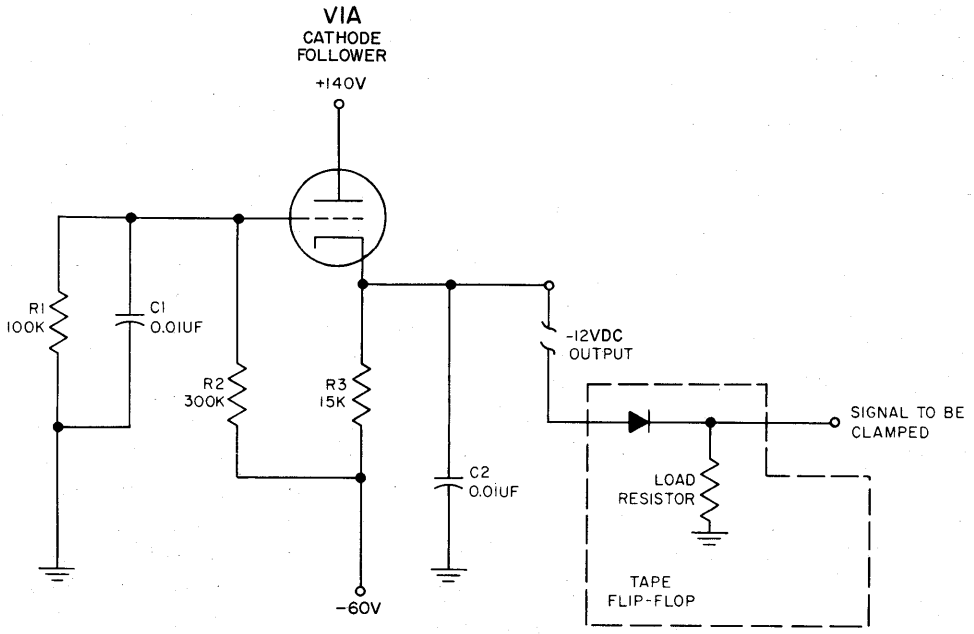


Figure 3–28. Cathode Follower Clamp, Model T, Schematic Diagram

3.11 COMPLEMENT CORE COUNTER

3.11.1 Definition and Description

The complement core counter (CCC) is a logic circuit which performs a count-down function and provides a 1's complement of the count. The logic block symbol for the CCC is shown in figure 3–29.

Two CCC's are employed in the GFI element of the Input System. One is used as a range counter; the other, as an azimuth counter. Range and azimuth increment pulses are received by the counter from the gap-filler radar site. Range increment pulses are counted by the range counter. Azimuth increment pulses are used to clear the range counter and are counted by the azimuth counter. Thus, the range counter indicates the range of the radar sweep inside each azimuth increment or sector, and the azimuth counter indicates the position of the radar scan with respect to radar north. The maximum range count is 64. The maximum azimuth count is 256.

3.11.2 Principles of Operation

3.11.2.1 Basic Operation

The CCC consists of 13 core shifts (CS), refer to figures 3–30 and 3–31, foldout. Each core possesses the ability to store either a 1 or a 0. Refer to paragraph 3–19 for details on basic CS and CS register operation. Cores 1 through 9 form a series-connected closed ring. Bits are read into core 9 from the add-in core, core A, and are transferred from core to core until they are read into the last core in the ring, core 1. Bits are read out of the ring serially through core 1′ which is connected in parallel with core 1. Cores B and C are used in more complex count-down operations.

The cores utilized in the CCC have as many as five windings. Each winding is labelled with the winding's function (fig. 3–31). The functions are listed and explained below:

a. Read-in (or add-in) winding, magnetizes a core to store a 1.

b. Readout winding, permits bit stored in a core to be extracted for use.

c. Drive winding, causes readout to be performed.

d. Reset winding, sets core to predetermined state of storing a 1 or a 0.

e. Feedback winding, returns a core to state prior to readout after readout occurs.

f. Inhibit winding, prevents a read-in of 1 or 0 into a core.

The following pulses are supplied to the CCC. Drive shift pulses are supplied by two ECSD's operated in parallel. The 40V pulse is 3.4 μsec wide. These pulses occur in groups (or bursts) of nine, each pulse occurring 20 μsec after the preceding one. The reset pulses, supplied by a GCSD, are 6.4-μsec positive current pulses.

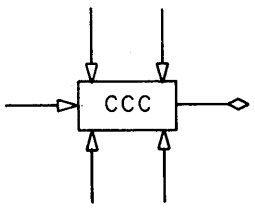


Figure 3–29. Complement Core Counter, Logic Block Symbol

Add-in pulses differ for the two counters. In the range counter, the add-in pulse is supplied by a DCSD and is a 5.9-μsec current pulse. In the azimuth counter, the add-in pulse is the same as the reset pulse.

3.11.2.2 Detailed Operation

The CCC cycle has three phases of operation, which are described in the sequence listed:

a. Counting with no borrowing

b. Counting involving borrowing

c. Clearing the counter to prepare it for a new count

Counting with no borrowing is performed as follows. Assume that the counter has been reset; i.e., cores 1 through 9 and 1′ are set to 1. The state of each core under these circumstances is shown in table 3–16. An add-in pulse is applied to the add-in winding of core A, setting a 1 in the core, as can be seen by the direction of the arrow in figure 3–31. The state of the remaining cores is unchanged. This is shown on the Add One Pulse line in table 3–16. A drive (shift) pulse is then applied to the series-connected drive windings. The drive pulse pulses every core in the counter, transferring the contents of each core to the succeeding core via the read-in and readout windings. It should be noted in figure 3–31 that the output of core A is coupled to the read-in winding of core B and the inhibit winding of core 9. Also, the output of core 1 is coupled to the read-in winding of core 9 and the inhibit winding of core B. All these windings are pulsed simultaneously after the duration of the drive pulse. In both cores 9 and B, the magnetic fields set up by having their read-in and the inhibit windings pulsed simultaneously will oppose and cancel each other. This is indicated by the arrows in figure 3–31. Thus, cores 9 and B will contain 0's after the first shift. (See the Drive (Shift) Pulse 1 line in table 3–16.) The serial output of the counter is obtained by means of a second readout winding in core 2. This second readout winding, with its associated coupling network, transfers the contents of core 2 to core 1′. The contents of core 1′, in turn, are transferred to the read-in winding of the first core in the readout register. The second drive pulse arrives and again transfers the con-

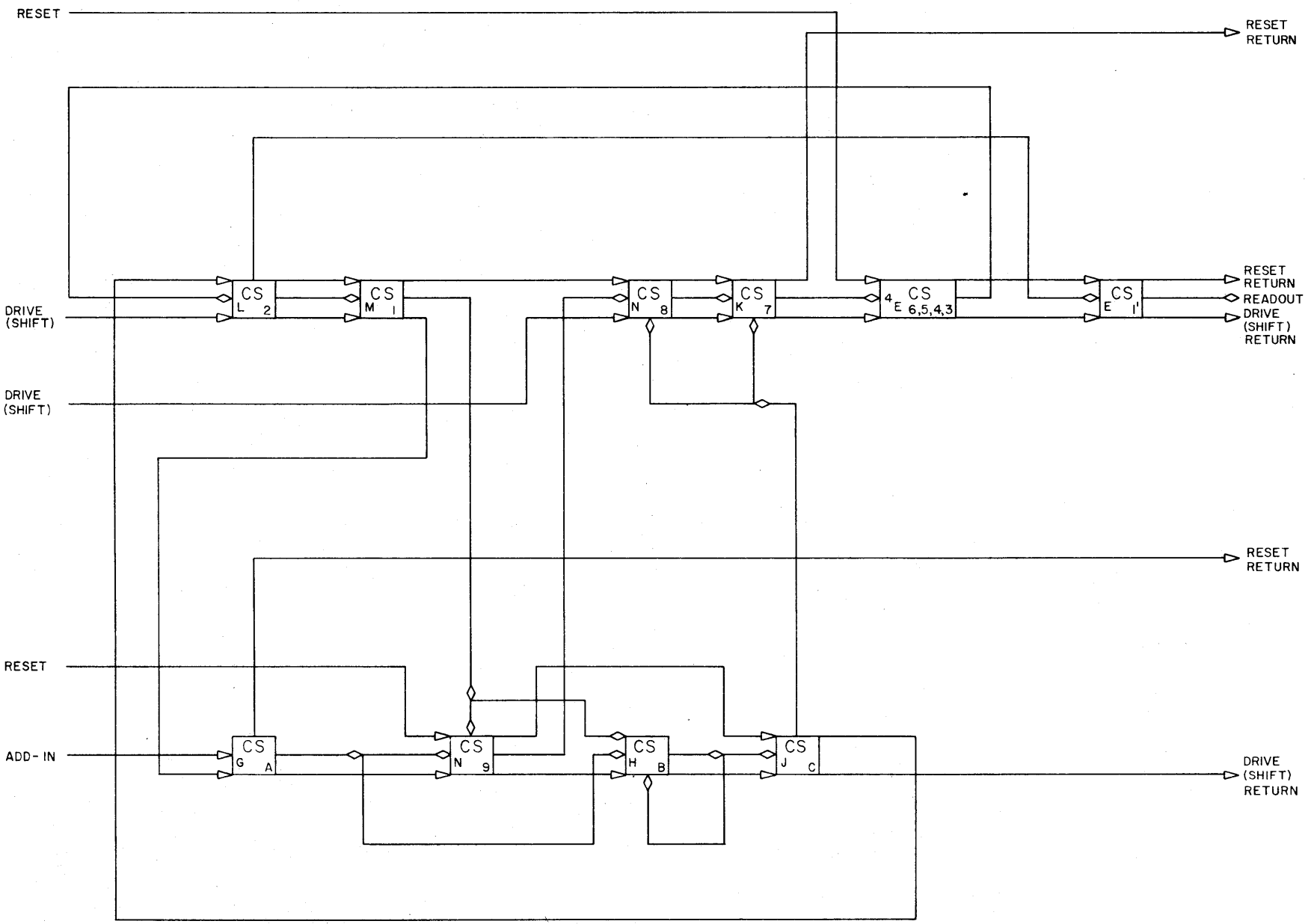


Figure 3–30. Complement Core Counter, Detailed Logic Block Diagram

tents of each core to the succeeding core. After the occurrence of the second drive pulse, no inhibition occurs. Core A having been cleared to 0 during the first shift, neither the read-in winding of core B nor the inhibit winding of core 9 is pulsed. Therefore, core B remains in the 0 state, while core 9 stores the 1 it receives from core 1. This is shown in the Drive (Shift) Pulse 2 line in table 3–16. For each succeeding drive pulse, the counter operates in the same manner as with the application of the second drive pulse. After the ninth (and final) drive pulse, the add-one operation is completed. The counter contains the digital number shown on the Drive (Shift) Pulse 9 line of table 3–16. This number is the 1's complement of the actual count of 1.

The detailed operation of the cores is the same as that of the basic CS operation described in paragraph 3.19. The purpose of CR1, the extra diode in the output circuit of core A, is to prevent the output pulse on capacitor C1 from charging when a 1 is being read out of core 9. Diode CR3 serves a similar function in the output circuit of core 1′. Diode CR2, in the output circuit of core B, prevents a negative charge from building up on capacitor C2 via the feedback winding. The voltage divider circuit in the output circuit of core 1, R29 and R30, provides a slight bias which prevents 1-degeneration from occurring in core B from a 0 readout in core 1 when core B is being set by the feedback winding. (The loss of a 1 because of low read-in current is called a 1-degeneration.)

Counting involving borrowing is performed as follows. After the addition of the first add-in pulse and the subsequent shifting, the counter contained the binary count 111 111 110. Upon the addition of a second add-in pulse, the counter should operate in such a manner as to end (after 9 shifts) with a count of 111 111 101, or the 1's complement of 2 in binary. It can be seen that, in the first step of this operation, subtracting 1 from the least significant digit of 111 111 110 (i.e., 0) will produce a 1 with a borrow of 1 from the next bit. Feeding such borrows back into the ring (cores 1 through 9) at the proper time is the function of cores B and C. A detailed description of the operation of cores B and C is given below.

The second add-in pulse sets core A to 1. It should be noted that cores 1, B, and C contains 0's at this time. (See the Start line of table 3–17.) The first drive (shift) pulse is applied to the drive windings of all the cores, transferring the contents of each core to the succeeding core. The 1 stored in core A is transferred to core B. This is possible because the inhibit winding of core B is not pulsed, core 1 having contained a C prior to the shift. The inhibit winding of core 9 is pulsed, but this has no effect on core 8 since nothing is being read out of core 1. All 1's in the ring are transferred to the next core at the end of the first shift. The 1 previously stored in core 1′ is read out to the readout register. The state of each core at the end of this first shift is shown on the Drive (Shift) Pulse 1 line of table 3–17.

After the application of the second drive pulse, all the bits are again transferred in the same manner as before. Core A has no 1 to transfer; therefore, the inhibit winding of core 9 is not pulsed, and core 9 stores the 1 it receives from core 1. Also, the read-in winding of core B is not pulsed. Thus, a 1 cannot be read into core B from

TABLE 3–16. SEQUENCE OF CCC CORE STATUS DURING ADDITION OF FIRST PULSE

Bit Significance*			2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
Core Number		9	8	7	6	5	4	3	2	1	A	B	C
Start or Reset*		1	1	1	1	1	1	1	1	1	0	0	0
Add One Pulse		1	1	1	1	1	1	1	1	1	1	0	0
Drive (Shift) Pulse	1	0	1	1	1	1	1	1	1	1	0	0	0
Drive (Shift) Pulse	2	1	0	1	1	1	1	1	1	1	0	0	0
Drive (Shift) Pulse	3	1	1	0	1	1	1	1	1	1	0	0	0
Drive (Shift) Pulse	4	1	1	1	0	1	1	1	1	1	0	0	0
Drive (Shift) Pulse	5	1	1	1	1	0	1	1	1	1	0	0	0
Drive (Shift) Pulse	6	1	1	1	1	1	0	1	1	1	0	0	0
Drive (Shift) Pulse	7	1	1	1	1	1	1	0	1	1	0	0	0
Drive (Shift) Pulse	8	1	1	1	1	1	1	1	0	1	0	0	0
Drive (Shift) Pulse	9	1	1	1	1	1	1	1	1	0	0	0	0

**Bit significance applies to cores at start or reset and after the ninth drive pulse.*

this source. Meanwhile, the 1 being read into core 9 also pulses the inhibit winding of core B. Core B transfers the 1 it contained to core C and also pulses its own feedback winding in the process. This regenerative action, called "carry-around," whereby core B reads 1's back into its own core, occurs because the read-in winding of core C is in series with the feedback winding of core B. The inhibit winding of core B, being pulsed, counteracts the pulsation of the feedback winding, and, thus, no 1 is stored in core B. It should be noted that core C contained a 0 prior to the application of the second pulse. Therefore, upon shifting, the inhibit winding of core 8 and the read-in winding of core 7 are not pulsed. Core 8 stores a 0 since it receives no input from core 9. Core 7 stores the 1 it receives from core 8. In the shifting of bits, the 1 previously stored in core 1′ is transferred to the readout register. The contents of each core at the end of the second drive pulse are shown in the Drive (Shift) Pulse 2 line in table 3–17.

After the application of the third drive pulse, the following transfers occur. As before, core A has no 1 to transfer. Therefore, the inhibit winding of core 9 and the read-in winding of core B are not pulsed. Core 9 stores the 1 it receives from core 1. The 1 read out of core 1 also pulses the inhibit winding of core B, but this has no effect since core B contained a 0 prior to the shift. Nothing is fed to core C nor is the carry-around operation of core B initiated. Meanwhile, the 1 is read out of core C, pulsing the inhibit winding of core 8 and the read-in winding of core 7. The 1 previously stored in core 9 pulses the read-in winding of core 8. However, this is counteracted by the pulsing of the core 8 inhibit winding; thus, nothing is read into core 8. The core 7 read-in winding which is coupled to core 8 is not pulsed, since core 8 was in the 0 state. However, core 7 stores a 1 because its read-in winding which is coupled to core C is pulsed. It can be seen that the net effect of the core C readout is to delay the 0 in the counter for one shift. The remaining bits are shifted in the ring as shown on the Drive (Shift) Pulse 3 line in table 3–17. After the third drive pulse, the lettered cores (A, B, and C) are all in the 0 state. The subsequent six drive pulses transfer all bits one position per shift in the ring until, after the ninth drive pulse, the count in the ring is that shown in the Drive (Shift) Pulse 9 line in table 3–17. This is the binary number 111 111 101, which is one less than the binary count of 111 111 110 contained in the ring before the introduction of the second add-in pulse.

In the foregoing paragraphs, a counting operation with a simple borrow was described. In the following text, an operation involving repeated borrowing is discussed to illustrate the operation of the carry-around function of core B. The example shows what occurs when the 128th pulse is added with the counter containing the binary count of 110 000 000. This is beyond the count of the range counter but not of the azimuth counter.

Before the 128th pulse is added, each core contains the bits shown in the Start line of table 3–18. The 128th pulse is applied to the add-in winding of core A, setting a 1 in core A. After the first drive pulse is applied, the following transfers occur. Core A is cleared, and the 1 is set in core B. The core B inhibit winding is not pulsed

TABLE 3–17. SEQUENCE OF CCC CORE STATUS DURING ADDITION OF SECOND PULSE

Bit Significance*			2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
Core Number		9	8	7	6	5	4	3	2	1	A	B	C
Start		1	1	1	1	1	1	1	1	0	0	0	0
Add Pulse 2		1	1	1	1	1	1	1	1	0	1	0	0
Drive (Shift) Pulse	1	0	1	1	1	1	1	1	1	1	0	1	0
Drive (Shift) Pulse	2	1	0	1	1	1	1	1	1	1	0	0	1
Drive (Shift) Pulse	3	1	0	1	1	1	1	1	1	1	0	0	0
Drive (Shift) Pulse	4	1	1	0	1	1	1	1	1	1	0	0	0
Drive (Shift) Pulse	5	1	1	1	0	1	1	1	1	1	0	0	0
Drive (Shift) Pulse	6	1	1	1	1	0	1	1	1	1	0	0	0
Drive (Shift) Pulse	7	1	1	1	1	1	0	1	1	1	0	0	0
Drive (Shift) Pulse	8	1	1	1	1	1	1	0	1	1	0	0	0
Drive (Shift) Pulse	9	1	1	1	1	1	1	1	0	1	0	0	0

**Bit significance applies to cores at start or reset and after the ninth drive pulse.*

because core 1 contained a 0. The 1 in core 9 is shifted to core 8, and the 1 in core 8 is shifted to core 7. The read-in winding of core 9 is not pulsed since core 1 contained a 0. Thus, core 9 contains a 0 after the first shift. All the remaining bits are transferred one position, as indicated on the Drive (Shift) Pulse 1 line of table 3–18. After the second drive pulse is applied, the following transfer takes place. Core A being cleared to 0, the read-in winding of core B and the inhibit winding of core 9 are not pulsed. (These windings are effectively out of the circuit after the first shift and are disregarded in the following description.) Core 9 contains a 0 since it receives no input from core 1. The 1's in cores 8 and 7 are shifted to the succeeding cores. The 1 stored in core B is read out to core C. However, the same 1 is also read back into core B via the feedback winding. This is the carry-around operation. The carry-around operation is completed because the inhibit winding of core B is not pulsed, core 1 having contained a 0. Thus, at the end of the second drive pulse, cores B and C both contain 1's. All the remaining bits are transferred one position, as shown on the Drive (Shift) Pulse 2 line of table 3–18. After the application of the third drive pulse, the bits are shifted as follows. The 1's stored in cores 7 and 6 are read into cores 6 and 5.

The 1 stored in core C is read into core 7. This also pulses the inhibit winding of core 8; but this produces no result, since nothing is being read into core 8. The 1 stored in core B is transferred to core C and, in a carry-around operation, back into core B. The carry-around operation is not inhibited because nothing is read out of core 1. Again, at the end of the third shift, cores B and C still contain 1's. All the remaining bits are transferred one position, as shown on the Drive (Shift) Pulse 3 line of table 3–18. Shifts 4 through 7 are identical in action with shift 3. Before the application of the eighth drive pulse, the counter cores are storing the bits shown on the Drive (Shift) Pulse 7 line in table 3–18. After the application of the eighth drive pulse, the bits are shifted as follows. The 1 stored in core 1 is read into core 9. The inhibit winding of core B is also pulsed by this readout. Meanwhile, the 1 stored in core B is read out to core C and also pulses the feedback winding on core B. However, the 1 is prevented from being read back into core B by the pulse on the inhibit winding. Hence, a 0 is stored in core B. Core 9 contained a 0 before the eighth shift. During the shift, nothing is read into core 8; therefore, at the end of the eighth shift, core 8 contains a 0. Core 8 contained a 0 before the shift. During the shift, therefore, the read-in winding of core 7, which is coupled to core 8, is not pulsed. However, the core 7 read-in winding coupled to core C is pulsed, since core C contained a 1. Thus, core 7 contains a 1 after the shift. All the remaining bits are transferred one position, as shown on the Drive (Shift) Pulse 8 line of table 3–18. After the application of the ninth and final drive pulse, the bits are shifted as described below. The 1 stored in core 9 pulses the read-in winding of core 8. However, the inhibit winding of core 8 is pulsed by the 1 stored in core C. Thus, at the end of the final shift, core 8 contains a 0. Core C also pulses the read-in winding of core 7, storing a 1 in this core. The read-in winding of core C is not pulsed, since core B con-

TABLE 3–18. SEQUENCE OF CCC CORE STATUS DURING ADDITION OF 128TH PULSE

Bit Significance*			2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
Core Number		9	8	7	6	5	4	3	2	1	A	B	C
Start		1	1	0	0	0	0	0	0	0	0	0	0
Add Pulse 128		1	1	0	0	0	0	0	0	0	1	0	0
Drive (Shift) Pulse	1	0	1	1	0	0	0	0	0	0	0	1	0
Drive (Shift) Pulse	2	0	0	1	1	0	0	0	0	0	0	1	1
Drive (Shift) Pulse	3	0	0	1	1	1	0	0	0	0	0	1	1
Drive (Shift) Pulse	4	0	0	1	1	1	1	0	0	0	0	1	1
Drive (Shift) Pulse	5	0	0	1	1	1	1	1	0	0	0	1	1
Drive (Shift) Pulse	6	0	0	1	1	1	1	1	1	0	0	1	1
Drive (Shift) Pulse	7	0	0	1	1	1	1	1	1	1	0	1	1
Drive (Shift) Pulse	8	1	0	1	1	1	1	1	1	1	0	0	1
Drive (Shift) Pulse	9	1	0	1	1	1	1	1	1	1	0	0	0

**Bit significance applies to cores at start or reset and after the ninth drive pulse.*

tains a 0. Therefore, at the end of the final shift, all the lettered cores contain 0's. All the remaining bits are transferred one position during the final shift. The ninth and final shift leaves the counter as shown on the Drive (Shift) Pulse 9 line of table 3–18. The binary count is 101 111 111 which is one less than the starting number 110 000 000.

The CCC is cleared at the end of the count as follows. A 6.4-μsec pulse at standard level is applied to the series-connected core reset windings from the output of a GCSD. (Refer to 3.20 for a detailed description of the GCSD.) This resets all the cores in the ring (cores 1 through 9) to 1 and core C to 0.

Core C is cleared to 0 by the reset pulse to prevent it from performing an operation which would be erroneous. As described in 3.11.1, the azimuth counter counts to 256 before it is recycled. However, because of the arithmetic involved (1 from binary number 100 000 000) and complementing core limitation, a 1 remains in core B at the end of the operation. During the first shift of the subsequent countdown, this would be read out of core C, inhibiting core 8. Thus, a false count would be presented in the counter. To prevent this, core C is cleared during the reset operation. Core C in the range counter is also cleared during the reset operation in its counter. This is done for circuit standardization purposes only, since the range counter counts only to 64.

3.12 CONSTANT VOLTAGE AMPLIFIER

3.12.1 Definition and Description

The constant voltage amplifier (CVA) is an amplifier circuit which provides a constant voltage output. The logic block symbol for the CVA is shown in figure 3–32.

3.12.2 Principles of Operation

Figure 3–33 is the schematic diagram of the CVA. Table 3–19 lists the associated detail parts and their functions. The circuit consists of two pentode tubes and three triode sections. The two pentode tubes, V1 and V2, comprise a 2-stage voltage amplifier. The input signal, a 1,300-cycle 60V peak-to-peak sine wave, is applied to the control grid of V1. This signal is amplified and applied to the grid of V2 through C2. The output of V2 is a constant 12V peak-to-peak sine wave.

The triode tubes, V3, V4, and V5, comprise a negative feedback network which applies d-c bias to the control grids of V1 and V2. This bias is proportioned to the input voltage. Consequently, automatic regulation for producing a constant 12V peak-to-peak output is achieved for inputs from 2 to 12V peak to peak.

The feedback voltage is taken from the output of V2 and coupled through C7 to the grid of V5. Tube V5 amplifies the feedback voltage to 60V peak to peak. This 60V signal is applied to the grid of V4 which is operated near cutoff. The output of V4 taken from across C5 is a d-c level which varies in accordance with amplitude variations of the 1,300-cycle, 60V input signal. This d-c signal is amplified by V3 with capacitor C4 filtering out any remaining 1,300-cycle component present in the signal. The d-c signal is then used to bias voltage amplifiers V1 and V2. Negative bias is increased when the output from V2 tends to exceed 12V; it is decreased when the output tends to become less than 12V.

TABLE 3–19. CONSTANT VOLTAGE AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1
R2	Plate load for V1
R3	Screen-dropping resistor for V1
R4	Grid return for V2
R5	Plate load for V2
R6	Provides degeneration for improved regulation
R7	Screen-dropping resistor for V2
R8	Output load resistor
R9, R10	Provides bias for V1 and V2, with R10 as V3 plate load
R11	Part of V4 cathode load (with C5 and R13)
R12	Forms part of voltage divider network (with R14 and R16)
R13	Cathode load for V7 (with C5 and R11)
R14	Part of voltage divider (with R12 and R16)
R15	Grid-dropping resistor V4
R16	Part of voltage divider network (with R12 and R14)
R17	Plate load resistor for V5
R18	Cathode bias for V5
R19	Grid-dropping resistor V5
R20, R21	Voltage divider network
C1-C3	Coupling capacitors
C4	Bypass capacitor
C5	Part of V4 cathode load (with R11 and R13)
C6, C7	Coupling capacitors

3.13 CONTRAST GATE ISOLATION AMPLIFIER, MODEL A

3.13.1 Definition and Description

The model A contrast gate isolation amplifier (ACGA) is a non-logic circuit which isolates the contrast gate input from the erase gate input of the DD tube. The logic block symbol of the ACGA is shown in figure 3–34.

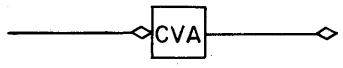
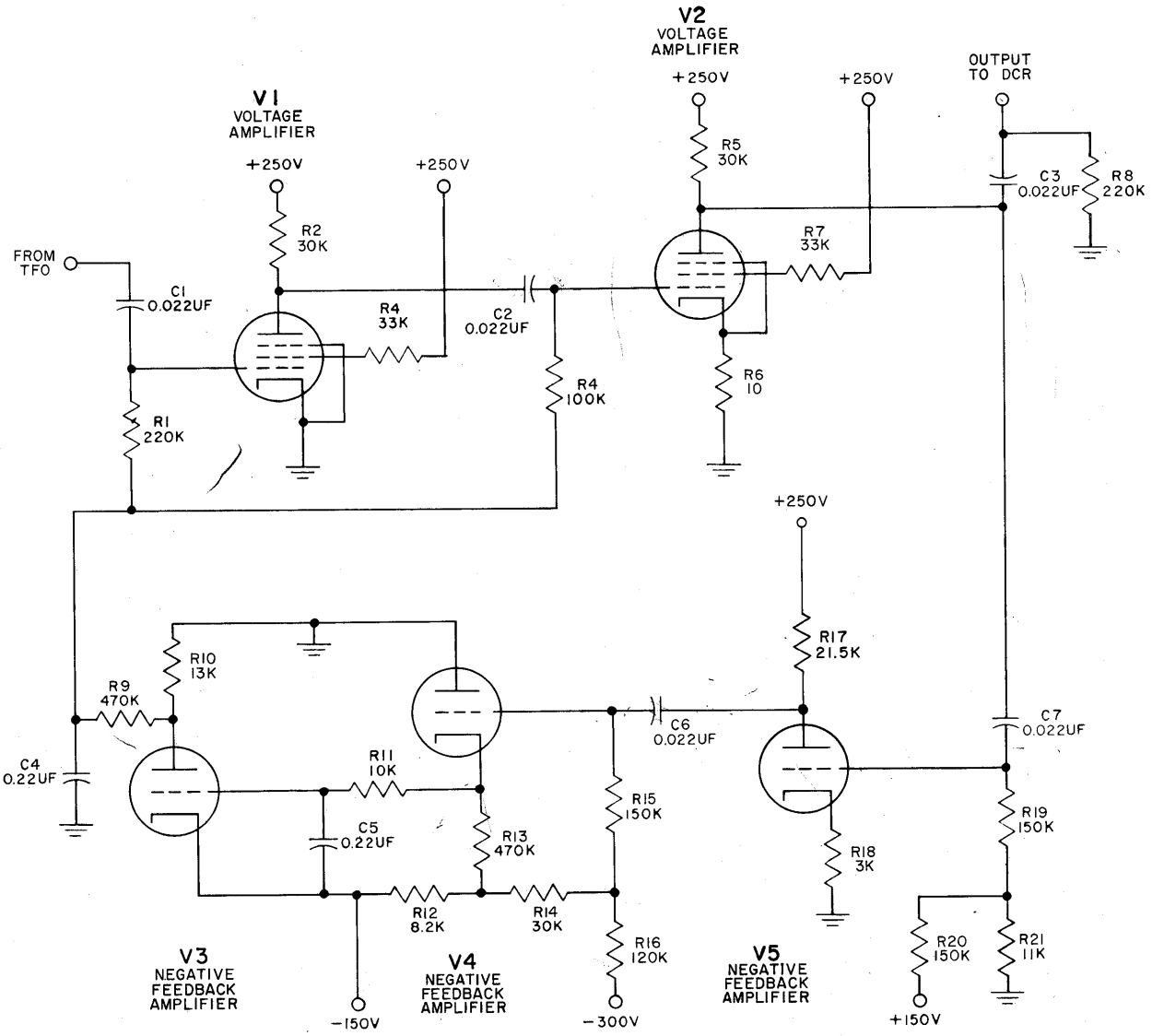


Figure 3–32. Constant Voltage Amplifier, Logic Block Symbol

3.13.2 Principles of Operation

Figure 3–35 is the schematic diagram of the ACGA. Table 3–20 lists the associated detail parts and their functions. The circuit consists of a cathode follower and associated components. With −30V applied to the input of the ACGA and R1 adjusted for maximum output, the cathode of V1 is at −30V. With a 40V, 10 -μsec positive pulse applied to the input and R1 adjusted for maximum output, the control grid of V1 is driven to +10V. This change in cathode potential is ac-coupled to the mesh level and erasure unit. The setting of potentiometer R1 determines the magnitude of cathode current which, in turn, establishes the output levels of the CGA.



NOTES:

1. SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT.
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED.

Figure 3–33. Constant Voltage Amplifier, Schematic Diagram

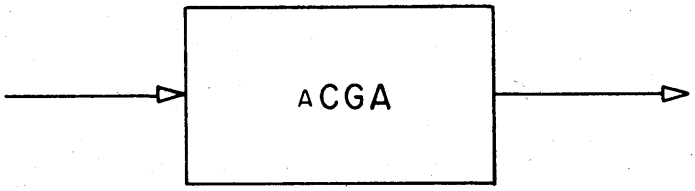


Figure 3–34. Contrast Gate Isolation Amplifier, Model A, Logic Block Symbol

TABLE 3–20. CONTRAST GATE ISOLATION AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Contrast gate amplitude control
R2	Cathode load resistor
C1	Output coupling capacitor
V1	Cathode follower triode

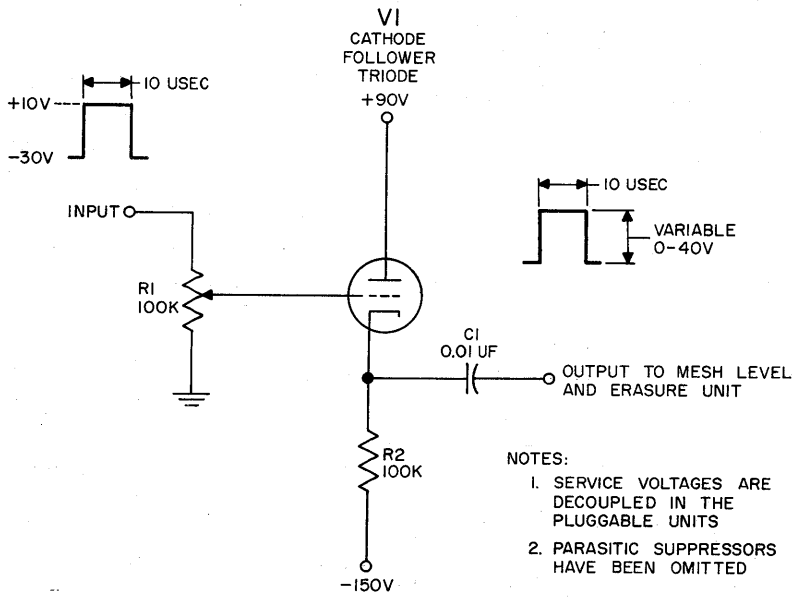


Figure 3–35. Contrast Gate Isolation Amplifier, Model A, Schematic Diagram

3.14 CONVERGENCE CURRENT REGULATORS, MODELS A, B, AND C

3.14.1 Definition and Description

The convergence current regulators (CCR) are non-logic circuits which provide regulated current supplies. In Display System logic, three models of CCR's are utilized. One model (ACCR) supplies current to the SD CRT convergence coil assembly; the second (model BCCR) supplies current to the DD CRT convergence coil; and the third (model CCCR) supplies current to the focus coil of the 7-inch SD CRT in the photographic-recorder reproducer. The logic block symbol for the models A and B CCR is shown in figure 3–36. Figure 3–37 is the logic block symbol for the CCCR.

Models A and B are identical with the exception of the two model-distinguishing components which are made necessary by the different load requirements of the SD and DD CRT convergence coil assemblies. Since both circuits perform identically, only one is discussed below.

The model CCCR is basically the same circuit as the model ACCR but has been modified to supply 25 ma to the focus coil. This circuit is discussed separately.

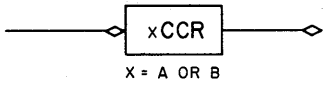


Figure 3–36. Convergence Current Regulator, Models A and B, Logic Block Symbol

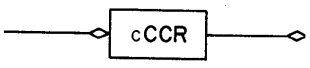


Figure 3–37. Convergence Current Regulator, Model C, Logic Block Symbol

3.14.2 Principles of Operation, Models A and B

3.14.2.1 Basic Operation

Figure 3–38 is the schematic diagram for both models A and B of the CCR. Table 3–21 lists the associated detail parts and their functions. As stated above, with the exception of the two model-distinguishing components (R5 and R6), both models are alike. The circuit consists of a cascade amplifier, a series regulator tube, a voltage regulator, and associated circuitry. With the convergence current amplitude controls adjusted, the magnitude of current applied to the convergence load becomes a function of V2 cathode current. Current regulation, with accelerating voltage constant, is accomplished by sampling the magnitude of load current. If this load current changes, a voltage proportional to this current variation is fed back to the cascade-connected amplifier and amplified. The output, applied to the control grid of V2, controls the conducting level of V2, opposing the original plate current variation and thus maintaining the convergence current constant.

TABLE 3–21. CONVERGENCE CURRENT REGULATOR, MODELS A AND B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Isolating resistor
R3	Plate load for V1A
R4	Cathode load for V2
R5	Current-limiting resistor, used only in model B
R6	Series-regulating resistor

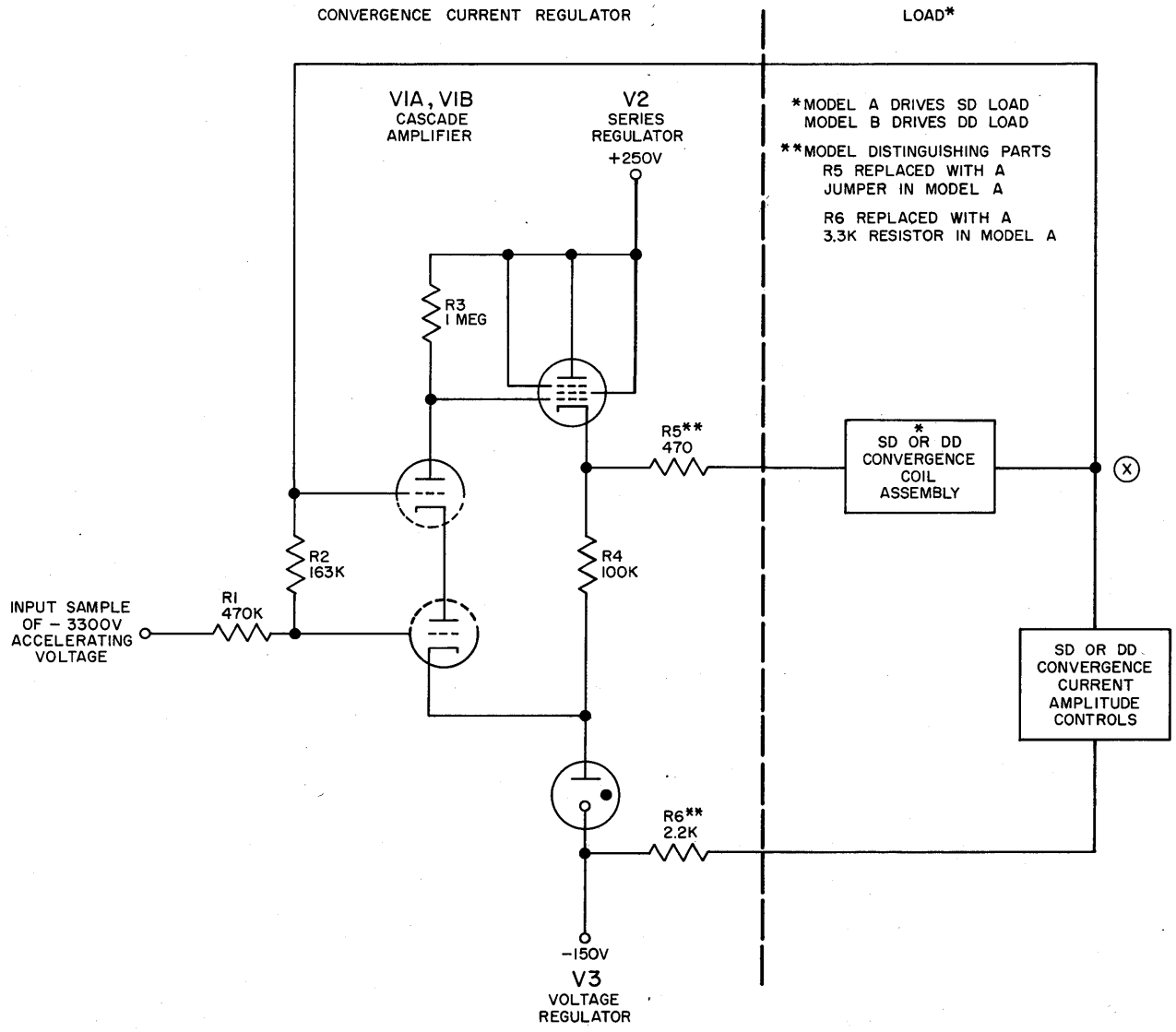


Figure 3–38. Convergence Current Regulators, Models A and B, Schematic Diagram

3.14.2.2 Detailed Operation

In its quiescent state, the CCR produces a constant output. Constant current regulation occurs in the following manner. Assume that the load current, which flows from the —150V source through R6, the convergence current amplitude controls, the convergence coil assembly, and V2, increases. When this occurs, the potential at point X becomes more positive. This positive voltage change appears at the control grids of cascade-connected triodes V1A and V1B. The cathode of V1B is held at a fixed potential by voltage regulator V3. The increase in potential at the grid of V1B produces a decrease in the plate voltage of V1B. Since the cathode of V1A is connected directly to the plate of V1B, triode V1A cathode potential also decreases. This adds to the effect of the increase in V1A grid voltage which, in turn, produces a drop in potential at the plate of V1A. The plate of V1A is directly coupled to the control grid of V2; hence, the potential at the control grid of V2 drops, reducing the current through V2. Since the convergence coil assembly current is dependent upon V2 plate current, the convergence current decreases, opposing the original change that had occurred. A decrease in convergence current would be compensated for in a similar manner. Cascade-connected amplifiers are employed to increase the overall sensitivity of the CCR to load current variations.

Voltage changes in the input sample caused by variations of accelerating voltage supply produce corresponding proportionate changes in the convergence current. Assume that an increase in the accelerating voltage has occurred (more negative). As a result of this change, the grid of V1B (and V1A) becomes more negative. The plate voltage of V1B rises, resulting in an increased cathode voltage for V1A. This change, in addition to the grid of V1A becoming more negative, increases the plate voltage of V1A which, in turn increases the control grid potential of series regulator V2. Consequently, V2 conducts more heavily, increasing the convergence current. Since the current changed from its quiescent state, voltage is fed back to the grids of V1A and V1B, attempting to oppose the change. The amount of feedback is less than the original change initiated by the accelerating voltage variation. Therefore, the resulting net increase in convergence current is sufficient to compensate for the increase in accelerating voltage. A decrease in accelerating voltage (—3,300V) would cause a decrease in convergence current in a similar manner.

3.14.3 Principles of Operation, Model C

3.14.3.1 Basic Operation

The cCCR is shown in schematic form in figure 3—39. Table 3—22 lists the associated detail parts and their functions. The circuit consists of a series regulator tube (V2), a feedback amplifier tube (V1), a voltage reference tube, and a manual current amplitude control.

TABLE 3—22. CONVERGENCE CURRENT REGULATOR, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Plate load resistor for V1A
R2, R3	Part of voltage divider (with R5 and R6)
R4	Current-limiting resistor
R5, R6	Part of voltage divider (with R2 and R3)
R7	Current amplitude control
R8, R9	Serves regulating resistors

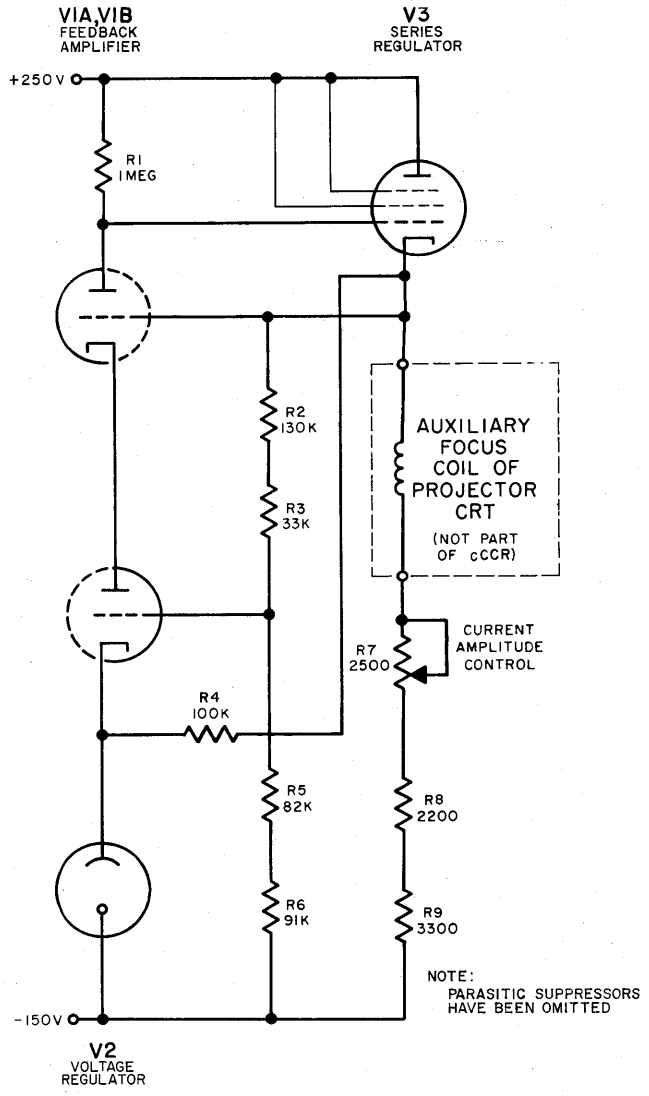


Figure 3—39. Convergence Current Regulator, Model C, Simplified Schematic Diagram

The primary function of this circuit is to regulate focus coil current of the 7-inch SD CRT. With the manual current amplitude control set, the magnitude of current applied to the focus coil becomes a function of the series regulator plate current. Current regulation is accomplished by controlling a series regulator with an amplified sample of the focus current. This voltage, proportional to the current through the auxiliary focus coil, is fed to the feedback amplifier. The output of the feedback amplifier is applied to the series regulator, opposing any variations in the focus coil current.

3.14.3.2 Detailed Operation

Regulation in the cCCR is accomplished in the following manner. Assume that the focus current increases (current flows from the —150V supply through resistors R9, R8, R7, the focus coil, and tube V3 to the +250V supply), making the cathode of V3 more positive. The cathode of V3 is coupled to the grids of V1A and V1B. The cathode of V1B is maintained at a fixed potential by voltage regulator V2. With a rise in potential on the grids of V1A and V1B, these triodes, which are connected in series, draw increased current through resistor R1, causing an increased drop across R1 and, hence, a lower potential on the control grid of triode-connected pentode regulator V3.

The reduction of control grid potential reduces the current passed by V3, correcting for the initial current increase which initiated the regulator action. A decrease in current would cause a comparable reaction in the feedback network but in the opposite phase, causing an increase in potential at the control grid of V3 and a resultant increase in the focus current flowing through the tube.

3.15 CORE CURRENT DRIVER

3.15.1 Definition and Description

The core current driver (CCD) is a nonlogic circuit which supplies the half-write current to ferrite cores in the ferrite core array of the Output System. The logic block symbol for the CCD is shown in figure 3–40.

3.15.2 Principles of Operation

Figure 3–41 is the schematic diagram for the CCD. Each CCD consists of a metallic tape core upon which are wound three separate windings, a set winding, a reset-inhibit winding, and an output winding. The set winding consists of 200 turns and represents the output of the set driver circuit. The reset-inhibit winding consists of 40 turns and represents the output of the reset-inhibit driver. The output winding, which consists of 30 turns, switches the associated ferrite cores in the array by driving a 2-turn winding on these associated cores. Operation of the CCD involves switching the tape core from its reset saturated state to a set saturated state and then back to its original state.

Switching of the CCD is influenced by two circuits: the set driver (par. 3.75) and the reset-inhibit driver (par. 3.71). The set windings of the CCD's are connected in series and represent the output load of the set driver circuit. The reset-inhibit windings of the CCD's are connected in series and represent the output load of the reset-inhibit circuit. The output winding of each of the CCD's is series-connected with a 2-turn winding on the ferrite cores in a particular address row or message column of the array.

A CCD is set when its associated set driver is pulsed after the latter has been conditioned by message or address information. The output current of the set driver required to switch from reset to set is nominally 28 ma. Switching from the reset state to the set state produces a pulse in the output winding of the CCD. Since during normal operation the output resulting from a set pulse to the CCD occurs only after the ferrite cores have been read out (driven to a 0 state), this output has a negligible effect on the ferrite cores. The set information is retained in the CCD until the reset-inhibit driver is pulsed. The reset-inhibit pulse resets the CCD, resulting in the CCD's output winding delivering a half-write current to all the ferrite cores in its associated row or column of the array.

For the situation where no information is set into a CCD by its associated set driver, but the reset-inhibit driver passes a current through the core winding, an out-

Figure 3–40. Core Current Driver, Logic Block Symbol

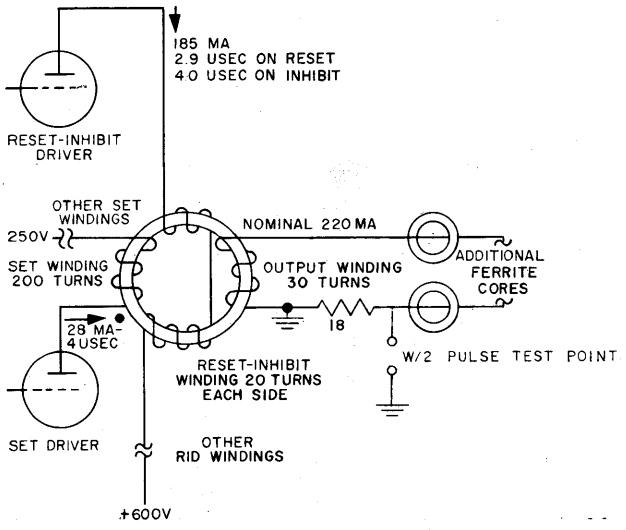


Figure 3–41. Core Current Driver, Schematic Diagram

put current is produced which has a negligible effect on the ferrite core array.

The full-write current necessary to set a ferrite core occurs with the coincidence current produced by two CCD outputs, one driving the address axis and the other driving the message axis.

3.16 CORE DELAY REGISTER

3.16.1 Definition and Description

The core delay register (CDR) is a logic circuit which is used to delay a pulse for a fixed period of time. The logic block symbol for the CDR is shown in figure 3–42.

In Input System logic, the CDR controls the number of drive pulses applied to the range and azimuth complement core counters (CCC's) and to the range and azimuth parallel readout registers.

3.16.2 Principles of Operation

Figure 3–43 is the schematic diagram of the CDR. The circuit is composed of nine 4-winding core shifts (one DCS and eight ECS's connected in series. (Core shifts are described in par. 3.19.) All core shifts in the CDR, with the exception of the last core, are identical. The output of the CDR sets a flip-flop. Therefore, no delay circuit is required in the readout winding of the last core. In addition, the terminals of the readout winding are reversed to produce a negative pulse to trigger the flip-flop.

A 1 is read into the CDR every 625 μsec by the application of a positive-current pulse to the add-in winding of the first core (DCS) in the register. The CDR is then shifted nine times. Each drive shift pulse at 20-μsec intervals causes the 1 read into the first core to be transferred to the next core until, at the ninth pulse, the 1 is read out of the ninth core. This output is used to stop the generation of shift pulses and to initiate the reset signal which clears the CDR.

A reset signal of 445-μsec duration is required to erase any extraneous 1's remaining in the CDR at the completion of the shifting operation. Assume that core four of the CDR is erroneously magnetized to the 1 state when the first 1 is read out of core nine. The next shifting operation will then continue until this 1 appears in the output. As a result, the generation of shift pulses will stop after five rather than after the required nine shift pulses have been received.

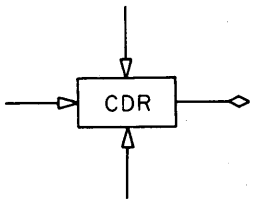


Figure 3–42. Core Delay Register, Logic Block Symbol

3.17 CORE MEMORY DRIVER

3.17.1 Definition and Description

The core memory driver (CMD) is a logic AND circuit which is capable of generating bidirectional output current pulses. There are 128 CMD's used in the core memory element. Each CMD supplies read and write

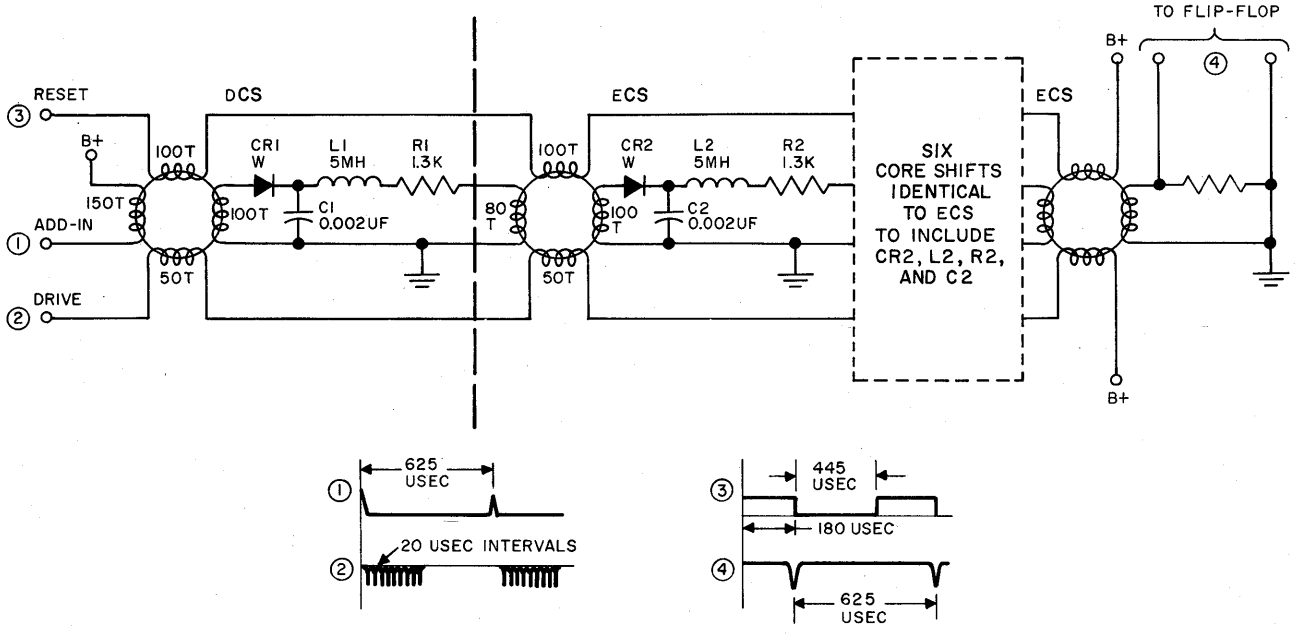


Figure 3–43. Core Delay Register, Schematic Diagram

current pulses to one X or Y line of a core memory array. The nominal value of these current pulses is equal to one-half the current needed to switch a ferrite core. Only one X and one Y core memory driver is fully selected at any one time. The logic symbol for the CMD is shown in figure 3–44.

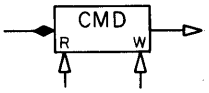
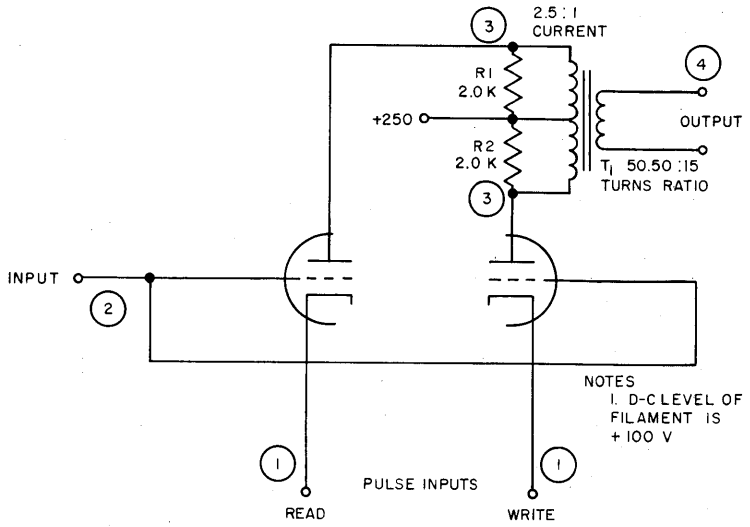


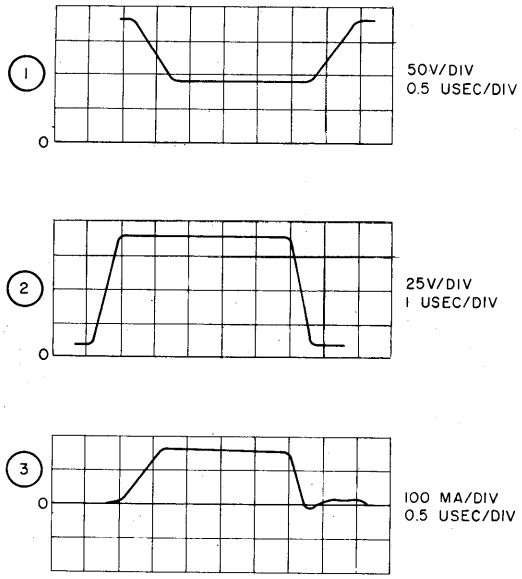
Figure 3–44. Core Memory Driver, Logic Block Symbol

3.17.2 Principles of Operation

Figure 3–45 is the schematic diagram of the CMD. The circuit consists of a dual triode (V1) one half of which drives read pulses and the other half of which drives write pulses. The plates of the tube are connected to a center-tapped pulse transformer.

An unselected matrix output amplifier applies approximately +10V to the grids of V1. The cathodes are held at +180V by the memory gate generator outputs to which the cathodes are connected. As long as these cathodes are held at +180 V, the CMD tubes will not conduct since the input from the matrix output amplifier is not sufficient to overcome the positive cathode potential.





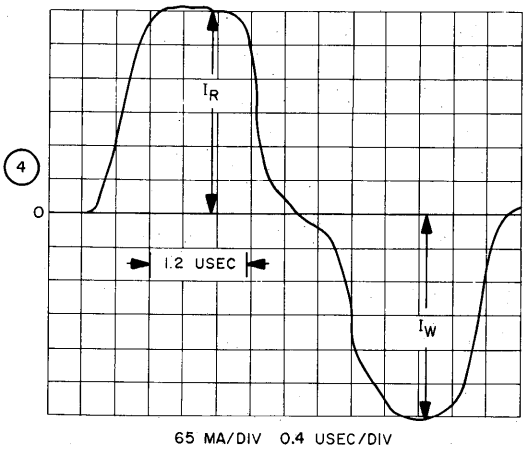


Figure 3–45. Core Memory Driver, Schematic Diagram

When a read pulse is applied to the read memory gate generator, the output of the generator falls toward —300V but is caught at about +90V. This lowers the bias on the CMD, permitting the read side of V1 to conduct. When the read side of V1 is conducting, a current flows in the pulse transformer secondary. The polarity of this current is defined as the read direction. The current ratio of the pulse transformer is 2.5 to 1. Consequently, a primary current of 160 ma produces a current of 400 ma in the secondary. A current of this magnitude is necessary to drive a core to the coincident current method of core selection used in the memory element.

When a write pulse is applied to the write cathode of V1, the other half-tube conducts; since this current is in the opposite direction in the pulse transformer primary, the secondary current is of opposite polarity to the read pulse. The magnitude of the write pulse can be equal to the read pulse, depending on how the memory gate generator output is adjusted.

3.18 CORE PRIME, MODELS A, B, C, AND D

3.18.1 Definition and Description

A core prime (CP) is a nonlogic power-amplifying circuit which provides a high-current output pulse utilized to set a core shift to the 1 state.

Table 3–23 lists the four models of CP's utilized in AN/FSQ-7 and -8 equipments. Each circuit is listed by logical symbol showing the characteristics which distinguish one model from the other.

TABLE 3–23. CORE PRIME MODEL-DISTINGUISHING CHARACTERISTICS

MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A	ACP	Drives a model A, B, or C core shift with standard level input pulse
B	BCP	Drives a model C core shift with either a standard pulse input or with a 1 output from a core bit.
C	CCP	Drives one or two model C core shifts connected in parallel upon application of an input pulse that consists of a 1 output from a core bit.
D +90	DCP	Drives a model C core shift with an output current which is generated within the circuit by the discharge of a capacitor through a choke, resistor, and core input winding in series. The depression of a pushbutton permits this to occur.

3.18.2 Principles of Operation

The electronic operation of the models is identical; therefore, only the model A is described in detail. The schematic diagram for the ACP is shown in figure 3–46. Table 3–24 lists the associated detail parts and their functions. The circuit consists of a cathode follower and associated components.

With no input signal, a negative voltage of approximately 22V (grid to cathode) maintains the tube at cutoff. This voltage is obtained by connecting the grid circuit to a voltage divider which is connected to the —30 and —150V supplies and by connecting the cathode circuit to the —15V supply. The voltage divider is placed at a-c ground potential by a capacitor which is located at the junction of the two resistors comprising the divider.

When a —30V level is applied to the input of the CP, the tube remains at cutoff; when the pulse level rises to +10V, plate current flows. The plate current, returning to the cathode through the input or prime winding of the core load, switches the core to the 1 state. When the input pulse level reaches + 10V, the grid becomes

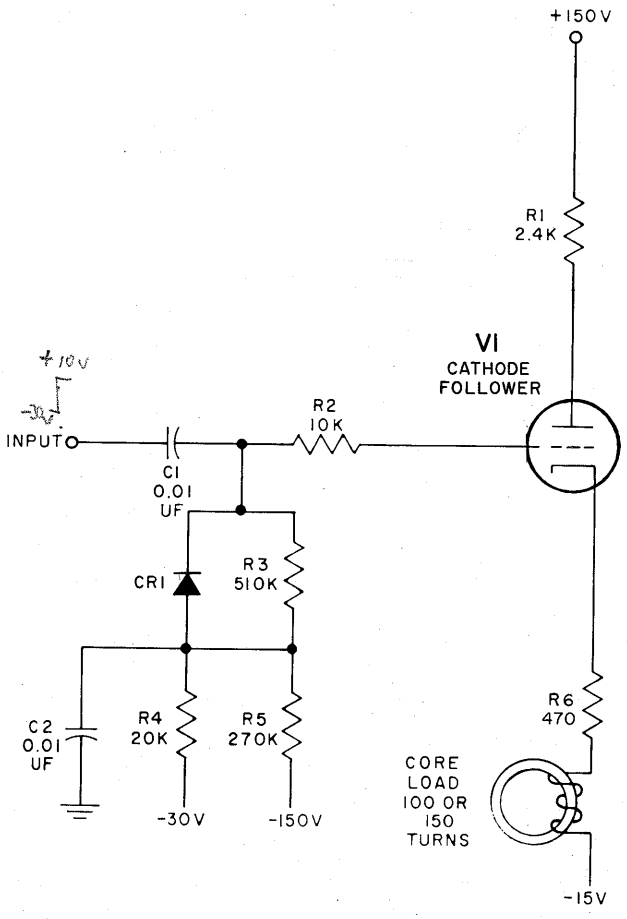


Figure 3–46. Core Prime, Model A, Schematic Diagram

TABLE 3–24. CORE PRIME, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Plate current-limiting resistor
R2	Grid-limiting resistor
R3	Grid return resistor
R4, R5	Form voltage divider which determines grid bias
R6	Prevents CP from conducting due to transformer action when the core shift driver is pulsed
C1	Input coupling capacitor
C2	Places junction of voltage divider R4 and R5 at a-c ground potential
CR1	Crystal diode which serves to prevent d-c restoration action at input

positive, causing grid current to flow, causing the coupling capacitor in the input circuit to charge. This tends to build up the bias, producing a d-c restoration action. However, this condition is prevented by the action of crystal diode CR1 in discharging the coupling capacitor rapidly.

3.19 CORE SHIFTS

3.19.1 Definition and Description

A core shift (CS) is a logic circuit which possesses two stable states of magnetization and is used as a storage device.

There are 15 models of CS's utilized in AN/FSQ-7 and -8 equipments. The most significant differences between each model are in the number of windings used and the number of turns in each winding. The basic CS contains three windings: an add-in (or read-in) winding, a readout winding, and a drive winding. All other CS's contain a fourth winding, the reset winding. In addition, several models contain a fifth winding, either inhibit or feedback, depending on its application in a circuit. Basically, the principles of operation for all CS's are identical. For this reason, only the basic CS is described in detail below. Figure 3–47 shows the logic block symbol of a basic CS.

3.19.2 Principles of Operation

Figure 3–48 is the schematic diagram of the basic CS. The core shift consists of three windings: an add-in (or read-in) winding, a readout winding, a drive winding, and associated components.

The magnetization state (1 or 0) of the core is varied by the application of current pulses applied to its add-in and drive windings. The magnetizing process follows the hysteresis loop illustrated in figure 3–49. Assume (fig. 3–49) that the core is initially at flux point A (0 state). The application of a positive current pulse to the add-in winding changes the flux state of the core to the point represented by C. When the current returns to 0, the flux value decreases to the point represented by B (1 state). A negative-current pulse applied to the drive winding will then change the flux state of the core to the point represented by D. When this current returns to 0, the flux value returns to point A and the core is once again at the 0 state. The flux value remains at point A until the application of a second positive pulse.

The application of a pulse to the drive winding will always cause the core to store a 0 regardless of its previous state. If the core had been storing a 1, applying a pulse to the drive winding causes a reversal in

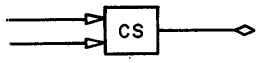


Figure 3–47. Basic Core Shift, Logic Block Symbol

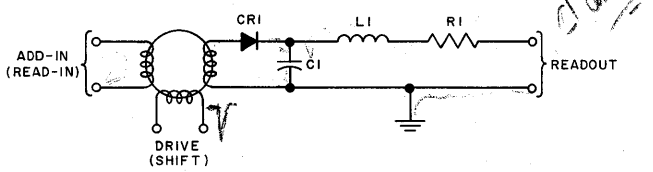


Figure 3–48. Basic Core Shift, Schematic Diagram

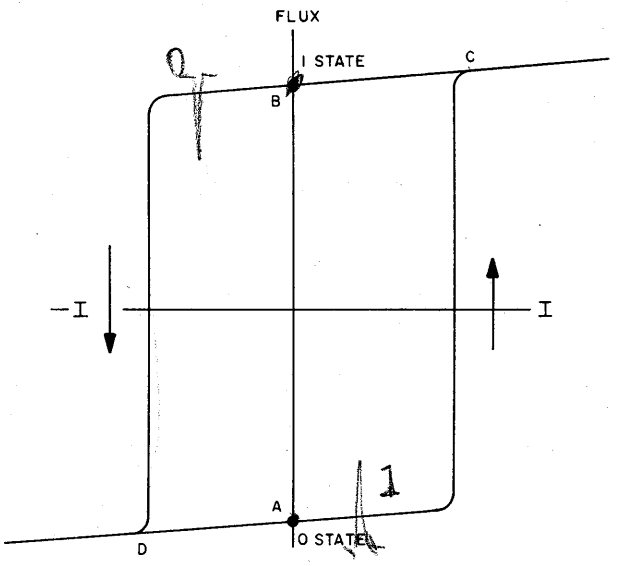


Figure 3–49. Typical Magnetic Tape Core Hysteresis Loop

the direction of core magnetization. As a result, the core is cleared and returns to the 0 state. If the core had been storing a 0, the application of a pulse to the drive winding has no effect on the magnetization and the induced output voltage is negligible.

The readout circuit of a CS makes possible the transfer of a 1 from one core to another. This transfer function is utilized in CS registers. As described previously, when a CS is magnetized in the 1 state, the application of a negative-current pulse to the drive winding causes a reversal in the magnetization of the core. This induces a voltage across the readout winding which charges capacitor C1 (fig. 3–48) through diode CR1. Diode CR1 prevents the capacitor from discharging through its charging path. Inductor L1, because of its high impedance, prevents the initial surge of the C1 charging current from flowing through the parallel path which includes the read-in winding of the next CS and resistor R1. The value of R1 determines the discharge time of C1. This resistance is sufficiently high to enable C1 to retain a considerable charge after the decay of the drive pulse. At the end of the drive pulse, C1 discharges completely through L1, R1, and the read-in winding of the next core. The discharge current writes a 1 into this core. This transfer of a 1 occurs whenever a drive pulse is applied to the drive windings of a core storing a 1. Thus, a stored 1 can be shifted through a register by applying as many drive (shift) pulses as there are CS's in the register.

3.20 CORE SHIFT DRIVERS

3.20.1 Definition and Description

A core shift driver (CSD) is a nonlogic circuit which provides the current necessary to transfer information serially through a register. Table 3–25 lists the seven models of CSD's utilized in AN/FSQ-7 and -8 equipments. Each model is listed by its logic block symbol showing the characteristics which distinguish one model from the other.

3.20.2 Principles of Operation, Model C

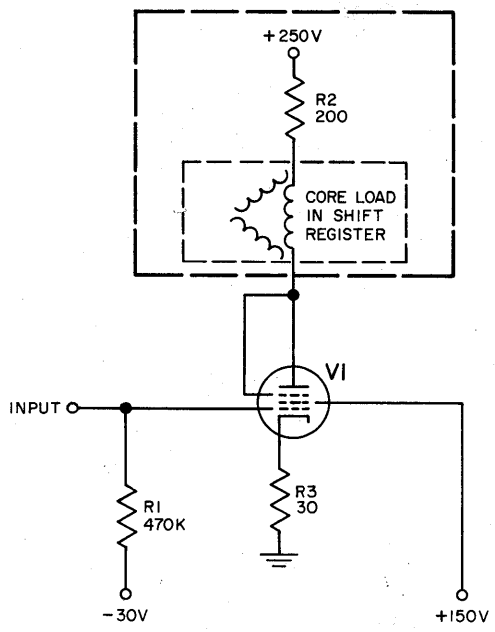
The cCSD is a typical CSD circuit and is used as an example of CSD circuits in general in the following discussion.

The cCSD, shown in schematic form in figure 3–50, consists of a pentode amplifier and associated components. The plate load of the stage consists mainly of the series-connected CS drive windings or the add-in windings. In its quiescent state, the voltage at the grid of V1 is −30V which is the effective bias on the tube, and the cathode is at ground potential. The input signal to the stage, which is developed across grid return resistor R1, is a pulse +10V in amplitude and approximately 3.5 μsec (bias-width) in duration. As this input voltage rises to +10V, the bias on the tube is overcome,

TABLE 3–25. CORE SHIFT DRIVERS, MODEL-DISTINGUISHING CHARACTERISTICS

MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A	ACSD*	Provides current to drive eight cores in the shift register of the manual data input unit.
B	BCSD	Provides current to read out tape cores in 3-output shift register of output storage section.
C	CCSD	Provides read current for the core shift register.
D	DCSD	Provides add-in current in tape-core counter.
E	ECSD*	Provides shift current in tape core counter.
F	FCSD*	Provides shift current in the parallel readout and identification register.
G	GCSD	Provides current to reset cores in azimuth counter.

**Logic block symbols for these models identical with that for model cCSD.*



NOTES:
1. SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

Figure 3–50. Core Shift Driver, Model C, Schematic Diagram

and the stage conducts. When the stage conducts, plate current flows through the core load in the shift register. When the stage is being employed to amplify drive pulses, the plate current magnetizes the cores in a direction opposite that caused by setting a 1 into the cores. When the stage is being employed to amplify add-in pulses, the plate current magnetizes the cores in such a direction as to set the cores to 1.

3.21 CRYSTAL OSCILLATORS

3.21.1 Definition and Description

The crystal oscillator (OSC) is a logic circuit which generates a sine wave signal of specified frequency. Table 3–26 lists the logic block symbols and the frequencies of operation of the three models of the oscillator. The cOSC and dOSC serve as master clocks in the Central Computer. The eOSC is used to produce simulated output drum timing pulses in the Display System.

3.21.2 Principles of Operation

3.21.2.1 Detailed Operation, Model C

Figure 3–51 is the schematic diagram of the cOSC. Table 3–27 lists the associated detail parts and their functions. The cOSC is a crystal-controlled oscillator. Crystal Y1 has the property of vibrating at its natural frequency when an a-c voltage is impressed across it. Similarly, if mechanically stretched or compressed in certain directions, the crystal will accumulate a charge (voltage) across its terminals. If the frequency of the a-c voltage impressed on the crystal is close to its natural frequency, the crystal will produce an amplified voltage at its natural frequency. Crystal current produced at the natural frequency of the crystal is similar to the current produced by a series-resonant circuit. Thus, the crystal may be represented by the parallel combination of a series-resonant circuit and a capacitor. See figure 3–52. Capacitance CM is the capacity added across the crystal by the physical mounting of the crystal in the circuit. Detail parts LC and CC form the series-resonant crystal-equivalent circuit. The plate tank circuit, L1, C1, and C2 in figure 3–51, is tuned to a frequency that is higher than the natural frequency of the crystal. The crystal equivalent series-resonant circuit is inductive at this frequency; that is, the impedance of LC is greater than the impedance of CC. Combined with CM, the inductive

TABLE 3–26. CRYSTAL OSCILLATORS, LOGIC BLOCK SYMBOLS AND OPERATING FREQUENCIES

MODEL	LOGIC BLOCK SYMBOL	FREQUENCY
C	cOSC →	2 mc
D	dOSC →	1.19 mc
E	eOSC →	400 kc

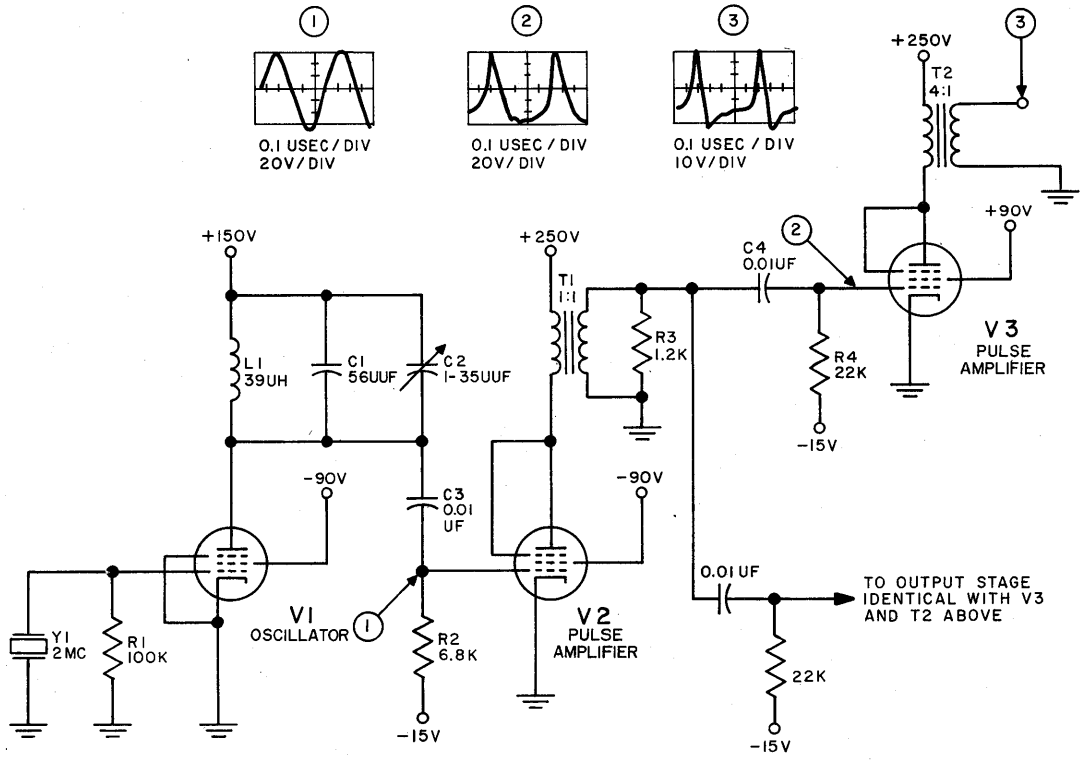


Figure 3–51. Crystal Oscillator, Model C, Schematic Diagram

circuit forms a parallel resonant circuit at the calibrated frequency of the crystal (2 mc in cOSC).

As in tuned-plate, tuned-grid oscillators, the feedback path must be capacitive for the plate voltage to produce a leading current (90 degrees) in the grid circuit. Inter-electrode capacitance between the grid and plate of V1 is the feedback coupling capacitor. The impedance of the capacitor is larger at the feedback frequency than the grid circuit inductance, making the resultant current a leading one by 90 degrees with respect to plate voltage. In turn, this current induces a leading voltage (90 degrees) across the inductance in the grid circuit. The 180 degree shift in voltage provides the requisite in-phase relationship between plate feedback voltage and grid voltage to sustain oscillation.

3.21.2.2 Detailed Operation, Model D

The DOSC (fig. 3–53) is similar to the cOSC. The calibrated frequency of the crystal is 1.19 mc. Detail parts L1, C1, and C2 are selected to make the plate tank circuit capable of being tuned to a frequency higher than 1.19 mc. The 1.19 mc output sine wave of the DOSC is fed through two cascaded model D shapers (DSH) to produce a train of standard pulses at 0.84-μsec intervals. Refer to table 3–28 for the function of DOSC detail parts.

3.21.2.3 Detailed Operation, Model E

The EOSC (fig. 3–54) is similar in operation to the oscillator stage of the cOSC. Crystal Y1 is calibrated at 400 kc. Tank circuit detail parts L1 and C2 are selected to be resonant at a frequency slightly higher than 400 kc. The EOSC produces a 400-kc sine wave which is shaped by four cascaded model E pulse shapers, (EPS) into a train of standard pulses at 2.5-μsec intervals. Refer to table 3–29 for the function of detail parts.

TABLE 3–27. CRYSTAL OSCILLATOR, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Plate tank circuit (with L1 and C2)
C2	Tank circuit trimmer
C3, C4	Coupling capacitors
L1	Plate tank circuit (with C1 and C2)
R1	Grid load for V1
R2	Grid return for V2
R3	Damping resistor
R4	Grid return for V3
T1, T2	Pulse-shaping transformers
Y1	Crystal

TABLE 3–28. CRYSTAL OSCILLATOR, MODEL D, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Plate tank circuit (with L1 and C2)
C2	Tank circuit trimmer (fine frequency adjustment)
L1	Plate tank circuit (with C1 and C2)
R1	Grid load resistor
Y1	Frequency-determining crystal

TABLE 3–29. CRYSTAL OSCILLATOR, MODEL E, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Feedback capacitor
C2	Plate tank circuit (with L1)
C3	Output coupling capacitor
L1	Plate tank circuit (with C2)
R1	Grid load resistor
Y1	Frequency-determining crystal

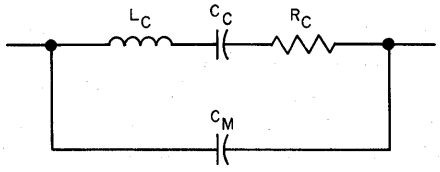


Figure 3–52. Crystal Equivalent Circuit

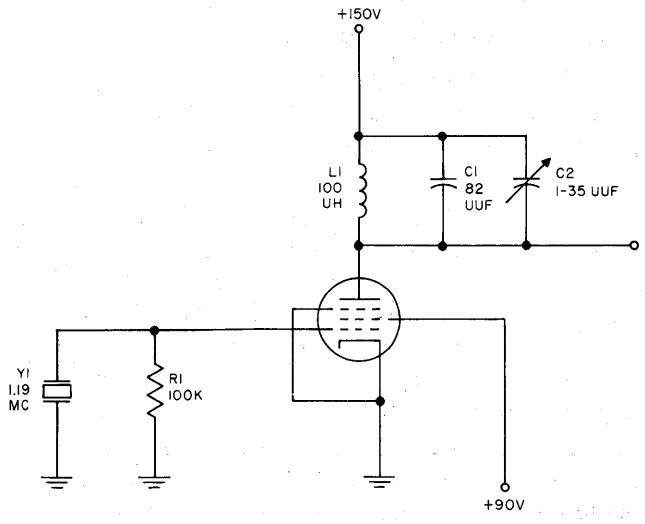


Figure 3–53. Crystal Oscillator, Model D, Schematic Diagram

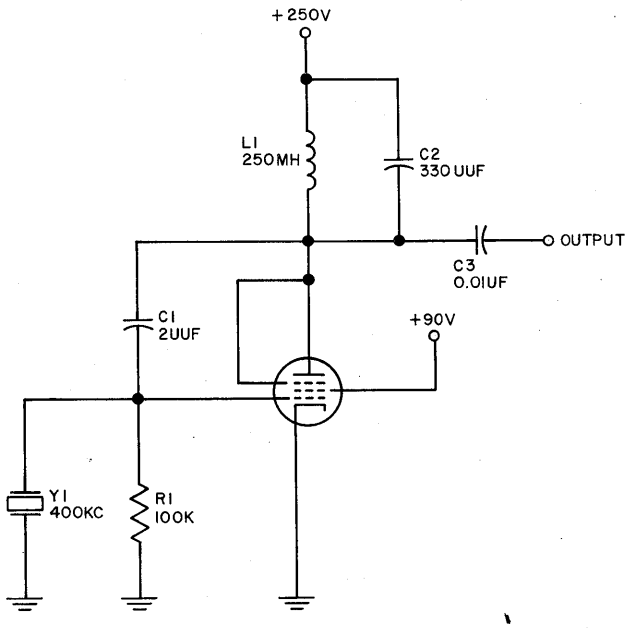


Figure 3–54. Crystal Oscillator, Model E, Schematic Diagram

3.22 CURRENT REGULATOR, MODEL A

3.22.1 Definition and Description

The model A current regulator (ACR) is a logic circuit which functions as a current pulse generator. The logic block symbol for this circuit is shown in figure 3–55. In Central Computer logic, the ACR has two states of operation: not selected and selected. When the ACR is not selected, the input level is at +10V and there is no output. When the ACR is selected, the input level is at −30V and the output is a current pulse of 700 to 800 ma. This current pulse is fed through one of 16 switch drivers to a 16 × 16 core matrix.

3.22.2 Principles of Operation

3.22.2.1 Basic Operation

Figure 3–56, foldout, is the schematic diagram of the ACR. Table 3–30 lists the associated detail parts and their functions.

Output amplifiers V3 and V4 generate a driving pulse of current when the input of the ACR is at −30V. The signal level at the input of amplifier V1A is the difference between this negative level and a positive degenerative voltage fed back from the output amplifier. This circuit arrangement provides added stability to the output signal level.

The negative input is amplified and inverted by input amplifier V1A and fed through two successive cathode followers. The first of these, V1B, serves as a buffer amplifier between V1A and driver cathode follower V2 to minimize the loading on the input amplifier. Cathode

TABLE 3–30. CURRENT REGULATOR, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Speedup capacitor
C2	Part of feedback loop
C3	Coupling capacitor
C4	Bypass capacitor
C5	Tuning capacitor, vary load capacitance of V1B
C6	Coupling capacitor
C7, C8	Bypass capacitors
CR1	Part of input circuit (with R2)
CR2, CR3	Clamping diodes for grid of V1A
CR4, CR5	Clamping diodes for grid of V1B
CR6, CR7	Clamping diodes for grids of V3 and V4
R1	Grid resistor for V1A
R2	Part of input circuit (with CR1)
R3	Current-limiting resistor for CR3
R4	Plate load for V1A
R5, R6	Equalizing resistors
R7, R8	Voltage divider
R9	Cathode resistor for V1B
R10	Common cathode resistor for V2A and V2B
R11, R12	Equalizing resistors
R13, R14	Voltage divider
R15, R16, R17	Part of resistor network for cathodes of V3 and V4 (with R18)
R18	Gain control and part of resistor network for cathodes of V3 and V4 (with R15, R16, and R17)

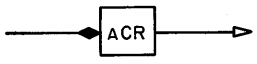


Figure 3–55. Current Regulator, Model A, Logic Block Symbol

follower V1B incorporates a tuning capacitor to vary its load capacitance, providing a means for adjusting the fall time of the positive output pulse. Cathode follower V2 provides the current required to drive output amplifier V3 and V4.

3.22.2.2 Detailed Operation

The input voltage is always either +10V or −30V. With +10V at the plate of CR1, input amplifier V1A conducts, causing its plate to fall to +80V. Grid current through resistor R1 drops grid voltage to cathode or ground level. The grid of V1B is clamped at −50V. The grids of output amplifier V3 and V4 are clamped at −225V by voltage divider R13 and R14. As a result, the output amplifier is biased well beyond cutoff; i.e., cathodes at −150V and grids at −225V.

A shift of input voltage from +10V to −30V results in a fall of V1A grid voltage and a rise of V3 and V4 cathode voltage. This rise of voltage is fed back to the input circuit of V1A through C2. Without feedback, the grid of V1A is clamped at −15V by CR2 and CR3. With an approximately 12V rise fed back, diode CR2 clamps the grid of V1A at −3V. Thus, the shift from a positive to a negative standard level at the input produces a fall from +0.5V to −3V at the grid of V1A. The 3.5V grid voltage change produces a 90V rise in V1A plate voltage to +170V. This 90V rise is coupled through V1B and V2 to the grids of V3 and V4, raising them from −225V to −135V. Output amplifier V3 and V4 conducts and the cathodes rise from −150V to −138V. The output amplifier is connected to B+ through 16 switch drivers (SWD, par. 3.77), and its conduction presupposes the conditioning of one of the 16 SWD's to pass the output current pulse.

3.23 DATA CONVERSION RECEIVERS, MODELS A, B, C, AND D

3.23.1 Definition and Description

The data conversion receivers (DCR) are logic circuits which convert sinusoidal input signals into signals suitable for processing within the Input and Output Systems. Table 3–31 lists the logic block symbols and functions of the four models of the DCR. The principles of operation for the four models are similar; for this reason, only the model ADCR is described in detail. Models B, C, and D are shown schematically, accompanied by tables listing the detail parts and their functions.

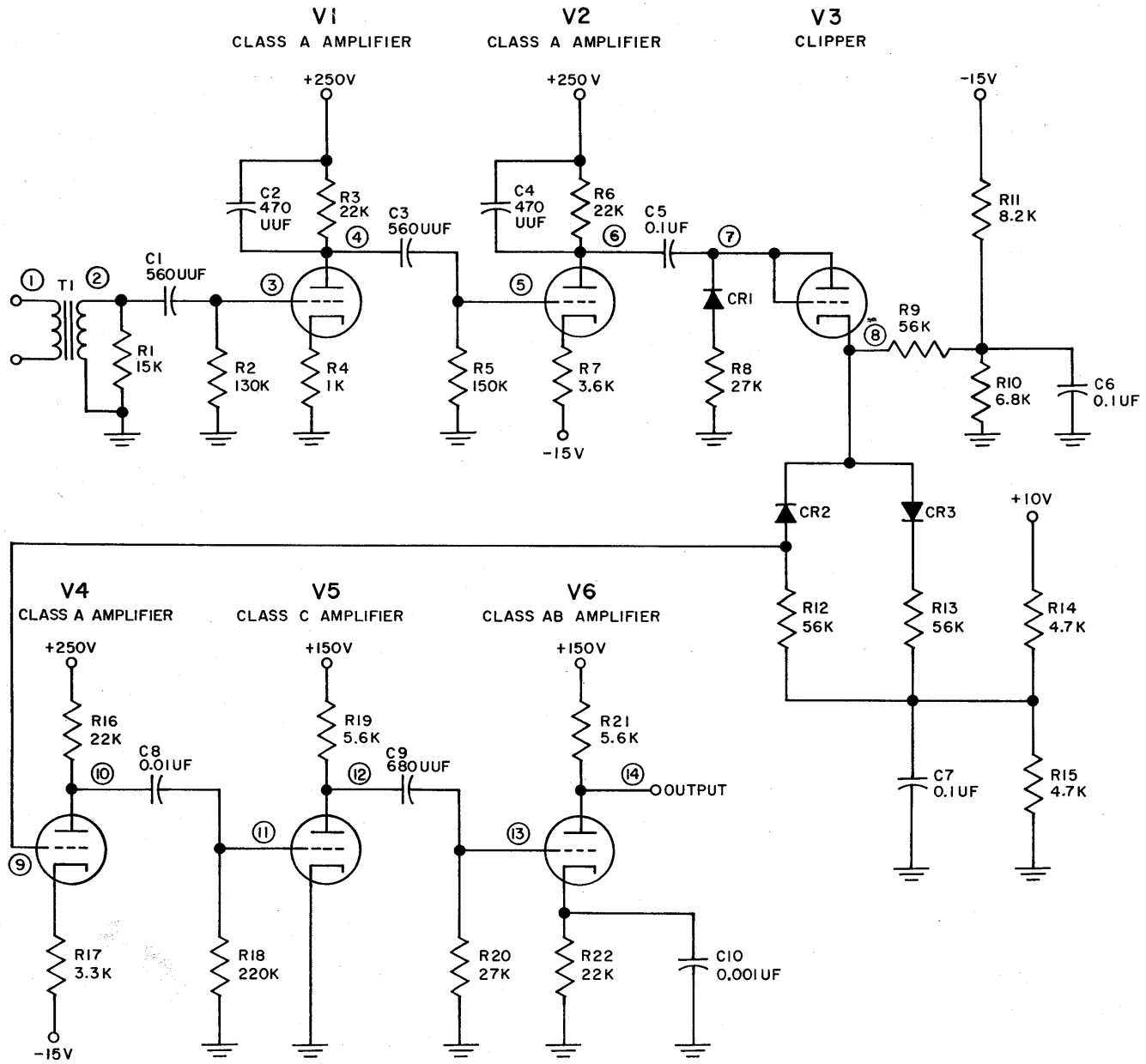
3.23.2 Principles of Operation

Figure 3–57 is the schematic diagram for the ADCR. Table 3–32 lists the associated detail parts and their functions. The ADCR employs three double triodes to convert a 2V sine wave into a narrow, negative 50V pulse. Transformer T1 amplifies the input signal by 5 and is connected to produce an in-phase signal across R1. Capacitor C1 and resistor R2 form the first phase shifting network. The network at the grid of V1 leads the T1 output signal by 48 degrees (see waveform 3, fig. 3–57). The unbypassed cathode resistor R4 of V1 minimizes distortion by providing degenerative feedback. Plate load resistor R3 is shunted by C2 to bypass high-frequency noise generated in the telephone lines feeding the ADCR. The input to V1 is amplified by 3 and coupled to V2 by the second phase shifting circuits consisting of C3 and R5. The signal at the grid of V2 leads the V1 plate signal by 48 degrees. Cathode resistor R7 of V2 being larger than R4 introduces a larger feedback signal and reduces the gain of V2 to 2.6. The negative bias of −15V on the cathode enables V2 to function as a class A amplifier. The 85V output signal of V2 is coupled to V3 by C5.

Tube V3 is a diode-connected triode. The clipping circuit connected to the cathode of V3 provides a square wave input to V4 and operates as follows. The voltage at the junction of R10 and R11 is −7V. At the junctions of R14 and R15, the voltage is +5V. The difference in potential at these points produces a current through R9, CR2, and R12. The resultant voltage at the anode of CR2 is approximately 0V. During the negative half cycles of

TABLE 3–31. DATA CONVERSION RECEIVERS, MODEL-DISTINGUISHING CHARACTERISTICS

MODEL	LOGIC BLOCK SYMBOL	FUNCTION
A	ADCR	To convert a 1,300-cps continuous sine wave into a series of negative pulses at 1,300 pps. Each pulse occurs approximately 90° before the positive-going crossover of the input sine wave.
B	BDCR	To convert the negative half of a single cycle of a 1,300-cps sine wave into a positive standard level shift of 200 μsec duration.
C	CDCR	To produce a series of negative pulses each coincident with the positive-going zero crossover of the 1,300- or 1,600-cps input sine wave.
D	DDCR	To produce a series of standard pulses each occurring 12 μsec before the positive-going zero crossover of the 1,300- or 1,600-cps input sine wave.



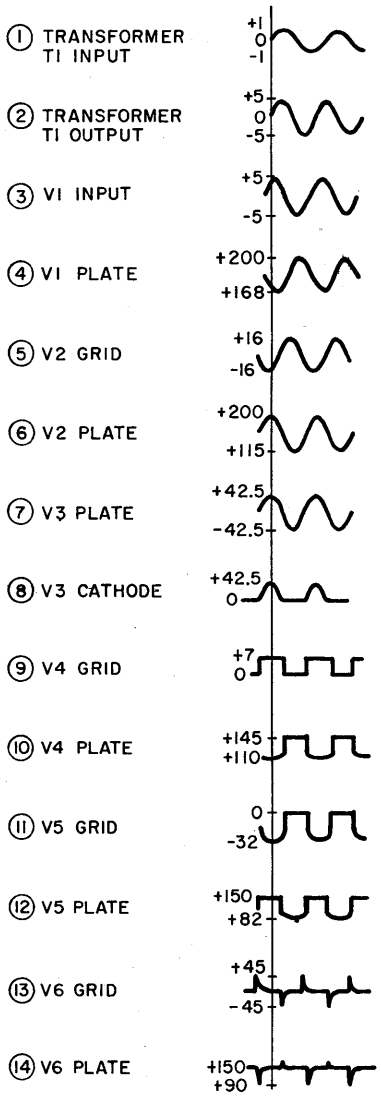


Figure 3–57. Data Conversion Receiver, Model A, Schematic Diagram

signals developed by V2, clipper V3 is cut off and 0V present at the anode of CR3 is applied to V4. Clipper V3 conducts during the positive half cycle of signals developed by V2. The cathode of V3 follows the plate (see waveform 8, fig. 3–57). A 40V forward bias causes CR3 to conduct, dropping 35V across CR3 and R13. Voltage divider action of the back resistance of CR2 and R12 set the anode of CR2 at +7V. Thus, the grid of V4 is fed by a square wave varying between 0 and +7V at 1,300 cps (see waveform 9, fig. 3–57).

Because of the unbypassed cathode resistor, amplifier V4 conducts throughout the entire input cycle. With the application of the 0 to +7V input signal on the grid, the resultant output is a square wave of 35V peak to peak (waveform 10, fig. 3–57) which is coupled by capacitor C8 to the grid of V5.

Tube V5, a class C amplifier, amplifies the square wave output of V4, resulting in a square wave at the plate of V5 (+82V to +150V) which is then differentiated by the network consisting of capacitor C9 and resistor R20. The result is a series of negative and positive pulses appearing at the grid of V6. The amplitude of the spikes is 45V (waveform 13, fig. 3–57).

Tube V6 is the final stage of the ADCR. This tube operates as a class AB amplifier. The positive and negative spikes from V5 are applied to the grid of V6. The tube conducts during the positive spikes and is cut off during the greater portion of the negative spikes. The resultant output of V6 consists of sharp negative-going pulses with an amplitude of 60V and small positive pulses from slightly under +150V. These small positive pulses result from the fact that the tube is self-biased and these pulses have no deleterious effect on the circuit.

An analysis similar to the one presented above can be applied to the models B, C, and D DCR's. Figures 3–58, 3–59, and 3–60, respectively, are the schematic diagrams for the models B, C, and D. Tables 3–32, 3–33, and 3–34 list the associated detail parts and their functions for these models.

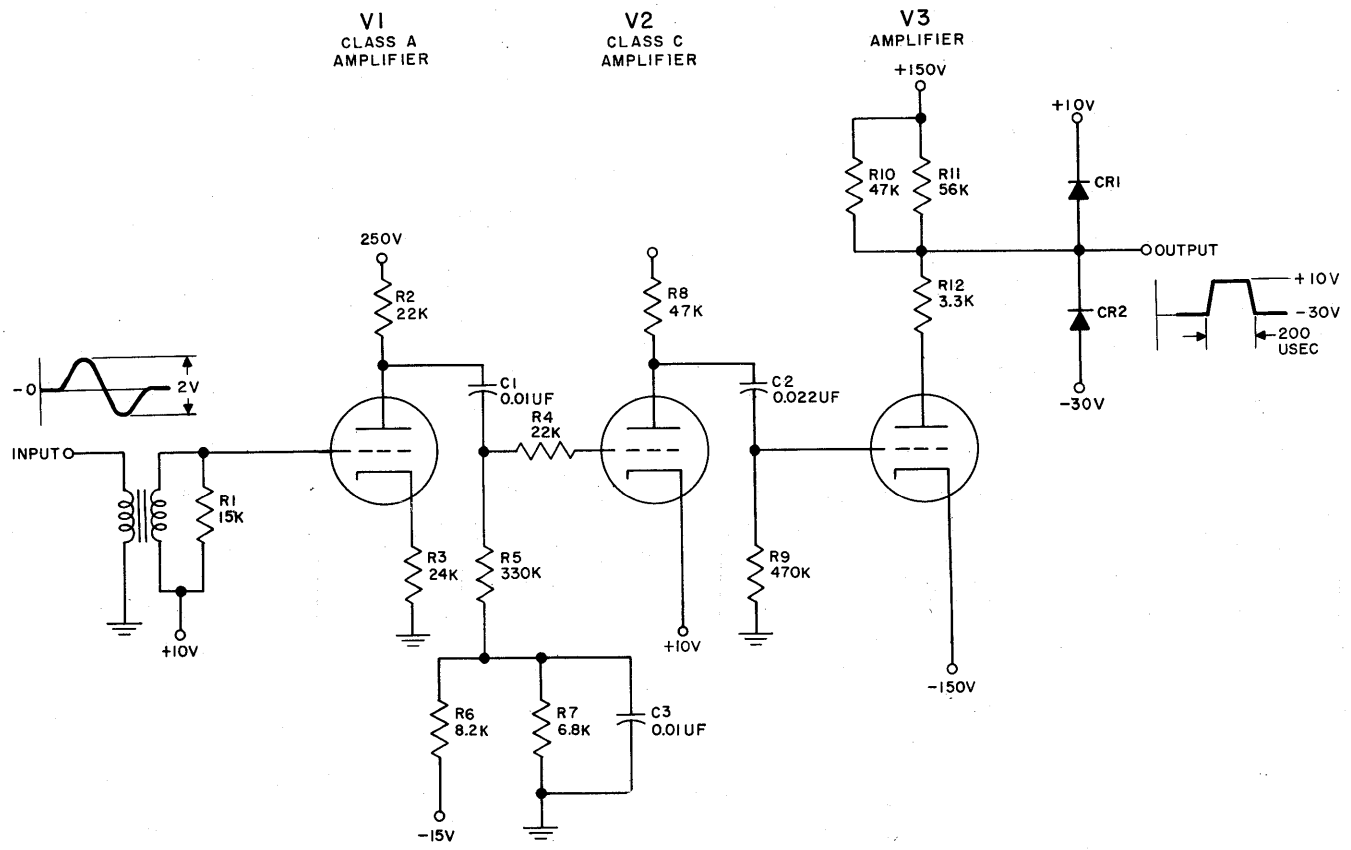


Figure 3–58. Data Conversion Receiver, Model B, Schematic Diagram

TABLE 3–32. DATA CONVERSION RECEIVER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	Shunting resistor	R18	V5 grid leak resistor
R2	Part of 48-degree phase shifting network (with C1) and V1 grid return	R19	V5 plate load resistor
		R20	Part of differentiating network (with C9)
R3	V1 plate load resistor	R21	V6 plate load resistor
R4	V1 cathode resistor	R22	V6 cathode resistor
R5	Part of second 48-degree phase shifting network (with C3), and V2 grid return	C1	Part of phase shifting network (with R2)
R6	V2 plate load resistor	C2	Shunting capacitor
R7	V2 cathode resistor	C3	Coupling capacitor and part of phase shifting network (with R5)
R8	Provides zero references for V3 plate voltage (with CR1)	C4	Shunting capacitor
R9, R10, R11	Voltage divider	C5	Coupling capacitor
R12, R13	Part of clipping network (with CR2 and CR3)	C6	Bypass capacitor
R14, R15	Voltage divider	C7	Bypass capacitor
R16	V4 plate load resistor	C8	Coupling capacitor
R17	V4 cathode resistor	C9	Coupling capacitor and part of differentiating network (with R20)
		C10	Bypass capacitor

TABLE 3–33. DATA CONVERSION RECEIVER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	Impedance-matching resistor	R9	Part of RC coupling network (with C2)
R2	V1 plate load resistor	R10, R11, R12	V3 plate load resistors
R3	V1 cathode resistor	CR1	Crystal diode; +10V clamp
R4	V2 grid current limiting resistor and part of RC coupling network (with C1 and R5)	CR2	Crystal diode; —30V clamp
		C1	Part of RC coupling network (with R4 and R5)
R5	Part of RC coupling network (with C1, R4)	C2	Part of RC coupling network (with R9)
R6, R7	Voltage divider		
R8	V2 plate load resistor	C3	Bypass capacitor

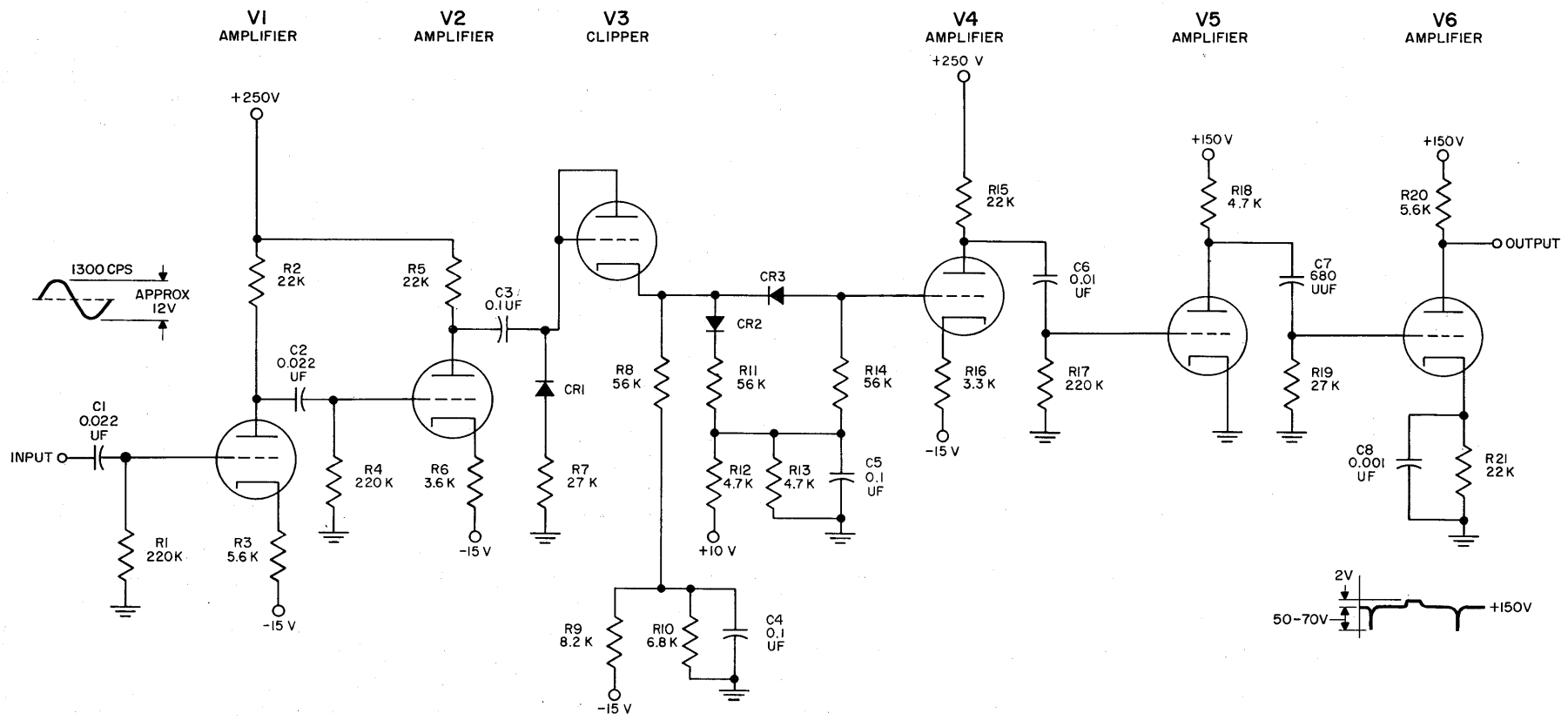


Figure 3—59. Data Conversion Receiver, Model C (Zero Detector), Schematic Diagram

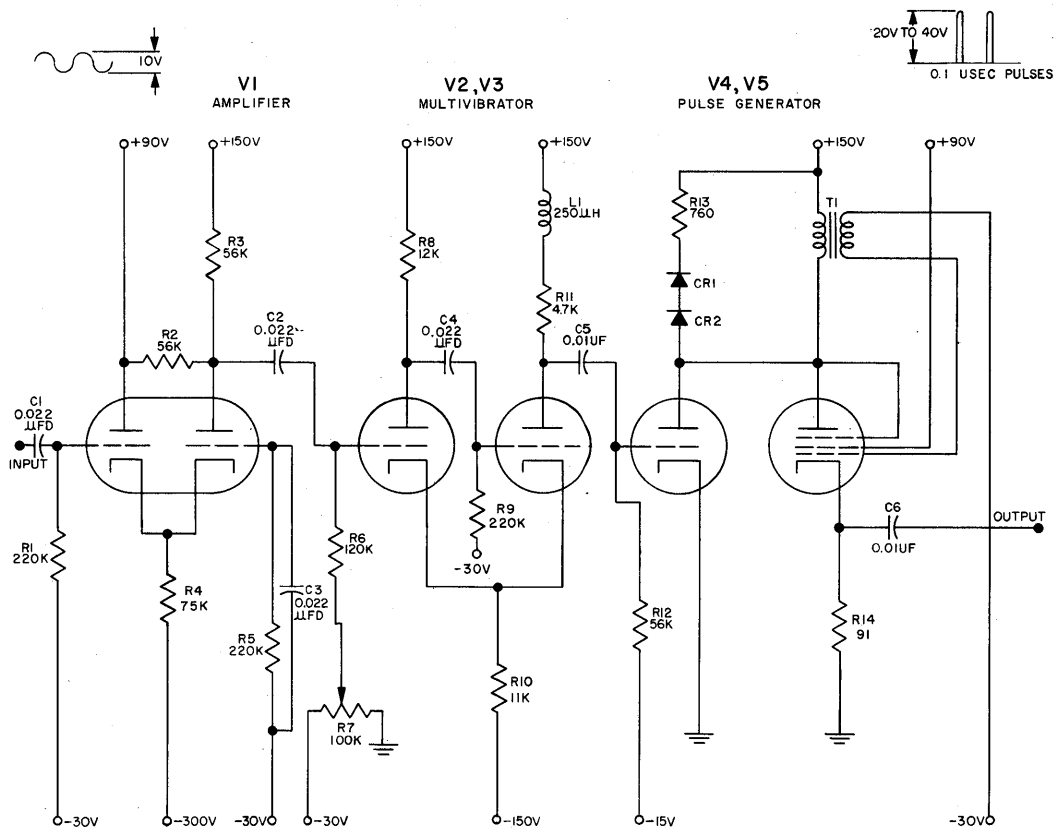


Figure 3–60. Data Conversion Receiver, Model D, Schematic Diagram

TABLE 3–34. DATA CONVERSION RECEIVER, MODEL C (ZERO DETECTOR), FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	V1 grid return	R20	V6 plate load resistor
R2	V1 plate load resistor	R21	V6 cathode resistor
R3	V1 cathode resistor	CR1, CR2, CR3	Part of clipping and clamping network (with R7-R14)
R4	Part of RC coupling network (with C2) and V2 grid return	C1	Coupling capacitor
R5	V2 plate load resistor	C2	Part of RC coupling network (with R4)
R6	V2 cathode resistor	C3	Coupling capacitor
R7-R14	Part of clipping and clamping network (with CR1, CR2, and CR3)	C4	Bypass capacitor
R15	V4 plate load resistor	C5	Bypass capacitor
R16	V4 cathode resistor	C6	Part of RC coupling network (with R17)
R17	Part of RC coupling network (with C6) and V5 grid return	C7	Part of RC coupling network (with R19)
R18	V5 plate load resistor	C8	Bypass capacitor
R19	Part of RC coupling network (with C7) and V6 grid return		

TABLE 3–35. DATA CONVERSION RECEIVER, MODEL D, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	V1A grid resistor	R13	Part of clamping circuit in T1 primary (with CR1, CR2)
R2, R3	Voltage divider in V1 plate circuit	R14	V5 cathode resistor
R4	V1 cathode resistor	CR1, CR2	Part of clamping circuit in T1, primary
R5	V1B grid resistor	C1	Input coupling capacitor
R6, R7	Part of RC coupling network and V2 grid return (with C2)	C2	Part of RC coupling network (with R6, R7)
R8	V2 plate load resistor	C3	Bypass capacitor
R9	Part of RC coupling network (with C4) and V3 grid return	C4	Part of RC coupling network (with R9)
R10	V2, V3, common cathode resistor	C5	Part of RC coupling network (with R12)
R11	V3 plate load resistor	C6	Output coupling capacitor
R12	Part of RC coupling network (with C5) and V4 grid return		

3.24 DECODER SIMULATORS

3.24.1 Definition and Description

The decoder simulator (DCS) is a nonlogic circuit which provides a compensated reference voltage for the output of the 10-bit binary decoder. The logic block symbol for the DCS is shown in figure 3–61. Two models of the DCS (models B and C) are employed in the AN/FSQ-7 and -8 equipments. Both circuits are identical except for variations in the values of several of the detail parts in the model cDCS. Therefore, only the model B is discussed in detail.

3.24.2 Principles of Operation

3.24.2.1 Basic Operation

Figure 3–62 is the schematic diagram of the BDCS. Table 3–36 lists the associated detail parts and their functions. Two identical decoder simulators (BDCS's) are employed with the 10-bit binary decoder; one for X-axis positioning (BDCS(X)) and the other for Y-axis positioning (BDCS(Y)). Only the X-axis positioning DCS is discussed below.

The BDCS is similar to the output stage of the 10-bit binary decoder, consisting of a constant current tube (V2)

TABLE 3–36. DECODER SIMULATOR, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	Grid-limiting resistor	R8	Part of X-axis gain control network (with R6, R7, R9)
R2	Grid-limiting resistor	R9	Part of X-axis gain control network (with R6, R7, R8)
R3	Part of mu-metal shield compensation network (with C3 and R4)	R10	Cathode resistor for V2
R4	Part of mu-metal shield compensation network (with C3 and R3)	R11	X-axis centering potentiometer
R5	Plate load for V1	C1	Grid bypass for V1
R6	Part of X-axis gain control network (with R7, R8, R9)	C2	Grid bypass for V2
R7	Part of X-axis gain control network (with R6, R8, R9)	C3	Part of mu-metal shield compensation network (with R3 and R4)
		C4	Cathode bypass for V2

and a gate tube (V1). The grid of V1 is returned to —10V; the plate is connected to +150V through a load that is the equivalent of the decoder output LS. The grid of V2 is returned to —162V and the cathode is returned to —300V. These identical reference voltages are employed by the 10-bit binary decoder. Fluctuations appearing in any of these voltages cause the BDCS(X) output of the plate of V1 to change. This change in potential at point D compensates for an equivalent change in the 10-bit binary decoder output (point A), maintaining the correct difference in potential between terminals E and F for a given positioning address (decoder input). The differential output (E-F) is applied to the deflection amplifier, representing a message position along the X-axis on the face of the SD CRT.

3.24.2.2 Detailed Operation

Assume that the X-axis gain control is adjusted for maximum output; that is, the wiper arm of R6 is set at point C and the wiper arm of R9 is set at point D. Let the input from the 10-bit binary decoder equal 25V (voltage at terminal A equals +125V). This voltage represents the center position on the X axis of the SD CRT. In order for the message to be positioned in the center, the voltage difference between terminals E and F must be 0. This is accomplished by the adjustment of the X-axis center control, R11, which adjusts the plate voltage of V1. Assume that R13 is adjusted so that the decoder simulator output (reference voltage for decoder output) is +125V.

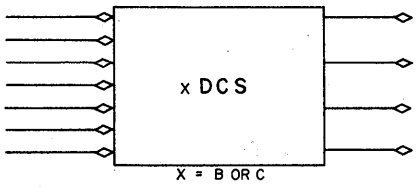


Figure 3–61. Decoder Simulators, Logic Block Symbol

Now, if the common +150V plate supply (terminal B) for V1 and the decoder gate tubes were to decrease to +148V, the voltage at terminal A (and E) would fall to +123V. Since a small change in the plate supply voltage of a tube has a negligible effect on plate current, this voltage change is reflected at the plate of the tube. Therefore, the plate voltage of V1 falls 2V to +123V. Thus, the difference in potential between terminals E and F remains at 0. If the —10V supply becomes more negative, it causes the output of the 10-bit binary decoder (terminal E) to increase; this same grid voltage change causes the plate potential of V1 to become more positive by the same amount. Once again the difference in potential between the decoder and decoder simulator output remains equal to 0. Since common reference voltages are used in the 10-bit binary decoder and the decoder simulator, variations in these voltages are compensated for by the output variations of the BDCS(X). Thus, for a given message

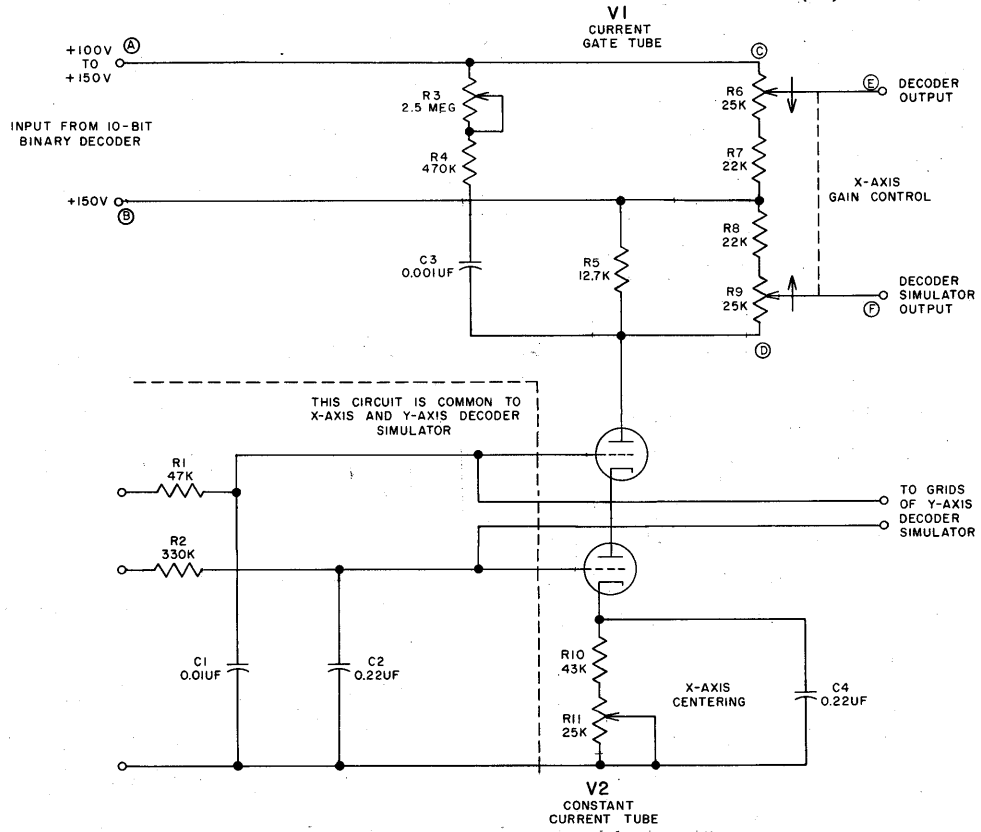


Figure 3–62. Decoder Simulator, Model B, X-Axis Portion, Schematic Diagram

position, the differential voltage applied to the deflection amplifier remains at a constant value regardless of reference voltage variations. The magnitude of this voltage is determined by the X-axis gain control, consisting of ganged potentiometers R8 and R11.

3.24.2.3 Circuit Refinements

Included in the BDCS(X) is a long time constant RC network used to compensate for the nonlinearities introduced into the magnetic deflection circuit by the mu-metal shield. The 10-bit binary decoder output is modified so that an exponential waveshape rather than a rectangular pulse is applied to the deflection amplifier. In this manner, the deflection field of the SD CRT stabilizes at the desired level within the required 30 μsec.

3.25 DEFLECTION AMPLIFIER, DISPLAY SYSTEM

3.25.1 Definition and Description

The Display System deflection amplifier (DA) is a nonlogic circuit used to amplify the analog outputs of the 10-bit binary decoder. These amplified outputs are applied to the deflection driver as push-pull voltages; the deflection driver provides the SD CRT deflection yoke with message-positioning currents. The logic block symbol for the DA is shown in figure 3–63.

The DA consists of two direct-coupled high-gain differential amplifiers, one for horizontal (X-axis) positioning and the other for vertical (Y-axis) positioning. Since the two amplifiers are identical, only the deflection amplifier for X-axis positioning is discussed.

3.25.2 Principles of Operation

3.25.2.1 Basic Operation

Figure 3–64, foldout, is the schematic diagram for the DA. Table 3–37 lists the associated detail parts and their functions.

The first stage of the DA is a differential amplifier consisting of V1A and V1B. The inputs to V1A, obtained from the 10-bit binary decoder, are analog levels that represent the message format position along the X-axis on the face of the SD CRT. These inputs

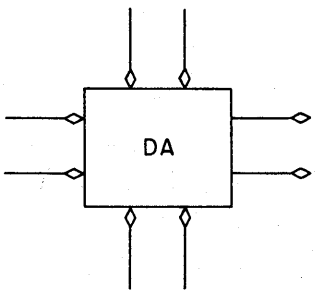


Figure 3–63. Deflection Amplifier, Display System, Logic Block Symbol

are any one of 1,024 discrete levels (par 3.7) between +100 and +150V. The input to V1B is supplied by the decoder simulator (par. 3.24); this voltage is employed as a compensated reference voltage for the differential input to the DA. In addition to the inputs that comprise the differential input, a large amount of degenerative feedback from the deflection driver is fed to the DA. This feedback ensures a linear relationship between the analog output of the 10-bit binary decoder and the output of the deflection driver.

The amplified output of the first stage is a pair of balanced levels which are direct-coupled through two stages of push-pull amplification, V2-V3 and V4-V5, respectively. The push-pull output of the final stage is applied to the deflection driver. Without degenerative feedback, the open loop gain of the DA is approximately 3,000; however, with the inclusion of the degenerative feedback loop, the gain is reduced to approximately 3.7.

3.25.2.2 Detailed Operation

A detailed discussion of the DA in terms of X-axis center positioning and X-axis off-center deflection follows; X-axis center positioning (quiescent state of the DA) is discussed first.

Assume that the input to triode V1A, generated by the 10-bit binary decoder, equals +125V. This analog voltage corresponds to a message position at the center of the X-axis. Assume that the input to V1B, supplied by the decoder simulator, equals +125V. This input represents the compensated reference voltage for the differential input to the DA. The cathodes of V1A and V1B are returned to the plate of constant current tube V6A. Cathode degeneration maintains the plate current of V6A at a relatively constant value; the magnitude of this current is adjusted with potentiometer R30. The setting of this variable resistor establishes the bias level for V6A and is maintained at a constant value by the action of voltage regulator V7. As a result of the equal potentials on the grids of V1A and V1B, the plate current of V6A is equally divided between these two triodes.

The resultant plate potential of V1A and V1B during quiescence is +130V. With +130V at the plate of V1A, 430V appears across the voltage divider comprised of resistors R10 and R12. As a result of voltage division, −55V also appears at the control grid of V3 due to the voltage division performed by resistors R11 and R13. The cathodes of V2 and V3 are returned to constant current tube V6B. The bias level for V6B, as for V6A, is determined by the setting of R30. Since the control grid voltages of both V2 and V3 are equal, the plate current of V6B is equally divided between V2 and V3.

As a consequence of the equal plate currents, the plate voltages of V2 and V3 are both equal to +105V. A potential of 405V exists across two identical dividers,

one consisting of resistors R19 and R21 and the other consisting of R20 and R22. The voltage division performed by these voltage dividers is the same, and therefore the potentials at the control grids of V4 and V5 both equal —146V. Since pentodes V4 and V5 employ a common cathode resistor (R27) and their grid voltages are equal, the plate currents of V4 and V5 are equal. The resultant plate voltages of V4 and V5 equal +40V.

The output of the DA is the difference in potential that exists between the plates of V4 and V5. Since both plates are at the same potential in the above discussion, the output is zero. This output represents a message position at the center of the X-axis on the face of the SD CRT.

Assume now that the voltage applied to the control grid of V1A is increased. This analog input represents a message position displaced from the X-axis center. This increase in grid voltage results in an increase in plate current and a resultant decrease in the plate voltage of V1A. The input to V1B is still maintained at its quiescent level of +125V. Since the plate current for both V1A and V1B is supplied by a common constant current source (V6A), the plate current of V1B decreases by an amount equal to the increase in plate current by V1A.

TABLE 3—37. DEFLECTION AMPLIFIER, DISPLAY SYSTEM, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of stabilization network (with R9)
C2, C3	Speedup capacitors, improve rise and fall time
C4	Part of stabilization network (with R18)
C5, C6	Speedup capacitors, improve rise and fall time
C7	Stabilization capacitor
C8	Bypass capacitor
R1, R2	Part of voltage divider network (with R5)
R3, R4	Part of voltage divider network (with R6)
R5	Part of voltage divider networks (with R1 or R2)
R6	Part of voltage divider networks (with R3 or R4)
R7, R8	Plate load resistors for V1A and V1B, respectively
R9	Part of stabilization network (with C1)
R10	Part of voltage divider network (with R12)
R11	Part of voltage divider network (with R13)
R12	Part of voltage divider network (with R10)
R13	Part of voltage divider network (with R11)
R14	Plate load resistor for V2
R15, R16	Cathode resistors for V2 and V3, respectively; improve linearity
R17	Plate load resistor for V3
R18	Part of stabilization network (with C4)
R19	Part of voltage divider network (with R21)
R20	Part of voltage divider network (with R22)
R21	Part of voltage divider network (with R19)
R22	Part of voltage divider network (with R20)
R23	Plate load resistor for V4
R24, R25	Cathode resistors for V4 and V5, respectively; improve linearity
R26	Plate load resistor for V5
R27	Common cathode resistor for V4 and V5
R28	Cathode resistor for V6A
R29	Part of voltage divider network (with R30 and R31)
R30	Bias-setting potentiometer for V6A and V6B
R31	Part of voltage divider network (with R29 and R30)
R32	Cathode resistor for V6B

This results in a rise in the plate voltage of V1B that equals the decrease in V1A plate potential.

The voltage divider comprised of R10 and R12 establishes a coupling ratio of 57 percent between V1A and V2; therefore, only this percentage of the decrease in the plate voltage of V1A is coupled to the control grid of V2. The plate current of V2 decreases, causing the plate potential of V2 to increase. Since an identical coupling arrangement is used between V1B and V3, 57 percent of the increase in the plate potential of V1B is coupled to V3. The resulting decrease in the plate voltage of V3 equals the rise in plate potential of V2.

The coupling ratio employed between V2 and V4 and V3 and V5 is 38 percent. This ratio is established by identical voltage dividers used between the respective stages. As a result of the voltages appearing at the control grids, the plate potential of V4 decreases and the plate potential of V5 increases.

The difference in potential between the plates of V4 and V5 represents a message position along the X axis on the face of the SD CRT. The magnitude of this voltage determines the displacement of the message from the X-axis center; the polarity determines the direction. The push-pull output of the DA is applied to the X-axis deflection driver. Refer to table 3–37 for the function of detail parts not discussed.

3.26 DEFLECTION AMPLIFIER, INPUT SYSTEM

3.26.1 Definition and Description

The Input System deflection amplifier (DA) is a nonlogic circuit employed to provide current to the deflection yoke of the LRI monitor. The inputs to the DA are analog voltages that represent X-Y co-ordinates of a target to be positioned on the screen of the LRI monitor. These inputs are supplied by the distribution power amplifier. The logic block symbol for the DA is shown in figure 3–65.

The DA consists of two direct-coupled negative feedback amplifiers, one for horizontal (X-axis) positioning and the other for vertical (Y-axis) positioning. Since the two amplifiers are identical, only the amplifier for X-axis positioning is discussed.

3.26.2 Principles of Operation

3.26.2.1 Basic Operation

Figure 3–66 is the schematic diagram for the DA; table 3–38 lists the associated detail parts and their functions.

The input stage of the DA is a differential amplifier consisting of triodes V1A and V1B. The input to V1A is an analog voltage that represents the X-axis displacement of an LRI target; this input will be at any one of a number of discrete levels between +26 and −26V. The signal applied to V1B is a portion of the DA output. This voltage is employed as the reference voltage for the differential input. In addition, the input to V1B serves as degenerative feedback to maintain a linear relationship between the analog input and the current supplied to the deflection coil.

The differential output of the input stage is direct-coupled to the cathode follower consisting of triodes V2A and V2B connected in parallel. This stage effects a match between the positive level of the plate of V1A and the negative level at the grid of high gain pentode

TABLE 3–38. DEFLECTION AMPLIFIER, INPUT SYSTEM, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of high-frequency bypass network (with R7)
C2	Part of high-frequency bypass network (with R10)
C3	Coupling capacitor for degenerative feedback from screen grid to cathode for V4, V5, and V6
F1	Fuse for deflection coil
I1	Blown-fuse indicator
R1, R2	Grid return resistors for V1A and V1B, respectively
R3	Plate load resistor for V1A
R4	Cathode resistor for V1B
R5	Common cathode resistor for V1A and V1B (with R6)
R6	Centering control
R7	Part of high-frequency bypass network (with C1)
R8	Cathode resistor for V2A and V2B
R9	Plate load resistor for V3
R10	Part of high-frequency bypass network (with C2)
R11	Common cathode resistor for V4, V5, and V6
R12	Screen-dropping resistor for V4, V5, and V6
R13	Current-limiting resistor for I1
R14	Gain control
R15	Part of voltage divider (with R14 and deflection coil)

amplifier V3. The output of V3 is direct-coupled to the output cathode follower stage comprised of three pentode power amplifiers (V4, V5, and V6) connected in parallel. The power amplifiers are placed in parallel to meet the current requirements of the deflection coil. In addition to power amplification, these tubes serve as constant current devices; that is, maintaining the current supplied to the deflection coil at a constant level for a given amount of X-axis displacement.

The output of the DA is applied through a fuse and phone jack to the deflection coil. The phone jack provides a convenient test point to measure deflection coil current. The output current is of the same polarity as the input voltage and proportional to its amplitude.

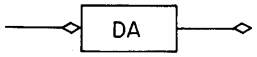


Figure 3–65. Deflection Amplifier, Input System, Logic Block Symbol

3.26.2.2 Detailed Operation

The analog voltage obtained from the distribution power amplifier is applied to the grid of V1A. The signal at the grid of V1B is a percentage of the DA output voltage that appears across the voltage divider consisting of

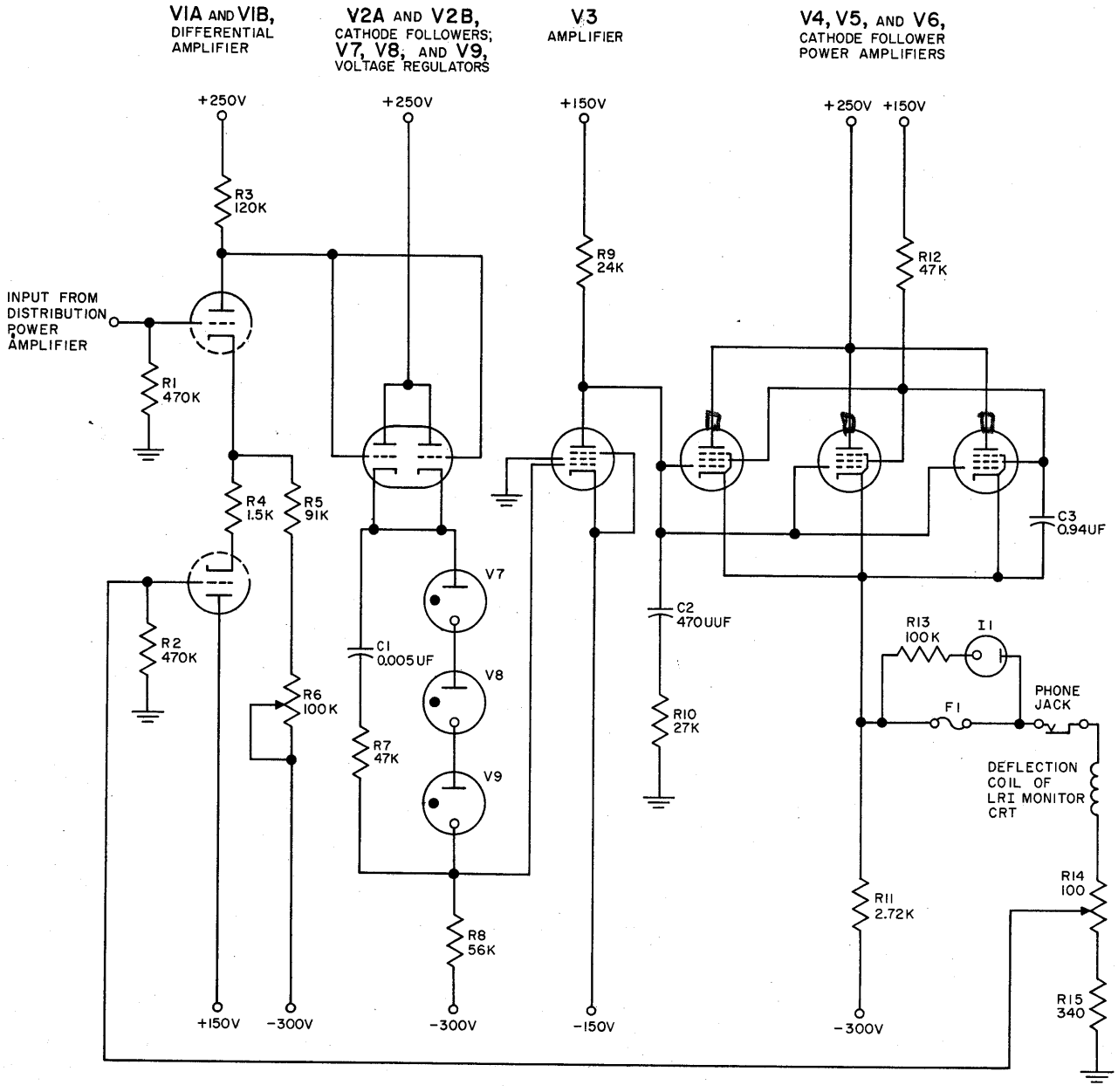


Figure 3–66. Deflection Amplifier, Input System, Schematic Diagram

R14, R15, and the d-c resistance of the deflection coil. Since the polarity of the output is the same as that of the input, the voltage at the grid of V1B is of the same polarity, but smaller in magnitude, as the grid voltage of V1A. The cathodes of the differential amplifier (V1A and V1B) are returned to —300V through a common return consisting of R5 and R6. Therefore, the output of the differential amplifier is a function of the grid voltages appearing at both V1A and V1B. In effect, the voltage difference between the two grids is amplified in the plate circuit of V1A. Since current is diverted from V1A through V1B, the input to V1B functions as degenerative feedback in addition to establishing the reference for the differential input. The setting of potentiometer R14 determines the amount of feedback and therefore is established as the gain control. Potentiometer R6 is used to establish a zero reference (centering) with no input to the DA.

The output of V1A is direct-coupled to the cathode follower comprised of V2A and V2B connected in parallel. The cathodes of this stage are maintained at a constant positive potential through the action of three series-connected voltage regulator tubes (V7, V8, and V9). The cathode follower effects a match between the positive level of the plate of V1A and the negative level at the grid of V3. In effect, this stage acts as a voltage divider between the plate potential of V1A and —300V. The voltage developed across resistor R8 (the output of V2A-V2B) is direct-coupled to high gain pentode amplifier V3. The cathode and suppressor grid are returned to —150V. Returning the cathode to —150V enables the plate potential to be reduced sufficiently to serve as the control grid voltage for the succeeding output stage.

The output cathode follower stage consists of three power amplifiers (pentodes V4, V5, and V6) connected in parallel. Degenerative feedback, screen grid to cathode through capacitor C3, is employed to ensure stable operation at the output stage. The output, a constant current proportional to the analog input, is fed through fuse F1 and a phone jack (test point for an ammeter) to the deflection coil. The fuse is paralleled by neon light I1 that is employed as a blown-fuse indicator. Refer to table 3—38 for the function of detail parts not discussed.

3.27 DEFLECTION DRIVER

3.27.1 Definition and Description

The deflection driver (DEF) is a nonlogic circuit which provides current to the deflection yoke of the SD CRT for message format positioning. The logic block symbol for the DEF is shown in figure 3—67.

Two identical deflection drivers are employed in situation display, one for horizontal (X-axis) positioning and the other for vertical (Y-axis) positioning. The X-axis deflection driver is discussed below.

3.27.2 Principles of Operation

3.27.2.1 Basic Operation

Figure 3—68 is the schematic diagram for the DEF. Table 3—39 lists the associated detail parts and their functions. The circuit consists of a push-pull cathode follower circuit (V1A, V1B) and a push-pull power amplifier circuit (V2A, V2B).

The input to the DEF is a push-pull analog voltage that represents an X-axis displacement. The outputs of cathode followers V1A and V1B are directly coupled to the grids of V2A and V2B, respectively. The plates of V2A and V2B are connected directly to the X-axis deflection coils; the center of these coils is returned to +600V. The output of the DEF provides the SD yoke with the X-axis deflection currents. As a result of these currents, the yoke develops a magnetic field that positions the message on the face of the SD CRT. The strength of the field (flux density) is proportional to the current through the yoke. A linear relationship is established between the analog input voltage to the deflection amplifier and the resultant current output of the driver. This is accomplished by a degenerative feedback loop from the cathode of the driver to the input of the deflection amplifier.

3.27.2.2 Detailed Operation

The operation of the DEF for X-axis center positioning is discussed first.

TABLE 3—39. DEFLECTION DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Grid return for V1A and V1B, respectively
R3, R4	Cathode resistors for V1A and V1B, respectively
R5	Part of selective compensation RC network (with C1, C2, C3, and S1)
R6, R7	Cathode resistor for V2A and V2B, respectively
R8, R9	Damping network for one deflection coil
R10, R11	Damping network for other deflection coil
C1, C2, C3	Part of selective compensation RC network (with R5, S1)
S1	Selection switch for compensation network

When the message is positioned at the center of the face of the SD CRT, the voltages appearing at the grids of V1A and V1B are equal in amplitude and of the same polarity. The plate current of V1A is equal to that of V1B, developing equal potentials across the cathode resistors (R3 and R4, respectively). The output of V1A is directly coupled to the grid of V2A and V1B is directly coupled to the grid of V2B. Since these voltages are equal, the plate currents of V2A and V2B are equal. These currents are then fed to the X-axis deflection coils connected to each plate. Equal currents through the X-axis deflection coils result in a flux distribution which positions the electron beam in the center of the X-axis.

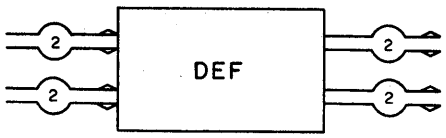


Figure 3-67. Deflection Driver, Logic Block Symbol

For X-axis off center positioning, the DEF operates in the following manner. Assume that the potential appearing on the control grid of V1A has increased. Since this voltage is obtained from the push-pull output of the deflection amplifier, the potential on the grid of V1B will decrease by an equal amount. The increased potential on the grid of V1A causes the plate current of V1A to increase, resulting in an increased voltage across cathode resistor R3. Simultaneously, the potential across cathode resistor R4 of V1B is decreased, due to the reduced voltage on the grid of this tube. The increase in voltage across R3 is directly coupled to the control grid of V2A, causing the plate current of this power amplifier to increase. The reduced output voltage of V1B, which is directly coupled to the grid of V2B, causes the plate current of V2B to be reduced an equal amount. This current unbalance through the X-axis deflection coils results in a flux distribution which deflects the electron beam away from the center.

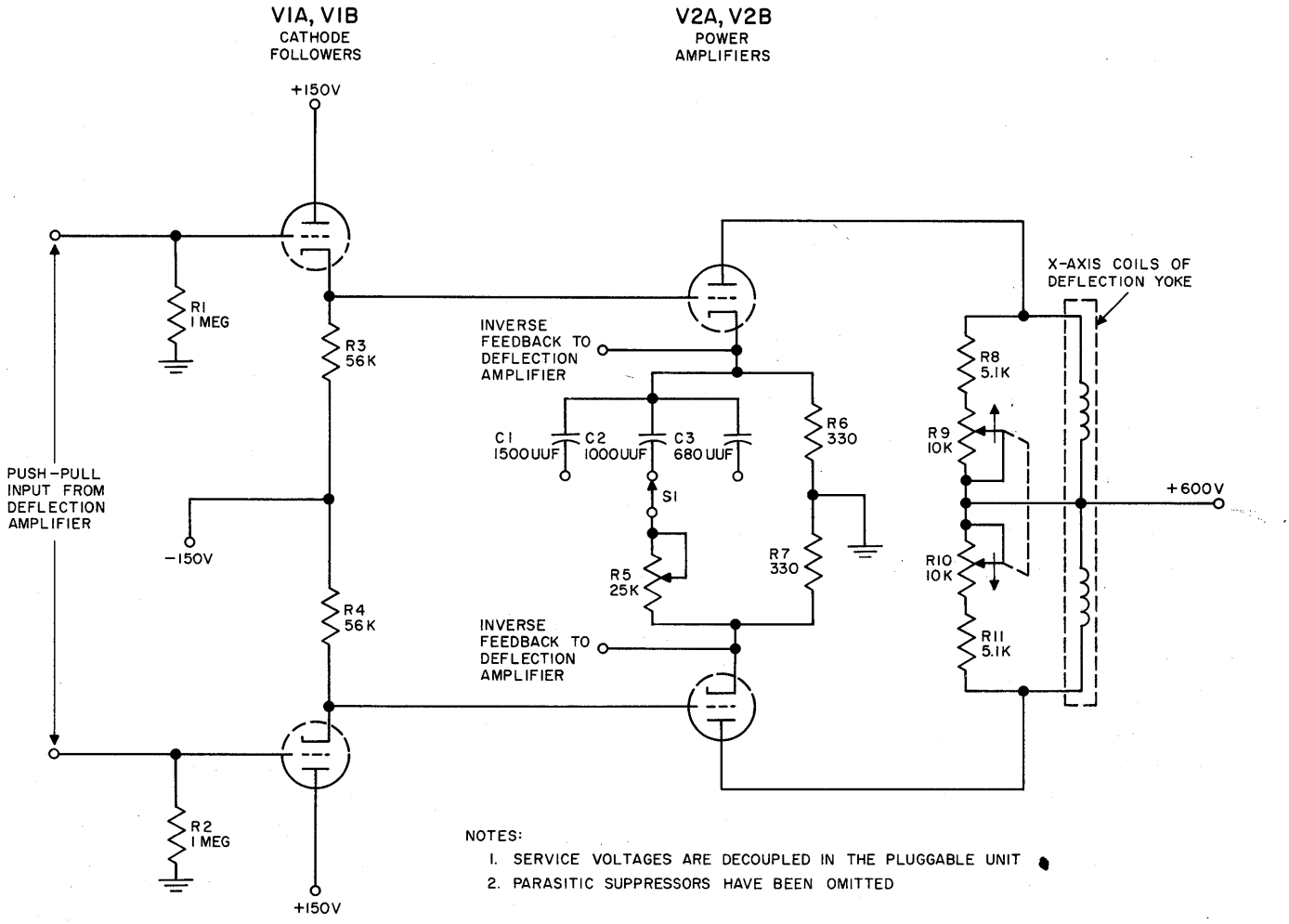


Figure 3-68. Deflection Driver, X-Axis Portion, Schematic Diagram

3.27.2.3 Circuit Refinements

Compensation for the nonlinear characteristics unique to the magnetic deflection circuit is accomplished by several circuit refinements to the DEF. An RC network is connected between the cathodes of V2A and V2B which compensates for any lag in flux response that may occur. Since the cathode resistors of V2A and V2B are not bypassed, cathode degeneration is introduced. Capacitor C2, which is part of the RC network mentioned, maintains the cathode at a constant potential during the transition time, preventing cathode degeneration and resulting in added gain during this time. This increased current gain during rise and fall time effects a speed-up in current rise and current fall. The flux density (upon which deflection is dependent) is directly proportional to this current. The overall result of this compensation will be a resultant flux level of the correct value, which will be reached within 30 μsec, as compared to the 120 μsec without compensation. Because a wide range of compensation is required, the RC network employed is of a selective nature, consisting of three capacitors (C1, C2, and C3), a selection switch (S1), and a variable resistor (R5).

Yoke ringing is prevented by damping resistors R8 and R9 across one-half of the deflection coil and R10 and R11 across the other half. R9 and R10 are variable resistors which are ganged to maintain the same resistance-inductance ratio in both halves of the deflection coil.

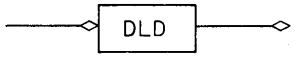


Figure 3–69. Digital Line Driver, Logic Block Symbol

3.28 DIGITAL LINE DRIVER

3.28.1 Definition and Description

The digital line driver (DLD) is a nonlogic circuit which provides power amplification. The logic block symbol for the DLD is shown in figure 3–69. In Input System logic, the DLD is employed to drive a test bus with either continuous sine waves (timing signals) or gated sine wave cycles (information bits).

3.28.2 Principles of Operation

Figure 3–70 is the schematic diagram of the DLD. Table 3–40 lists the associated detail parts and their functions. The circuit consists of a cathode follower and associated input and output impedance-matching transformers.

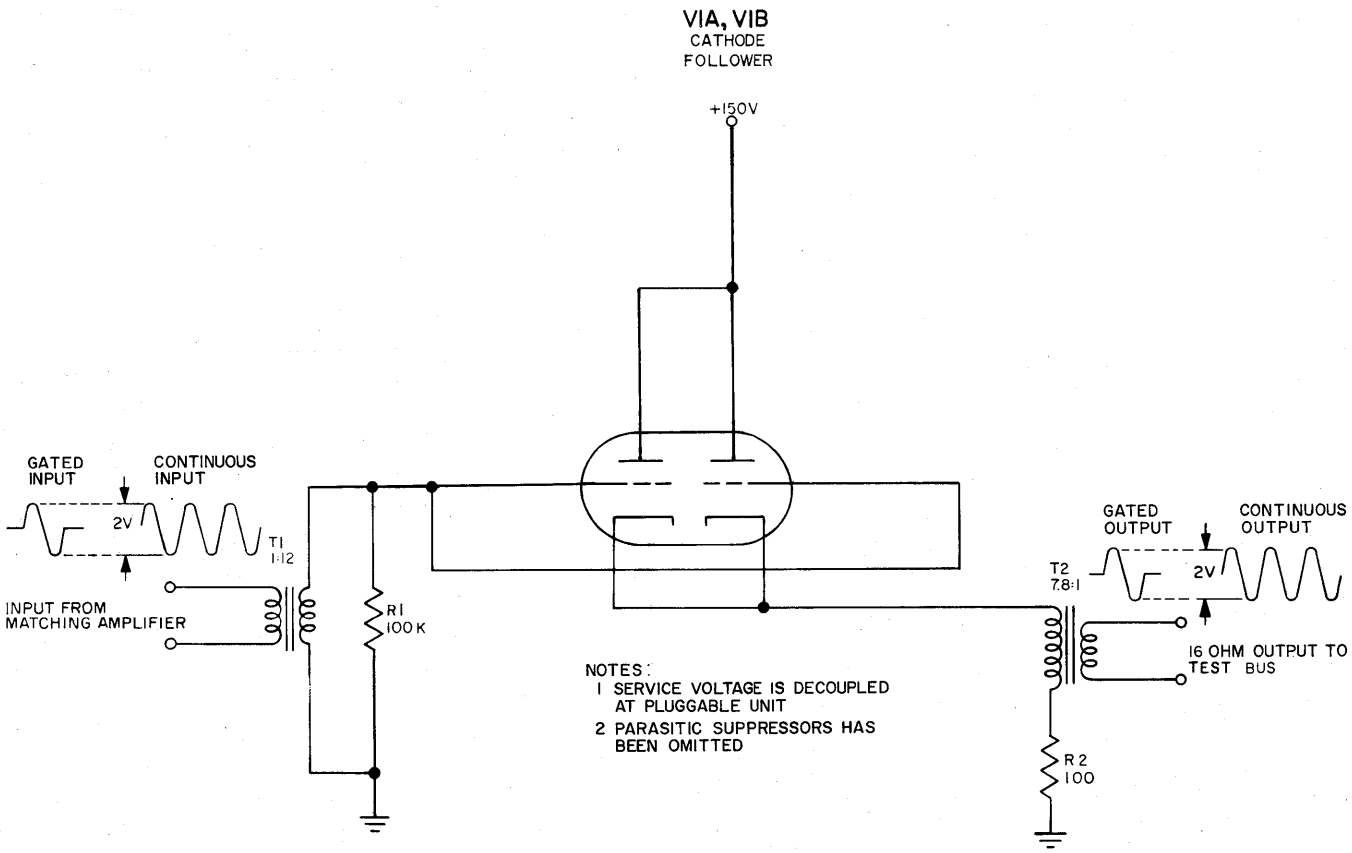


Figure 3–70. Digital Line Driver, Schematic Diagram

The input signal, which is either a continuous sine wave or a gated sine wave cycle, is coupled by input transformer T1 to the grids of the cathode follower. The signal power is amplified by the cathode follower and is developed across the primary of output transformer T2. This transformer provides a 16-ohm impedance in order to match the DLD output to the impedance of the test bus.

TABLE 3–40. DIGITAL LINE DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Shunts secondary of T1
R2	Cathode resistor for V1
T1	Input transformer which provides 600-ohm input impedance
T2	Output transformer which provides 16-ohm output impedance
V1	Dual triode connected in parallel as cathode follower

3.29 DIGIT PLANE DRIVERS, MODELS A AND C

3.29.1 Definition and Description

The digit plane drivers (DPD) are logic circuits which function as negative current pulse generators. Two models of the DPD are utilized in AN/FSQ-7 and -8 equipments. Model A is used in Central Computer memory 2; model C, in Central Computer memory 1. The logic block symbols for both models are shown in figure 3–71. These circuits differ somewhat in configuration and principles of operation. For this reason, each model is discussed separately below.

3.29.2 Principles of Operation, Model A

3.29.2.1 Basic Operation

A block diagram of the ADPD is shown in figure 3–72. The input stage of the DPD consists of a d-c gate tube. The input from the inhibit selection gate has standard levels of −30 and +10V. When the DPD is not to be selected, this input is at the −30V level. When the DPD is to generate an inhibit pulse on its associated memory plane, the input is at the +10V level. The inhibit selection gate is approximately 5.5 μsec wide. The other input to the d-c gate tube also has standard levels of −30 and +10V. When the DPD is used to generate a current pulse, the inhibit pulse is used to control the current pulse width. If the inhibit selection gate is at the lower level when the inhibit pulse is applied, no output is generated. However, if the inhibit selection gate is at the

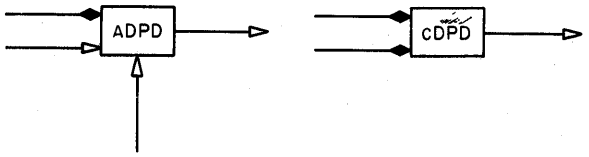


Figure 3–71. Digit Plane Driver, Models A and C, Logic Block Symbols

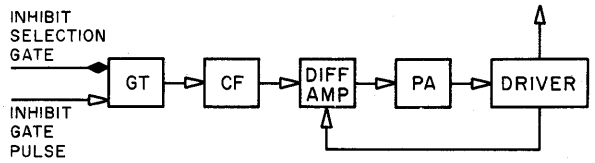


Figure 3–72. Digit Plane Driver, Model A, Block Diagram

upper level, application of the inhibit pulse to the d-c gate causes a negative pulse to be applied to the cathode follower. The output of the cathode follower is fed into the difference amplifier. Because of the feedback loop from the driver stage of the DPD, the output pulse of the difference amplifier is a negative signal. The negative signal is applied to the pulse amplifier which performs amplification, a shift in level, and inversion. The output of the pulse amplifier is applied to the driver stage and conditions it, causing a current pulse to be generated by this stage. The current pulse developed in the inhibit winding is a negative pulse of approximately 400 ma, controlled in duration and of approximately 2.5-μsec duration at the 10-percent point.

3.29.2.2 Detailed Operation

Figure 3–73, foldout, is the schematic diagram of the ADPD. Table 3–41 lists the associated detail parts and their functions. The circuit consists of a d-c gate tube (V1), a cathode follower (V2A), a difference amplifier (V2B and V3A), a pulse amplifier (V3B), and a driver tube (V4A and V4B connected in parallel).

The inhibit selection gate input line to V1 is normally at the −30V level. If the level on this line is at +10V when the inhibit pulse and the inhibit selection gate inputs are applied to the suppressor grid of V1, the tube conducts, thereby lowering its plate voltage from the normal +150V supply to a +60V level. The output of V1, which is coupled to the grid of cathode follower V2A, is a negative pulse of approximately 90V in amplitude, and, since the inhibit pulse is approximately 2.5 μsec in duration, the output of V1 is also of that duration.

In the quiescent state, the grid of V2A is held at approximately the +10V level by the action of resistor R4 and crystal diodes CR2 and CR3. When the output of V1 is coupled to the control grid of V2A, it causes this

tube to be cut off, and the voltage on the cathode starts to fall from +10V to −80V. It does not reach −80V, however, but is caught by the cathode of V2B. The cathodes of V2B and V3A are connected to the V2A cathode, and under steady-state conditions, all three cathodes are at the +10V level. When V2A conducts, the cathodes of V2B and V3A maintain these tubes at cutoff. When V2A is cut off, the current through the common cathode resistor utilized by these three tubes is transferred from V2A and is supplied by V3A. In supplying this current, the plate voltage of V3A starts to fall, and the negative signal thus generated is applied to the grid of V3B through a coupling capacitor.

Under steady-state conditions, V3B is conducting heavily, with the result that the plate is at a low level. Therefore, when the negative signal is transmitted from V3A to the grid of V3B, this tube is driven toward cutoff and the output pulse from its plate is coupled to the grids of V4A and V4B. These tubes are normally at cutoff with the cathode voltage being supplied by the −150V supply and the grids obtaining their voltage from the top point of a voltage divider connected between the grid circuit and −300V. When the positive signal is transferred from the plate of V3B to the control grids of V4A and V4B, crystal diode CR4 is cut off, representing a very high resistance path. As a result, the driving path of coupling capacitor C5 is through grid resistor R13. Because of the values of these two components, the time constant is very long compared to the pulse duration of the signal supplied by V3B. This signal causes the bias on the grids of V4A and V4B to decrease, resulting in a heavy conduction through the tubes, causing a nominal current pulse of approximately 400 ma to flow through a dropping resistor in the plate circuit, resulting in a 20V drop. This 20V drop represents itself as a negative signal to the grid of V3A. Thus, the negative signal generated by the plate of V3A which is transferred to the grid of V3B is limited, with the result that V3B will not cut off. Instead, a negative bias is applied to it and causes it to generate a positive signal which is transferred to the grids of V4A and V4B, resulting in a current pulse being generated in the inhibit winding. The amount of current flowing through the inhibit winding is a direct result of the steady-state voltage supplied to the grid of V3B. As this voltage is made more negative, a higher value of current flows through the inhibit winding; conversely, as this voltage is made more positive, the inhibit winding current is decreased.

TABLE 3–41. DIGIT PLANE DRIVER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Part of divider network between V1 grid and −150V supply (with CR1)
R3	V1 plate load resistor
R4	V2A grid-return resistor
R5	Common cathode resistor for V2A and V2B
R6, R7, R8	Form voltage divider in V2B grid circuit
R9	V3A plate load resistor
R10	V3B grid resistor
R11	V3B plate load resistor
R12	V4 plate load resistor
R13	Equalizing resistor
R14, R15	Voltage divider connected between −300 and −150V supplies
R16	Damping resistor
CR1	Part of divider network in V1 grid circuit (with R1 and R2)
CR2, CR3	Clamp V2A grid at +10V in quiescent state
CR4	Grid-clamping diode for V4A and V4B
C1	Coupling capacitor
C2	Shunting capacitor
C3	Shunting capacitor
C4	Coupling capacitor
C5	Coupling capacitor
C6	Bypass capacitor

3.29.3 Principles of Operation, Model C

Figure 3–74 is the schematic diagram of the cDPD. Table 3–42 lists the associated detail parts and their functions. The circuit consists of three stages: an input amplifier, a cathode follower, and a current driver.

When a DPD is not selected, the voltage at the cathode of diode CR1 is +10V. The +10V input is applied through R1 to the grid of V1. Grid current flow reduces the signal level at the grid to a potential slightly greater than 0V, resulting in a plate voltage of +70V. The grids of V2 are clamped at −215V from the action of voltage divider R7 and R8. Approximately the same potential appears at the cathodes of V2 and, by virtue of a common condition, at the grids of V3. The cath-

odes of V3 are returned to —150V, resulting in a —65V bias existing at the V3 grid. This bias prevents the tube from conducting.

When the input level shifts to —30V, the level at the grid of V1A drops from a slightly positive value to a steady value of approximately —3V. An initial negative spike occurs but recedes rapidly when the rising output voltage pulse is fed back to the input. The —3V input to the grid of V1 causes the plate voltage to rise from +70V to +140V. The net change of 70V is coupled through C1 to cathode follower V2, raising the potential at the grids from —215 to —145V. A similar rise at the cathode of V2 is applied to the grids of V3, thereby changing the net bias on V3 from —65V to approximately +4V, causing it to conduct. The cathode current for a —30V level input signal is approximately 460 ma of which approximately 440 ma is delivered to the inhibit region winding connected in the plate circuit. The remaining 20 ma constitutes grid current.

3.30 DIODE-CAPACITOR GATES, MODELS A AND B

3.30.1 Definition and Description

A diode-capacitor gate (DCG) is a logic circuit which passes a signal when conditioned by a level. The logic block symbols for the two DCG's utilized in the AN/FSQ-7 and -8 equipments are shown in figure 3–75. The differences between the models are accounted for by

TABLE 3–42. DIGIT PLANE DRIVER, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	V1 grid resistor
R2	Part of input AND circuit (with CR1)
R3	Current-limiting resistor
R4	V1 plate load resistor
R5, R6	Equalizing resistors
R7, R8	Voltage divider
R9	V2 cathode resistor
R10, R11	V2 plate resistors
R12, R13	V3 cathode resistor network (with R14)
R14	Gain control and part of V3 cathode resistor network
CR1	Part of input AND circuit (with R2)
CR2-CR5	Clamping diodes
C1	Speed-up capacitor
C2	Coupling capacitor
C3	Bypass capacitor
C4	Feedback capacitor

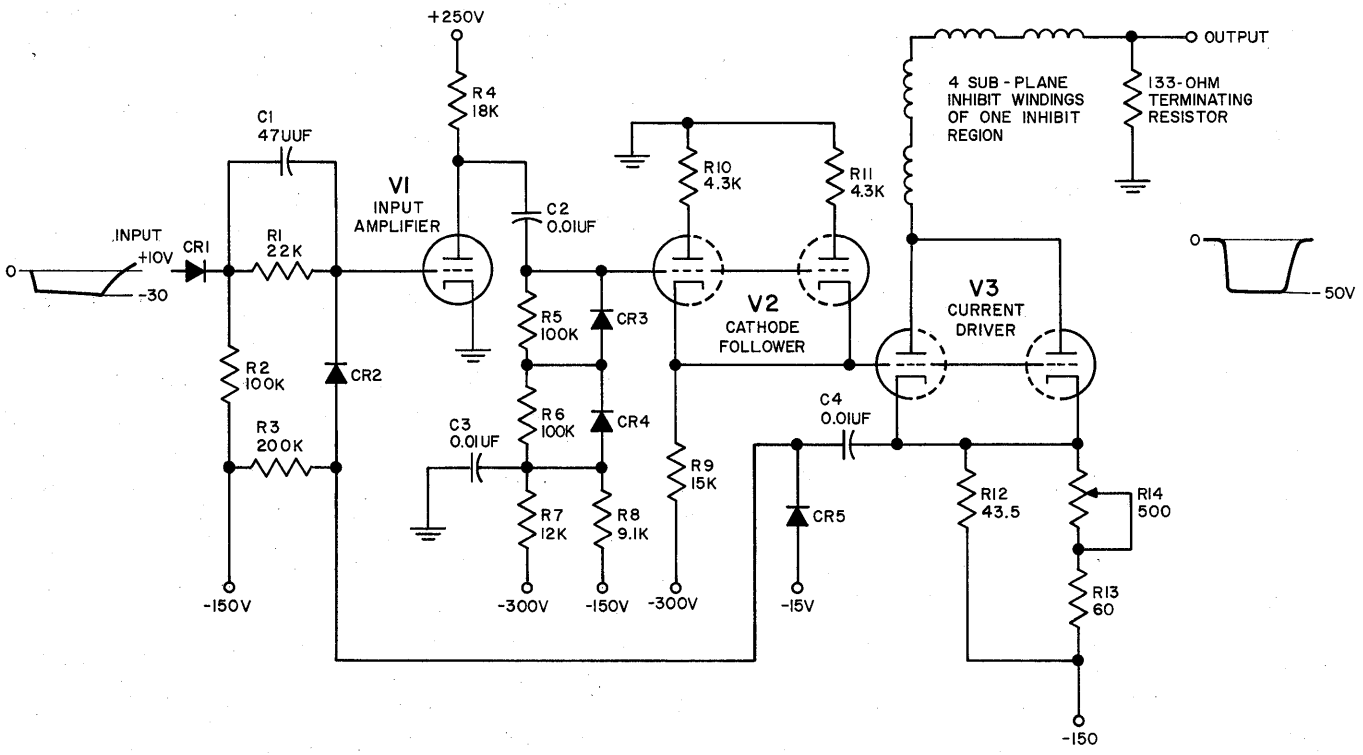


Figure 3–74. Digit Plane Driver, Model C, Schematic Diagram

the changes in detail components in the circuits and by the different type of signals received and transmitted by each model.

3.30.2 Principles of Operation

Figure 3–76 contains the schematic diagrams of the two models of the DCG. Table 3–43 lists the associated detail parts and their functions.

First consider the model ADCG (fig. 3–76,A). The circuit consists of a diode, a choke, a capacitor, and a resistor. The PULSE IN terminal is returned, in the feeding circuit, to –30V. With DC IN at +10V, the anode of diode CR1 is biased 40V negative with respect to the cathode. A standard pulse (40V maximum) cannot pass through CR1. With DC IN at –30V, the anode and cathode of CR1 are at the same potential. A standard pulse applied to PULSE IN develops a 40V pulse across L1 and R1 and is coupled to PULSE OUT by C1.

Now consider the model BDCG (fig. 3–76,B). This circuit consists of a diode, a capacitor, a voltage divider, and a BIT SELECTION switch. A 1 pulse (approximately +30V) is applied to the anode of CR1 through PULSE IN. The voltage divider biases CR1, the bias potential depending on the position of S1 in the DC IN. When S1 is in the OFF position, +90V is applied across the voltage divider and a resulting +76V is applied to the cathode of CR1. The +30V 1 pulse on the anode of CR1 makes the anode negative with respect to the cathode, and as a result, this pulse is prevented from passing through. When S1 is in the ON position, a +10V potential is applied across the voltage divider, resulting in a bias of +8.5V on the cathode of CR1. The +30V 1 pulse on the anode is now sufficient to overcome this bias and, as a result, is coupled to PULSE OUT by capacitor C1.

3.31 DISTRIBUTION POWER AMPLIFIER

3.31.1 Definition and Description

The distribution power amplifier (DPA) is a non-logic direct-coupled, voltage-controlled, negative feedback circuit which performs a buffering function. The logic block symbol for the DPA is shown in figure 3–77.

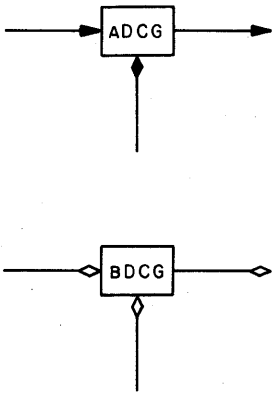


Figure 3–75. Diode Capacitor Gate, Models A and B, Logic Block Symbols

TABLE 3–43. DIODE-CAPACITOR GATE, MODELS A AND B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	USED ON MODEL	FUNCTION
C1	Both	Coupling capacitor
CR1	Both	Gating diode
R1	A	Load resistor
R2,R3	B	Voltage divider
Rx	A	D-C return of feeding circuit
S1	B	Bit selection switch

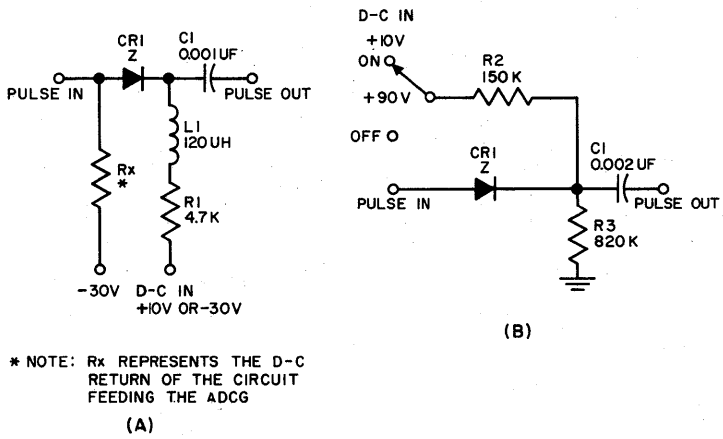


Figure 3–76. Diode Capacitor Gates, Models A and B, Schematic Diagrams

3.31.2 Principles of Operation

Figure 3—78 is the schematic diagram of the DPA. Table 3—44 lists the associated detail parts and their functions. The input signal is applied to a voltage divider network connected between the regulated +150V and regulated —150V supplies. The grid voltage for V1A which is set by potentiometer R6 determines the operating point of the differential tube whose common cathode connection is returned to —250V through cathode resistor R9. The grid of V1B is connected to potentiometer R18 which is part of an output load network to ground. In this manner, a fraction of the output voltage on the grid of V1B is compared with a portion of the input voltage on the grid of V1A. The difference voltage between the two grids is amplified in the plate circuit and directly coupled to the grid of V2B. Since

TABLE 3—44. DISTRIBUTION POWER AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1-R7	Form voltage divider network between regulated power supplies
R8	V1A plate load resistor
R9	Common cathode resistor for V1A, V1B
R10, R11	Voltage divider network between +150V and ground
R12	Forms part of network which stabilizes VR tubes from transients (with C2, C3, C4)
R13-R15	Part of V2B cathode parallel network (with VR3)
R16	V3 plate load resistor
R17	Part of high-frequency bypass network (with C6)
R18, R19	Output load network
R20	V5 cathode resistor
C1	Bypass capacitor
C2, C3, C4	Parallel capacitor bank which stabilizes VR tubes from transients
C5	Coupling capacitor
C6	Part of high-frequency bypass network (with R17)
C7	Compensating capacitor

Figure 3—77. Distribution Power Amplifier, Logic Block Symbol

the two cathodes are tied together and returned to a —250V supply, conduction takes place in both sections of the differential amplifier. The plate of V1A is returned to the +150V supply through plate load resistor R8. To increase the stability of this stage, the plate voltage of V1B is supplied by a series-current tube which acts as a variable resistance to compensate for variations within V1B. The plate of V2A is connected directly to the +250V supply, and the grid bias is established by a voltage divider network between +150V and ground. The cathode of V2A is tied to the plate of V1B.

The amplified difference voltage now on the grid of cathode follower V2B is taken from a paralleled network in the cathode of this tube and is coupled directly to the grid of V3. The cathode voltage of V2 is maintained positive by the action of VR3 in series with VR1, VR2, and current-limiting resistor R14. V2 functions as a matching circuit to establish the correct plate-to-grid relationship of the differential amplifier and the high-gain pentode amplifier.

The signal appearing on the grid of tube V3 is amplified and directly coupled from the plate to the grid of V4. With the cathode and suppressor grid connected together and tied to —150V, pentode V3 operates at a negative level to enable its plate voltage to be used as bias for output driver tube V4. Current flow through plate load resistor R16 of tube V3 reduces plate voltage sufficiently to serve as grid voltage for V4 which is now more negative than its cathode. Capacitor C6 and resistor R17, connected from the grid input to ground, serve as a high-frequency bypass. Slow variations are unaffected by the capacitor; frequencies high enough to pass through the capacitor will be dampened by resistor R17 and bypassed to ground.

Output driver tube V4 is connected as a cathode follower. The cathode output load consists of potentiometer R18 and resistor R19 to ground. Series-current tube V5 has its plate connected to the cathode of V4 and its cathode connected to the —300V supply through resistor R20. The current tube acts as a variable resistance, compensating for load variations within V4, and helps to maintain a zero reference level at the output. The operating point of V4 is set by potentiometer R18 (zero adjust) to a level where the plate current of V4 is equal to the current supplied by V5. As a result, no current will flow through load resistors R18 and R19, since all the current required by tube V4 is supplied by tube V5.

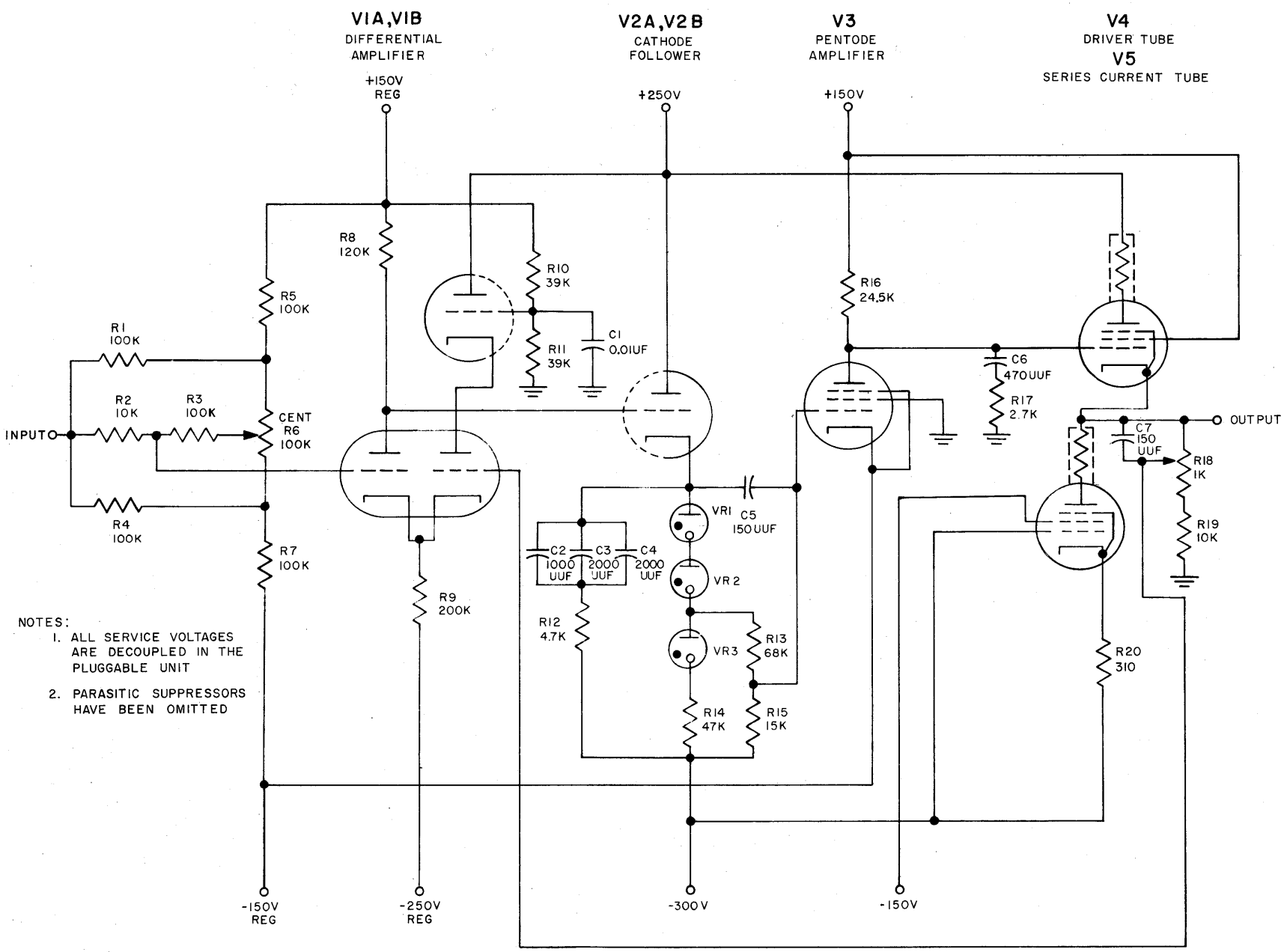


Figure 3–78. Distribution Power Amplifier, Schematic Diagram

When tube V4 receives a positive input signal, the additional tube current flows from ground through the load (R18 and R19), producing a positive voltage output. When V4 receives a negative signal, part of the current supplied by V5 then flows from the load to ground, producing a negative voltage output. The DPA is required to produce an output which is proportional to, and of the same polarity as, the input which can swing from any value between + or −26V.

3.32 DRUM FIELD DRIVER

3.32.1 Definition and Description

The DFD is a nonlogic circuit which amplifies the driving power of standard levels. Figure 3–79 shows the logic block symbol for the DFD. In Drum System logic, the DFD is part of the drum field selection circuits. Each DFD is connected to a drum field consisting of 33 drum heads (read-write) in parallel. When a drum field is selected, a +10V standard level is applied to the associated DFD. When a drum field is not selected, a −30V standard level is applied to the associated DFD. The DFD amplifies these levels. One DFD produces an upper level to permit drum heads in the selected field to conduct during a reading or writing operation. All other DFD's produce a lower level which cuts off or isolates the drum heads of the not-selected drum fields.

3.32.2 Principles of Operation

Figure 3–80 is the schematic diagram for the DFD. Table 3–45 lists the associated detail parts and their

Figure 3–79. Drum Field Driver, Logic Block Symbol

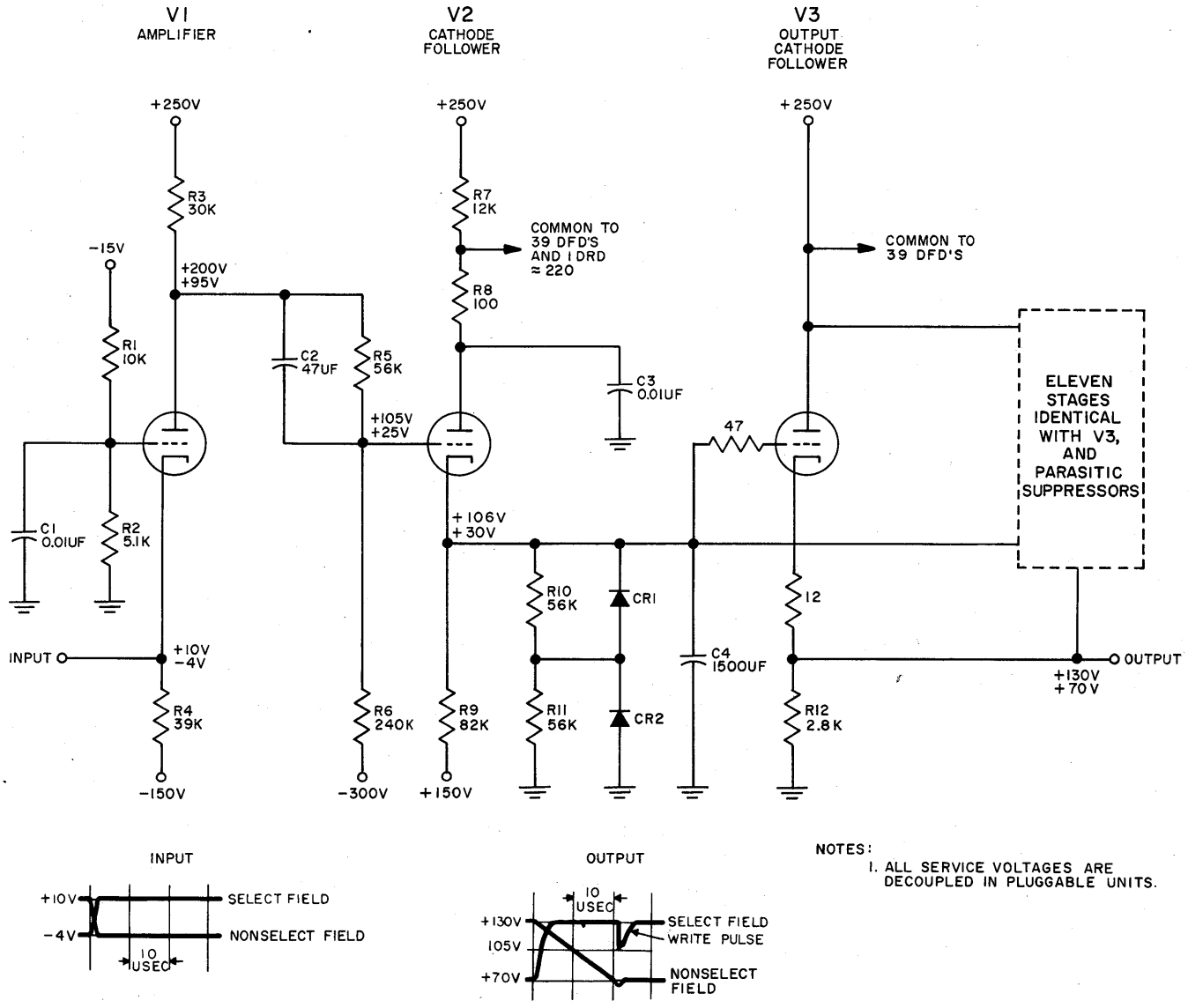


Figure 3–80. Drum Field Driver, Schematic Diagram

functions. The DFD consists of three stages. Input stage V1 is an amplifier of the grounded grid type. The intermediate stage, V2, is a cathode follower which isolates the input stage from the output stage. The output stage, V3, consists of 12 tubes connected in parallel as a cathode follower. This output stage provides sufficient current to enable 33 drum writers to perform their functions in the selected field.

The input level to the cathode of V1 is always either +10V or −4V. The grid is maintained at −5V by voltage divider R1 and R2. With +10V at the cathode, amplifier V1 is biased beyond cutoff and does not conduct. Current through voltage divider R5, R8, and R9 sets V1 plate voltage at +300V and V2 grid voltage at +105V. The cathode of V2 rises to +106V. This voltage is applied to the 12 grids of the output stage and the output voltage rises to +130V.

With −4V at the cathode of V1, the plate voltage falls to 100V. Current through V1 and R8 and R9 combines in R5 to produce the fall. The current through voltage divider R8 and R9 sets grid voltage at 25V. The cathode of V2 settles at 30V and the cathode of V3 follows to 70V. Forty volts bias on the 12 output stages is sufficient to cause each tube to contribute its share of the total current (25 ma) required.

TABLE 3–45. DRUM FIELD DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Bypass capacitor
C2	Compensating capacitor
C3	Decoupling network with R8
C4	Shaping network (with R9, R10, and R11)
CR1, CR2	Clamping diodes
R1, R2	Grid bias voltage divider
R3	V1 plate load resistor
R4	Cathode input load resistor
R5, R6	Direct-coupling voltage divider
R7	V2 plate dropping resistor
R8	Decoupling network with C3
R9	Cathode load resistor
R10, R11	Equalizing resistors for diodes CR1 and CR2
R12	Cathode load resistor

The rapid transitions of the input voltage from one level to another necessitate the use of components to preserve the fast rise time and slow down the fall time. The shift from 100 to 200V at the plate of V1 is applied to the grid of V2 with slight loss in rise time because of compensating capacitor C5. The input capacitance of V2 and C5 forms an a-c voltage divider for the high-frequency components of the input level shift and prevents excessive rounding off of the voltage rise.

On the other hand, capacitor C9 causes the fall of V2 from 106 to 30V to be applied to the grids of the output stages as a gradual change of 20-μsec duration. As a result, the output of the DRD falls linearly from 130 to 70V.

3.33 DRUM READ AMPLIFIER

3.33.1 Definition and Description

The drum read amplifier (DRA) produces a positive signal level shift which is of 2-usec duration and is centered on the negative-going crossover point of the input signal. The logic block symbol for the DRA is shown in figure 3–81. In Drum System logic, the DRA produces a level shift which is applied to a gate tube to pass a standard pulse each time a 1 bit is read by a read head. The logic block symbol shows three inputs. Two are the balanced output of a connection drum read head. The third is either a ground or one of two voltage levels and is dependent upon the specified application of the DRA.

3.33.2 Principles of Operation

The DRA is a 5-stage circuit which amplifies and shapes a sinusoidal input into an appropriate gating signal. Figure 3–82 is the schematic diagram for the DRA. Table 3–46 lists the associated detail parts and their functions. The input signal may be one of three types. See figure 3–83. Waveforms 1A, B, and C represent the signal developed by a drum read head when a series of 1 bits, a series of 0 bits, and an alternating series of 1 and 0 bits, respectively, are stored on a drum surface. Waveforms 1A and 1B have a frequency of 100,000 cps. Waveform 1C is composed of two sine waves: a fundamental with a frequency of 50,000 cps and a third harmonic with a frequency of 150,000 cps. All DRA circuit components have been selected to pass these frequencies without distortion and with a minimum difference in phase shift.

The input circuit to the DRA is a transformer with a center-tapped primary. The center tap is returned to +150, +100, or ground (fig. 3–82). When employed with the drum read-write heads, the primary winding of T1 is part of the circuit between the DFD and the DRD, as shown in figure 3–84,A. During a writing operation, the drum head is used for writing purposes and the DRA is isolated from the read-write head by the

diode switches which are biased beyond cutoff by the +150V applied to the center tap of T1. During a reading operation, the DRD level becomes +100V, making the diodes conductive. When used with the read head, the center tap of T1 is returned to ground (fig. 3–84,B). In either instance, current induced in the read head flows in the primary winding and induces a voltage in the secondary five times greater than that across the primary winding. Signal voltages applied to the grid of V1 vary between 250 mv and 1.5V peak to peak.

With no signal applied to V1, the grid is at ground, the cathode is at 1.5V, and the plate is at 140V. Bypass capacitor C1 in conjunction with R4 forms a cathode bias network which maintains the cathode at 1.5V. Resistor R2 is a grid-limiting resistor which prevents the grid from becoming positive with respect to the cathode in the presence of positive-going transient voltages. Stage

Figure 3–81. Drum Read Amplifier, Logic Block Symbol

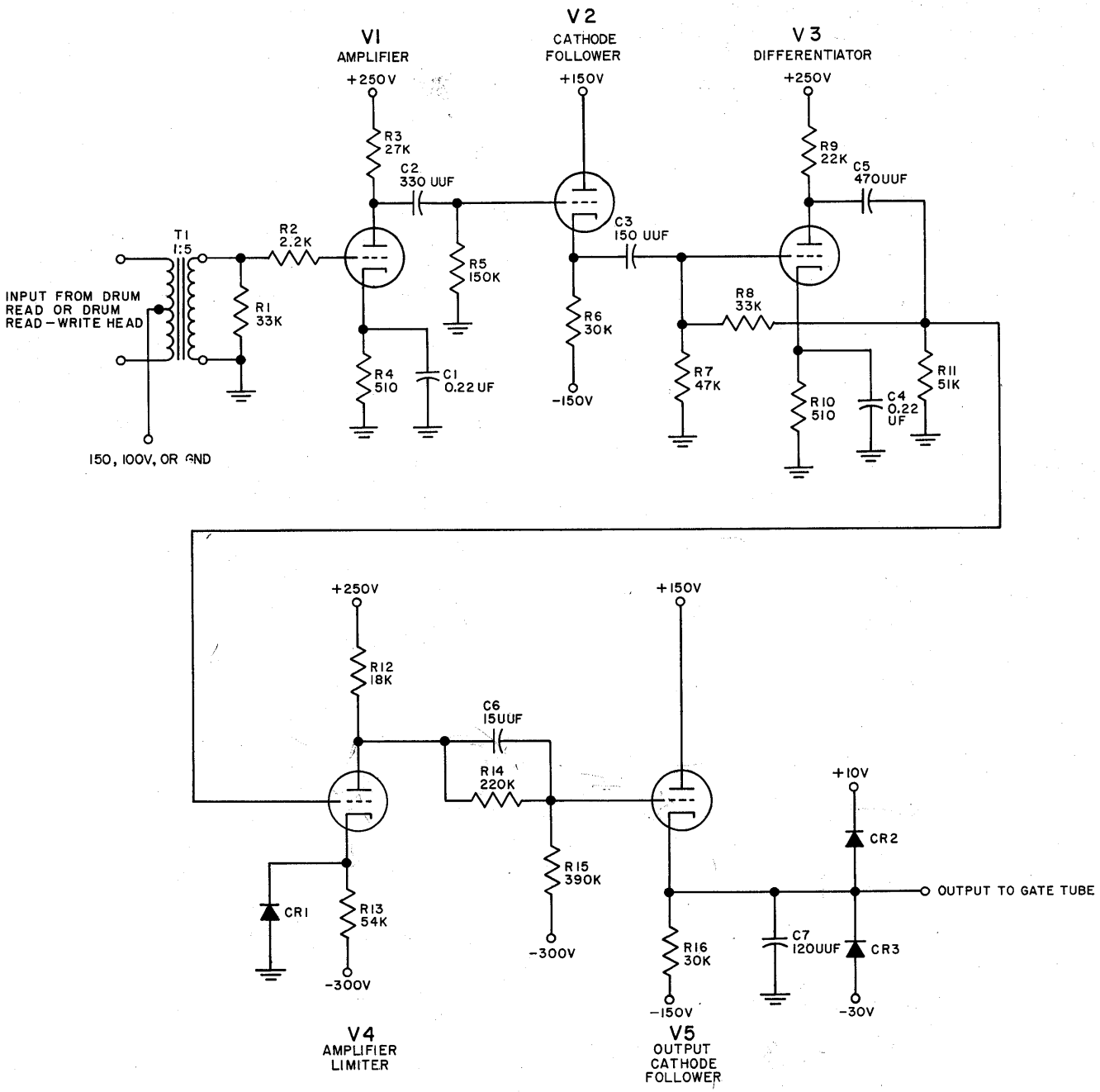


Figure 3–82. Drum Read Amplifier, Schematic Diagram

TABLE 3–46. DRUM READ AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1	Bypass capacitor	R5	V2 grid return
C2, C3	Coupling capacitor	R6	V2 cathode resistor
C4	Bypass capacitor	R7	V3 grid return
C5	Coupling capacitor and part of feedback network (with R8)	R8	Part of feedback network (C5)
		R9	V3 plate load resistor
C6	Compensating capacitor	R10	V3 cathode resistor
C7	Smoothing capacitor	R11	V4 grid return
CR1-CR3	Clamping diodes	R12	V4 plate load
R1	Transformer load resistor	R13	V4 cathode resistor
R2	V1 grid limiting resistor	R14, R15	Voltage divider forming direct-coupling network
R3	V1 plate load resistor		
R4	V1 cathode resistor	R16	V5 cathode resistor

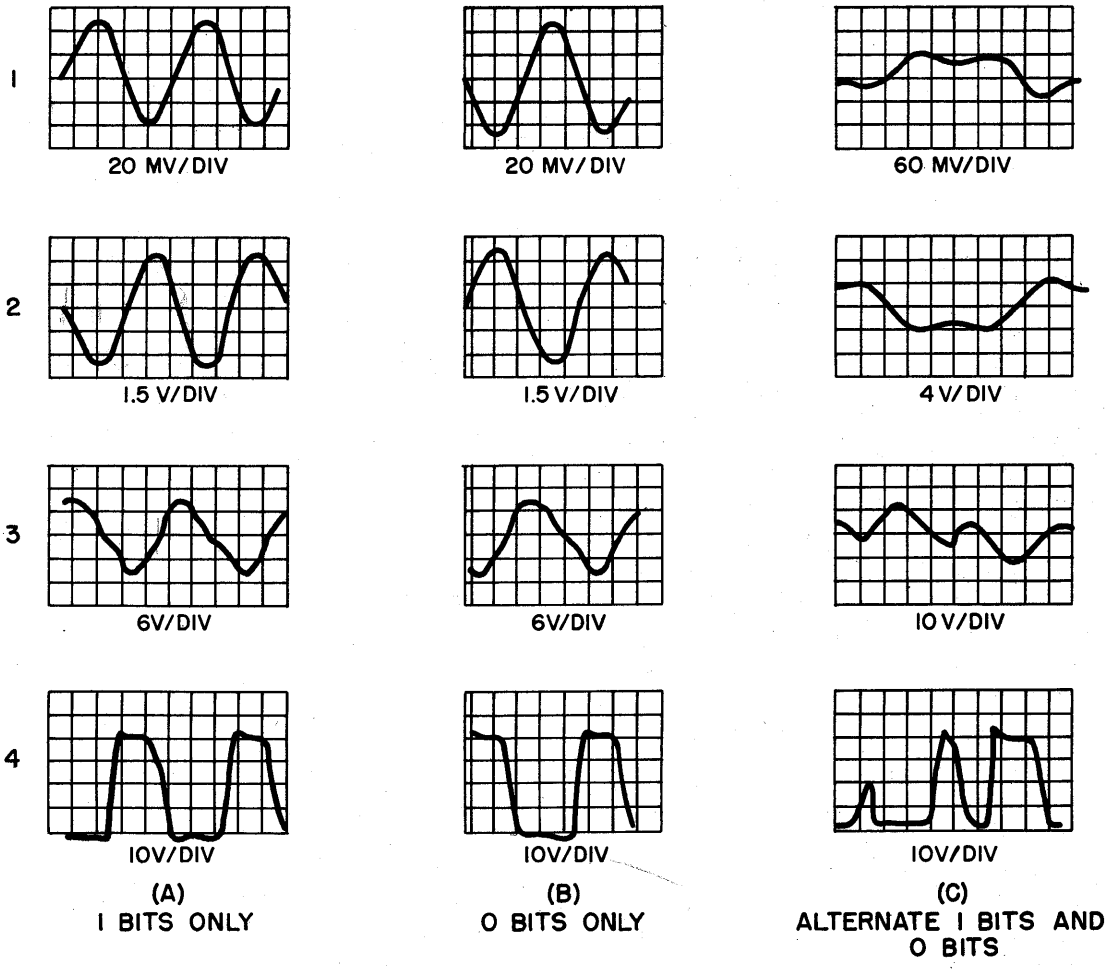


Figure 3–83. Waveforms for Drum Read Amplifier

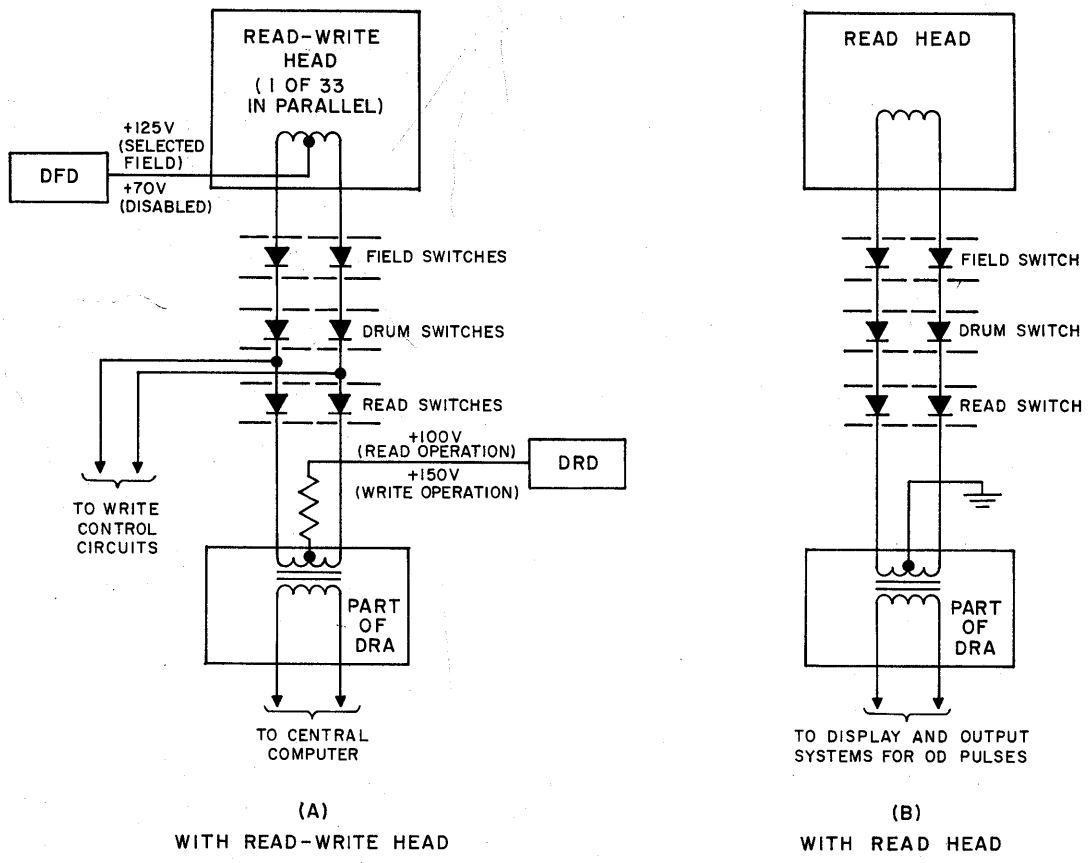
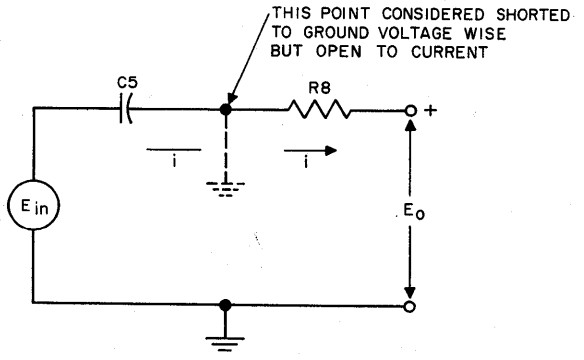


Figure 3—84. Drum Read Amplifier Applications

V1 amplifies input voltage by 20 times, producing an output of 5 to 30V peak to peak. Cathode follower V2, which acts as a buffer between the input stage, V1, and the differentiator, V3, applies the inverted signal (fig. 3—83, waveform 2) to the grid of V3.

The differentiator, V3, may be represented by the equivalent circuit shown in figure 3—85. The feedback to the input through C5 and R8 has the effect of producing 0V or a vertical ground at the grid. This ground applies to voltage only. The current flows past this point through R8 and the output load. With the grid at ground, the input voltage appears across C5 and a current leading this voltage by 90 degrees is generated. This leading current, in turn, produces a voltage across resistor R8 which leads the input voltage by 90 degrees.

Tube V4 amplifies and inverts the negative half cycles of V3 output voltage. Positive half cycles are limited by cathode follower action. The positive rise at the input equals 9V (fig. 3—83, waveform 3). The cathode follows this rise. The current through R12 required to produce this rise causes a 3V fall to 110V at the plate. When the grid voltage becomes negative, diode CR1 clamps the cathode at ground. The negative-going grid voltage (—9V peak) drives the tube almost to cutoff and plate voltage rises to +205 ±5 V. Voltage divider R14 and R15 couples 0.36 of V4 plate voltage rise and fall to the grid of V5. Capacitor C6 compensates for the attenuation of high frequencies by the input capacitance of V5. Cathode follower V5 provides a low impedance source of gating voltage for a model A gate tube. The output is illustrated in figure 3—83, waveform 4.



$$i = \frac{E_{in}}{\frac{1}{jWC}} = jE_{in}WC = E_{in}WC \angle 90°$$

$$e_o = Ri = E_{in}WCR \angle 90°$$

Figure 3—85. Differentiator, Equivalent Circuit

3.34 DRUM READ DRIVER

3.34.1 Definition and Description

The drum read driver (DRD) inverts the polarity and amplifies the driving power of standard voltage levels. Figure 3–86 is the logic block symbol for the DRD. In Drum System logic, the DRD applies two voltage levels, one at a time, to the inputs of three drum read amplifiers. One level (upper) inhibits the amplification of the drum head output; the other level (lower) permits the amplification of this output.

3.34.2 Principles of Operation

3.34.2.1 Basic Operation

Figure 3–87 is the block diagram of the DRD. The circuit consists of an inverter, isolating cathode follower, and power cathode follower output stage. The input to the DRD is always a standard level. To inhibit reading operations, the DRD input voltage must be −30V. To permit reading operations, the DRD input voltage must be +10V.

The input voltage is inverted by V1 and appears inverted at the output of the DRD. Thus, −30V at the input causes the output to rise to +150V, the upper output level. With the input at +10V, the output falls to +100V. The fall to +100V from +150V is slowed down to approximately 30 μsec to minimize the formation of transients which would block drum read amplifiers.

3.34.2.2 Detailed Operation

Figure 3–88 is the schematic for the DRD. Table 3–47 lists the associated detail parts and their functions. When the input voltage to V1 shifts from +10V to −30V, tube V1 is cut off because the cathode is at ground potential. The resultant plate voltage rise to +150V is direct-coupled to the grid of cathode follower V2. The cathode of V2 follows the grid rise to +150V and applies it to the six grids of the power cathode follower output stage. The output voltage rises to +150V. The rounded edge in the rise output voltage from +100V to +150V is due to the time required to charge capacitor C1 through the plate resistance of V2. In the applications of the DRD, resistor R3 is one of many resistors in the V2 return path to +25V. Thirty-nine drum field drivers, in parallel, are connected to the tube side of R3. Each of the DFD's, in turn, is returned to 250V through a 12K resistor. Therefore, the effective resistance in the return path to +250V is 12000/40 = 300 ohms. For this reason, resistor R3 has little effect on the charging time of C1 when compared with the effect of V2 plate resistance which is 25 times larger.

When the input voltage to V1 shifts from −30V to +10V, tube V1 conducts heavily. Grid current through R1 limits grid rise to between ground and +1V. V1 plate voltage falls to +83V. This fall in voltage is applied directly to the grid of V2, causing a decrease in current through V2. The resultant fall to +85V in cathode voltage is coupled directly to the six grids in parallel of the output stage. Each tube is a power triode capable of providing on the order of 55 ma with 20V negative bias. The output of V3 falls to +100V. The cathode, however, is at +105V due to parasitic suppressor R12 providing a net grid voltage of −20V.

Figure 3–86. Drum Read Driver, Logic Block Symbol

3.35 DRUM WRITERS, MODELS A AND B

3.35.1 Definition and Description

The drum writer (DW) produces a 2-μsec current pulse of predetermined direction as a function of three input voltages. Two of the voltages operate as a pair (standard level outputs of a flip-flop) and condition one

TABLE 3–47. DRUM READ DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Compensating capacitor
R1	V1 grid-limiting resistor
R2	V1 plate load resistor
R3	V2 plate-dropping resistor
R4	V2 cathode resistor
R5	V3 bias-developing resistor and parasitic suppressor
R6	Output developing resistor

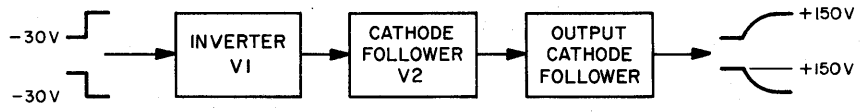


Figure 3–87. Drum Read Driver, Block Diagram

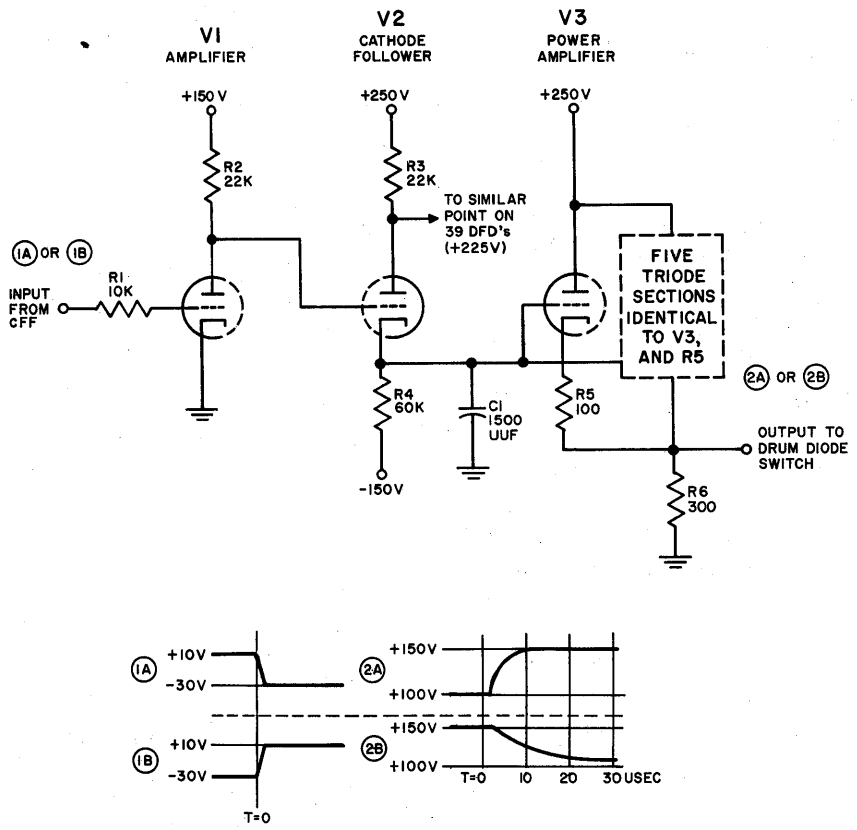


Figure 3–88. Drum Read Driver, Schematic Diagram

of two magnetizing current sources. The third input voltage determines the width or duration of the current pulse. Figure 3–89 is the logic block symbol for the DW.

In Drum System logic, the DW effects the transfer of a 1 or 0 bit from the write register to a drum by supplying the required magnetizing current to a drum write head. Two models of the DW are employed in the Drum System. Model A drives its associated drum head through a diode drum switch. Model B drives its associated drum head directly.

3.35.2 Principles of Operation

3.35.2.1 Basic Operation

Figure 3–90 is a block diagram of a DW. The input to the DW, applied at input amplifier stage V1A and V1B, are 1- or 0-state d-c levels from the output of an associated flip-flop in the write register. If the write register flip-flop is set, a positive voltage appears at the input to the V1B stage and a negative voltage appears at the input of the V1A stage. If the write register flip-flop is cleared, the positive voltage appears at the input to the V1A stage and the negative voltage appears at the input to the V1B stage. The input amplifier stage receiving the positive input conducts, and the other input amplifier is cut off. The nonconducting input amplifier stage conditions the associated output amplifier stage (tube V2A or V2B). A positive level shift from the drum write driver causes conduction in the conditioned output amplifier stage and through the write head coil connected to the drum writer. The direction of current flow is determined by the output amplifier stage that conducts. If stage V2A conducts, the direction of current flow through the coil produces a flux polarity that represents binary 1. If stage V2B conducts, the direction of current flow through the coil produces a flux polarity that represents binary 0.

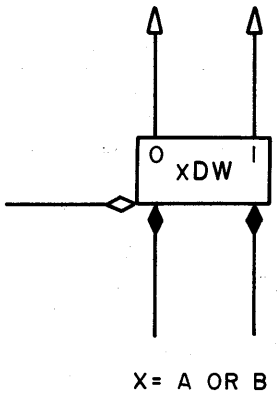


Figure 3–89. Drum Writer, Logic Block Symbol

3.35.2.2 Detailed Operation

Figure 3–91 is the schematic diagram for the ADW and BDW. Table 3–48 lists the associated detail parts and their functions. The inputs to V1A and V1B will always be +10V and −30V or −30V and +10V, respectively. Assume that the register feeding the ADW is set. Then the input terminal to V1B is at +10V and the input terminal to V1A is at −30V. Voltage dividers fix applied grid voltage levels at −150V for V1B and −170V for V1A. The common cathode connection of V1 will rise to the higher of these applied voltages; i.e., −150V. Thus, V1B conducts and V1A is cut off. The current through V1B drops plate voltage to −46V. This voltage is applied directly to the grid of V2B. The common cathode of V2 is connected to ground; therefore, V2B is cut off. The cathodes of diodes CR1 and CR2 are connected to the cathode circuit of a drum write driver (DWD). This cathode circuit consists of either a 470-ohm resistor to −150V in the ADWD or a 1,200-ohm resistor to −150V in the BDWD. The combination of 33 DW's in parallel connected in series with

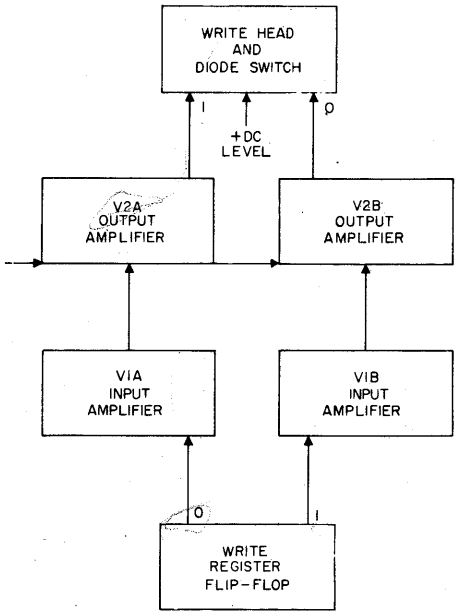


Figure 3–90. Drum Writer, Block Diagram

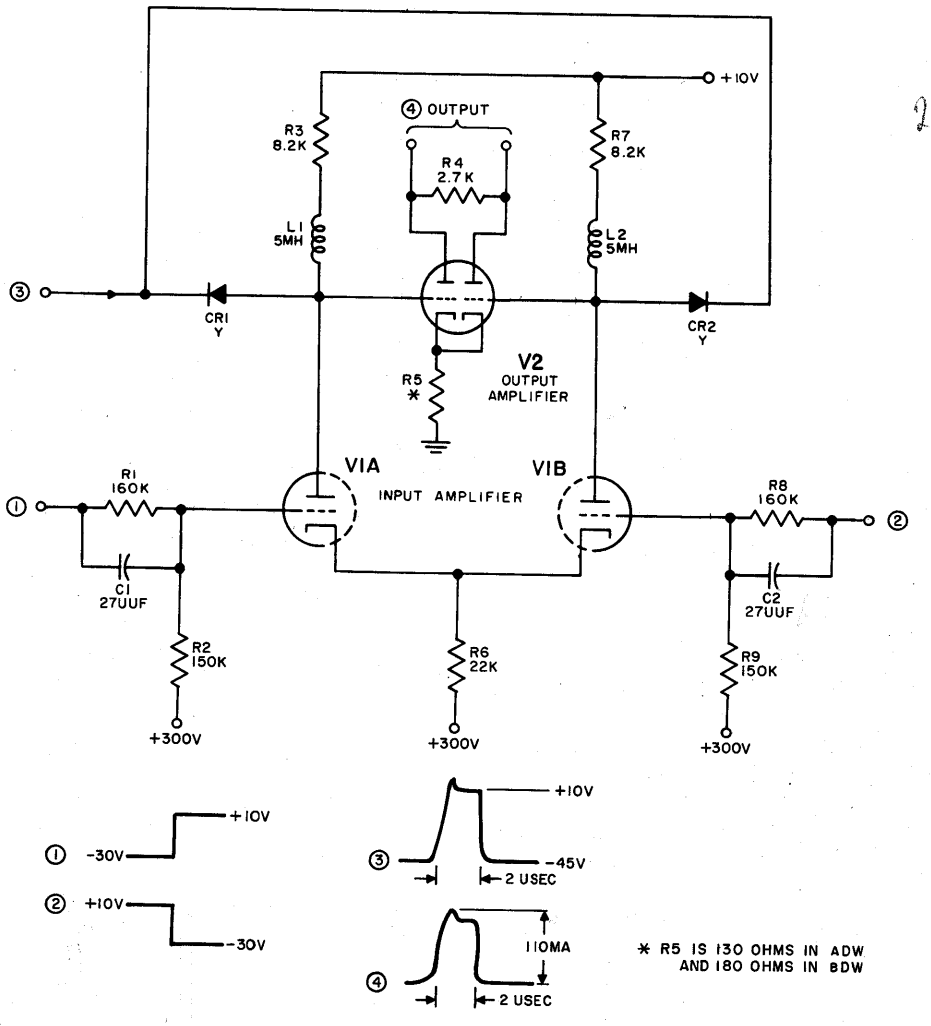


Figure 3–91. Drum Writer, Models A and B, Schematic Diagram

a 470-ohm resistor between +10V and —150V forms a voltage divider which fixes the plate voltage of V1A and the grid voltage of V2A at —45V. Thus, although V1B is conducting and V1A is not, both plates are at —45V.

A positive pulse from the DWD is applied simultaneously to the cathodes of CR1 and CR2. Since V2B is conducting, current through the tube maintains the anode of CR2 at —45V and the positive rise at the cathode of CR2 is isolated from the plate of V2B by the back resistance of the diode. However, V2A is not conducting. The voltage at the plate is a function of the current through R3, L1, CR1, and the cathode resistance of the DWD. Therefore, as the voltage at the cathode of CR1 starts to rise, current through R3, L1, and CR1 is reduced, and the voltage at the anode of CR1 and the grid of V2A rises. The voltage at the grid of V2A closely follows the input voltage pulse from the DWD, producing the current pulse shown in figure 3—91 in triode section V2A. This current passes through one-half of a center-tapped winding in a write head. The other half of the center-tapped winding is connected to the plate of V2B. The center tap is connected to a d-c voltage source. Since the winding is continuous, electron flow from each end to the center tap produces opposing magnetic fields.

TABLE 3—48. DRUM WRITERS, MODELS A AND B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1, C2	Speedup capacitors
CR1, CR2	Input isolating diodes
L1, L2	Peaking coils
R1, R2	Voltage divider
R3	V1A plate load resistor
R4	Damping resistor for drum writer head
R5	V2 cathode resistor
R6	V1 cathode resistor
R7	V1B plate load resistor
R8, R9	Voltage divider

For this reason, the drum writer will supply a 1- or 0-bit magnetizing current when V2A or V2B, respectively, is made conductive.

When the register is cleared, the applied voltages to V1A and V1B and the previously described actions of circuit pairs in the DW are interchanged. Thus, with V1B conductive, V2A will conduct when a pulse from a DWD is applied to the DW. With V1A conductive, V2B will conduct when a pulse from a DWD is applied to the DW. A 1 bit is magnetically stored on the drum when V2A conducts. A 0 bit is magnetically stored on the drum when V2B conducts.

3.36 DRUM WRITE DRIVERS, MODELS A AND B

3.36.1 Definition and Description

The drum writer driver (DWD) is a nonlogic circuit which inverts and amplifies the power of a voltage shift to the negative standard level of approximately 2-μsec duration. There are two models of the DWD. Model A with the greater power amplification can drive 33 DW's (par. 3.35). Model B is capable of driving 12 DW's.

In Drum System logic, the DWD inverts and power-amplifies a d-c command signal and applies it to DW's which thereupon generate write pulses for their associated drum heads. Figure 3—92 is the logic block symbol for the DWD.

3.36.2 Principles of Operation, Model A

3.36.2.1 Basic Operation

Figure 3—93 is the block diagram of the ADWD. The circuit consists of an amplifier input stage, clamping network, and cathode follower output stage. The clamping network prevents the amplifier output from exceeding +10V or —105V. The shift to the negative standard level at the input amplifier is amplified and inverted. The clamping network fixes the peak value of voltage rise at +10V. The cathode follower will produce this voltage at its output. Because of its connection

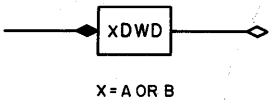


Figure 3—92. Drum Write Driver, Models A and B, Logic Block Symbol

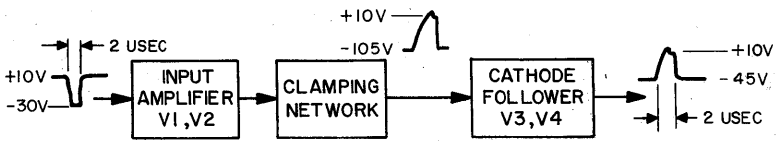


Figure 3—93. Drum Write Driver, Model A, Block Diagram

to DW's, the output voltage will rise from a quiescent value of —45V instead of —105V.

3.36.2.2 Detailed Operation

The schematic diagram for both models of the DWD is shown in figure 3–94. Table 3–49 lists the associated detail parts and their functions. The input signal, as shown, is a level shift from +10V to —30V for 1.7 or 1.8 μsec. Thus, with no signal input, the grids of V1 and V2 are at +10V. With the cathodes returned to —150V, V1 and V2 conduct and cathodes rise to +10V. The plates are at approximately 90V. The grids of V3 and V4 are at —105V as follows. The junction of resistors R8 and R9 is, by voltage divider action, at —105V. The junction of R5 and R6 is returned to —300V through R10. As a result, diodes CR4 and CR5 are positively biased and conduct, shorting resistors R6 and R7 and placing the junction of R6 and R5 or the grids of V3 and V4 at —105V. The cathodes of V3 and V4 are at —45V because of the voltage divider action of the DW plate circuits (not shown) in series with R11 between +10V and —150V. Thus, with —105V at the grids and —45V at the cathode, V3 and V4 are cut off when there is no signal.

The signal, a negative shift to—30V, is applied to the grids of amplifiers V1 and V2 through isolating network C1 and R1. Cathode voltage follows this fall to ground level. Below ground potential, CR1 conducts and clamps the cathode at ground level. The fall to —30V at the grid cuts the amplifier stage off and the plate voltage rises toward +250V. Peaking coil L1 ensures that the fall time of the input wave will appear in the rise time of the output wave. The junction of R5

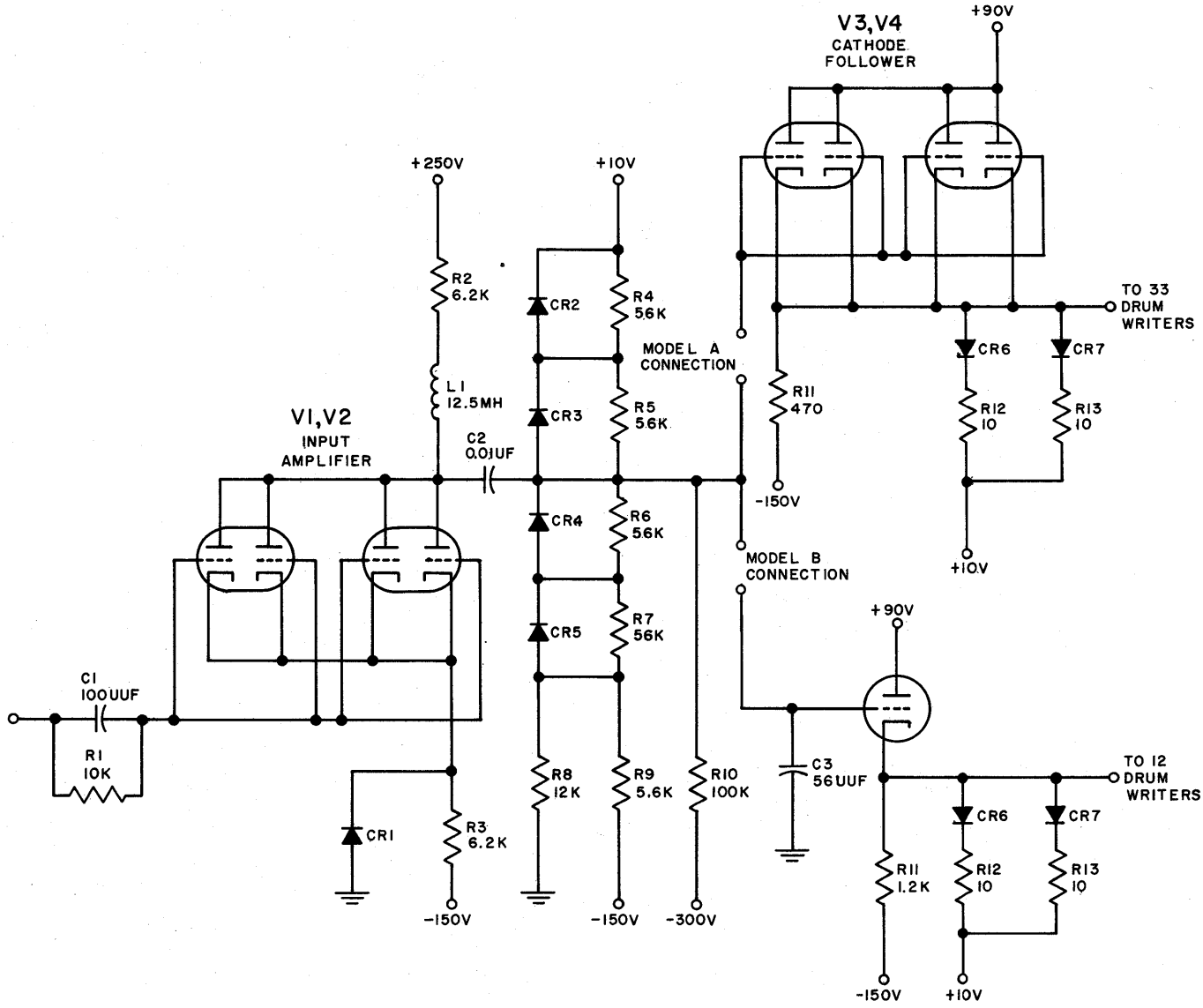


Figure 3–94. Drum Write Drivers, Models A and B Schematic Diagrams

and R6 will follow this rise in amplifier plate voltage because the charge across C2 cannot change instantaneously. When +10V is reached, diodes CR2 and CR4 conduct, maintaining the grids of V3 and V4 at +10V. The output voltage of V3 and V4 will rise with grid voltage from —45V when the grid voltage passes this level in its rise from —105V to +10V.

3.36.3 Principles of Operation, Model B

The operation of the BDWD is the same as that of the ADWD. Comparison of the output stages of each model reveals the following differences. The BDWD employs one triode section instead of four. The cathode load resistor of the BDWD is 12,000 ohms instead of 470 ohms. Only one triode section is employed in the BDWD because of the lighter load being driven. The cathode resistor is larger in order to establish a —45V output level during the no-signal period. It is recalled that the DW's, in series with the cathode load resistance of the DWD, form a voltage divider between +10V and —150V. Since the DW's are connected in parallel, the fewer the number of DW's the greater the equivalent resistance. Therefore, with 12 instead of 33 DW's, the equivalent resistance is approximately 33/12 times as great and the cathode load resistor must be approximately that many times larger than the cathode load resistor in the ADWD in order to have the same rate of voltage division.

3.37 FLUX AMPLIFIER

3.37.1 Definition and Description

The flux amplifier (FA) is a nonlogic circuit which is used to sense output signals, to discriminate between these signals as to amplitude, and to amplify them. The logic block symbol for the FA is shown in figure 3–95.

3.37.2 Principles of Operation

Figure 3–96 is the schematic diagram of the FA. Table 3–50 lists the associated detail parts and their functions. The circuit utilizes a twin-triode tube, one-half of which amplifies the approximately half-sine-wave output of a row of a ferrite core array; the other half drives the input winding of the associated core shift in the output shift registers.

The input signal is received from the sense winding of the associated row of ferrite cores. This negative pulse core output of approximately 0.35V is stepped up in transformer T1 to approximately 5.0V. A network, consisting of crystal diodes CR1 and CR2 with resistor R2, is used in the control grid circuit of the first stage to prevent unwanted triggering of the circuit by noise or other extraneous pulses. A gating voltage, clamped at standard levels, is supplied to the input transformer's secondary to condition the network and thereby reject spurious signals.

When the gate voltage is normally at its upper level of +10V, the cathode of CR1 is also at this voltage. The —30V supply places the anode of this diode at —30V because CR2 is conducting toward the +150V MC voltage supply through R2. The 40V (+10V level and —30V supply) is across the high back resistance of nonconducting CR1. This places the control grid at a potential of —30V. The cathode is returned to a —30V supply, but, due to the voltage drop across cathode bias resistor R3, the cathode is less negative than the —30V. This grid-to-cathode voltage biases the tube to the point which allows plate current to flow. Noise or extraneous positive pulses during this time make the cathode of

TABLE 3–49. DRUM WRITE DRIVER, MODELS A AND B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1	Forms input isolating network (with R1)	L1	Peaking coil
C2	Coupling capacitor	R1	Forms input isolating network (with C1)
C3	Compensating capacitor	R2	Plate load resistor for V1 and V2
CR1	Ground clamp for V1 and V2 cathode	R3	Cathode resistor for V1 and V2
CR2, CR3	+10V clamping diodes for grids of V3 and V4	R4-R7	Equalizing resistors
CR4, CR5	—105V clamping diodes for grids of V3 and V4	R8, R9	Voltage divider
CR6, CR7	+10V output clamping diodes	R10	Grid return resistor for V3 and V4
		R11	Cathode load resistor for V3 and V4
		R12, R13	Current-limiting resistors

CR1 more positive, preventing the pulse from affecting the control grid of the tube. The pulse voltage is dropped across the high resistance of the nonconducting diode. An unwanted negative pulse during the +10V time of the gate must exceed —40V to cause the diode to conduct. This eventuality is remote.

The gate is supplied from the same source that indicates the readout from the ferrite core array. When the array is ready to be read out, the gate drops to —30V, applying the voltage to the cathode of CR1. The anode remains at —30V which results in no potential difference across the diode, and the grid-to-cathode voltage remains unchanged.

The gate duration is 2.5 μsec; during this time, a pulse is obtained from the ferrite core array (if a 1 was entered in a core). This negative pulse, between 0.3 and 0.5V, after being stepped up through the input transformer, is a negative pulse of approximately 5.0V peak and of 0.25 to 0.45 μsec duration. Voltages less negative than —30V cannot cause conduction of CR1; but larger negative voltages, such as those obtained during the time of the input from the array, make the cathode of diode CR1 more negative than the anode, causing conduction. This current flowing through resistor R2 and the back resistance of diode CR2 produces a voltage drop which makes the grid negative. The change of plate current produces a large positive increase in plate voltage across inductive load L3.

The signal coupling to the next stage is provided by C1. Diode CR4 is biased negatively on its anode side by the clipping voltage applied through L1, setting a clipping level of —12V to —20V. The pulse from the first stage must exceed the clipping voltage to overcome this bias and cause a transfer of signal to the second stage. This transfer takes place only for a 1 which exceeds +20V; but a 0 input or noise pulses are not large enough to overcome the bias.

The duration of the pulse developed across diode load L2 must be increased to provide a pulse width of 0.6

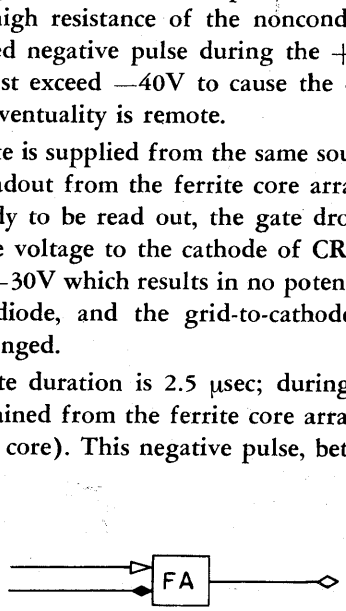


Figure 3—95. Flux Amplifier, Logic Block Symbol

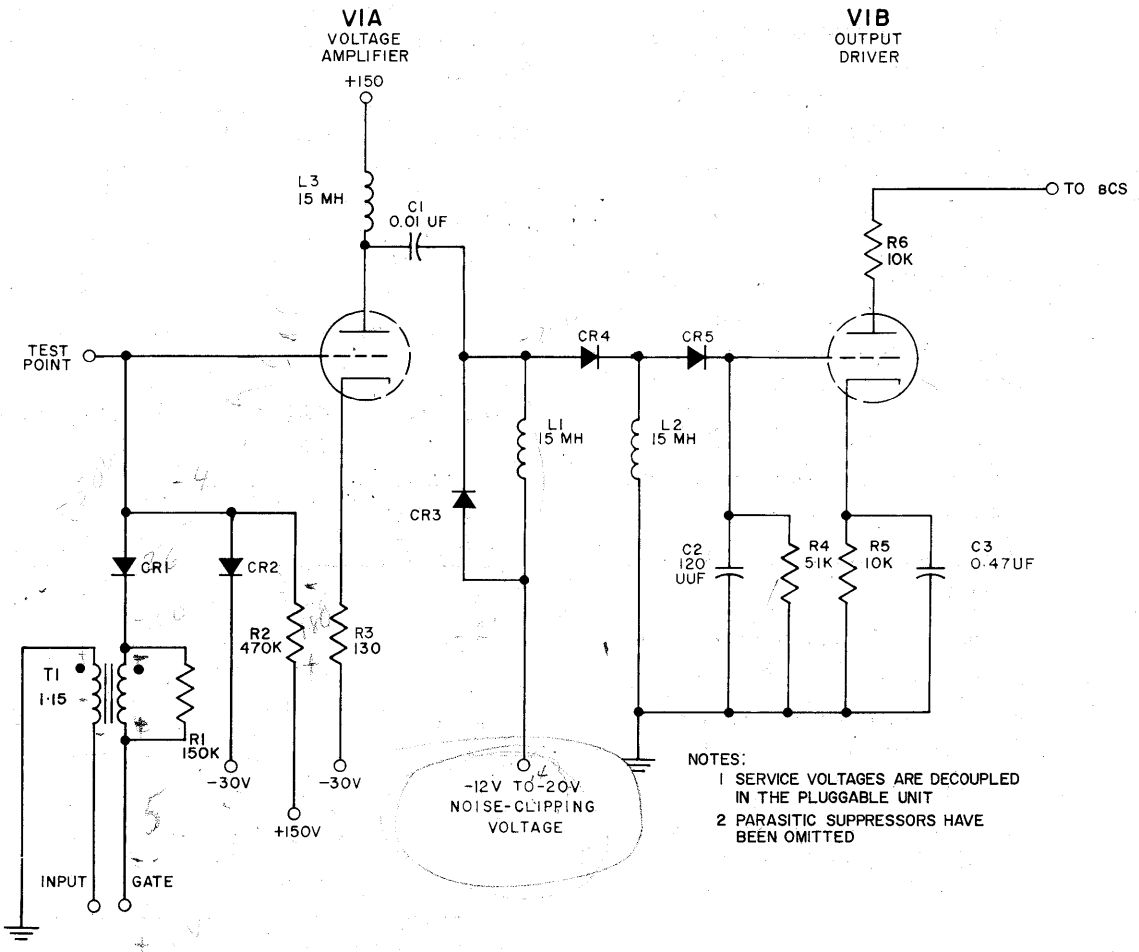


Figure 3—96. Flux Amplifier, Schematic Diagram

μsec for writing into the tape core load of the second amplifier stage. This is accomplished in the following manner. Capacitor C2 charges from ground toward the voltage source which is the pulse across L2. When the pulse level falls, the capacitor discharges through R4. The time constant of C2 and R4 is 6 μsec. The highest positive value reached by the pulse is 4.0V and, 6 μsec (one time constant) later, the pulse amplifier is approximately 2.5V. In discharging to this value in 6 μsec, the voltage at 3 μsec is still sufficient to produce the required tube current through the tape core load of the tube. The tube is initially biased near cutoff. Upon application of the lengthened pulse, plate current rises. When the input pulse reaches the required voltage, the plate current is sufficient to write a 1 into the core load. The input pulse amplitude remains great enough to maintain the plate current at a value sufficient to prime its core load.

TABLE 3–50. FLUX AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Load for T1
R2	Forms part of biasing network in grid circuit of first stage (with CR1 and CR2)
R3	Cathode bias resistor for V1A
R4	Forms part of network which is used to increase duration of pulse developed across diode load L2 (with C2 and CR5)
R5	Cathode bias resistor for V1B
R6	V1B plate load resistor
C1	Coupling capacitor
C2	Forms part of network used to increase duration of load pulse (with R4 and CR5)
C3	Cathode bias bypass capacitor
CR1, CR2	Part of biasing network in grid circuit of V1A (with R2)
CR3	Damps out ringing effects between stages
CR4	Forms part of amplitude-discriminating network (with L1 and L2)
CR5	Forms part of network used to increase duration of load pulse (with R4 and C2)
L1, L2	Forms part of amplitude-discriminating network (with CR4)
L3	Plate load for V1A
T1	Stepup input transformer

3.38 FREQUENCY DOUBLER

3.38.1 Definition and Description

The frequency doubler (FD) is a logic circuit which produces a sawtooth output voltage at twice the frequency of the input sawtooth voltage. The logic block symbol of the FD is shown in figure 3–97. In Input System logic, the FD is part of the azimuth synchronizing circuit. The FD receives the sawtooth output voltage (4.25 to 21.25 cps) from a model A Miller integrator (par. 3.54), doubles its frequency, and feeds it to the level amplifier. Thus, the input frequency (8.5 to 42.5 cps) to the azimuth synchronization circuit is restored.

3.38.2 Principles of Operation

Figure 3–98 is a schematic diagram of the FD. Table 3–51 lists the associated detail parts and their functions. The circuit consists of a cathode follower (V1) and a full wave rectifier (T1, V2A, and V2B).

The input signal is applied to the grid of cathode follower V1. This signal (a triangular wave 40V peak to peak) is developed across the primary of transformer T1. The transformer steps up the peak-to-peak voltage by 3 and provides a triangular wave output across its secondary winding which varies about a d-c level of —185V. With no input signal applied, the voltage divider of R3 and R4 between —300V and ground keeps the cathodes and plates of V2A and V2B at —185V. As the input triangular wave begins its positive excursion at the grid

TABLE 3–51. FREQUENCY DOUBLER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	V1 grid resistor
R2*	Plate load for FD and grid return for LEA circuit
R3, R4	Voltage divider which fixes maximum negative output voltage at —185V
C1**	Coupling capacitor
T1	Stepup transformer

**Part of level amplifier*
***Part of Miller integrator*

of V1, V2A cathode voltage becomes less negative and V2B cathode voltage becomes more negative. As a result, V2B conducts and continues to conduct as long as its cathode voltage is more negative than —185V. When the input triangular wave begins its negative excursion, the cathode of V2A becomes more negative and the cathode of V2B becomes less negative. Tube V2A then starts to conduct and continues to as long as V2A cathode voltage is more negative than —185V. Thus, it becomes apparent that electron flow during the positive-going and negative-going half cycles of the input wave is in the same direction across output load resistor R2 toward the —185V point. Consequently, each complete cycle of input signal in the FD results in two cycles of output signal.

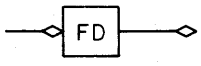


Figure 3–97. Frequency Doubler, Logic Block Symbol

3.39 INPUT AMPLIFIER, MODEL B

3.39.1 Definition and Description

The model B input amplifier (BIA), employed in the 256² memory, functions as an inverter, amplifier, and level setter. The logic block symbol for the BIA is shown in figure 3–99. The inputs to the BIA are standard levels of +10 and —30V obtained from a diode matrix in the memory address register; the outputs are non-standard levels of —240 and —150V, respectively. These outputs are fed to associated switch drivers as conditioning levels. (A —240V level will cut off the switch driver; a —150V level enables the switch driver to conduct.)

3.39.2 Principles of Operation

The schematic diagram of the BIA, together with related waveforms, is shown in figure 3–100. Table 3–52 lists the associated detail parts and their functions. The BIA consists of three stages: an input cathode follower (V1), an amplifier (V2), and an output cathode follower (V3). The input cathode follower is employed as

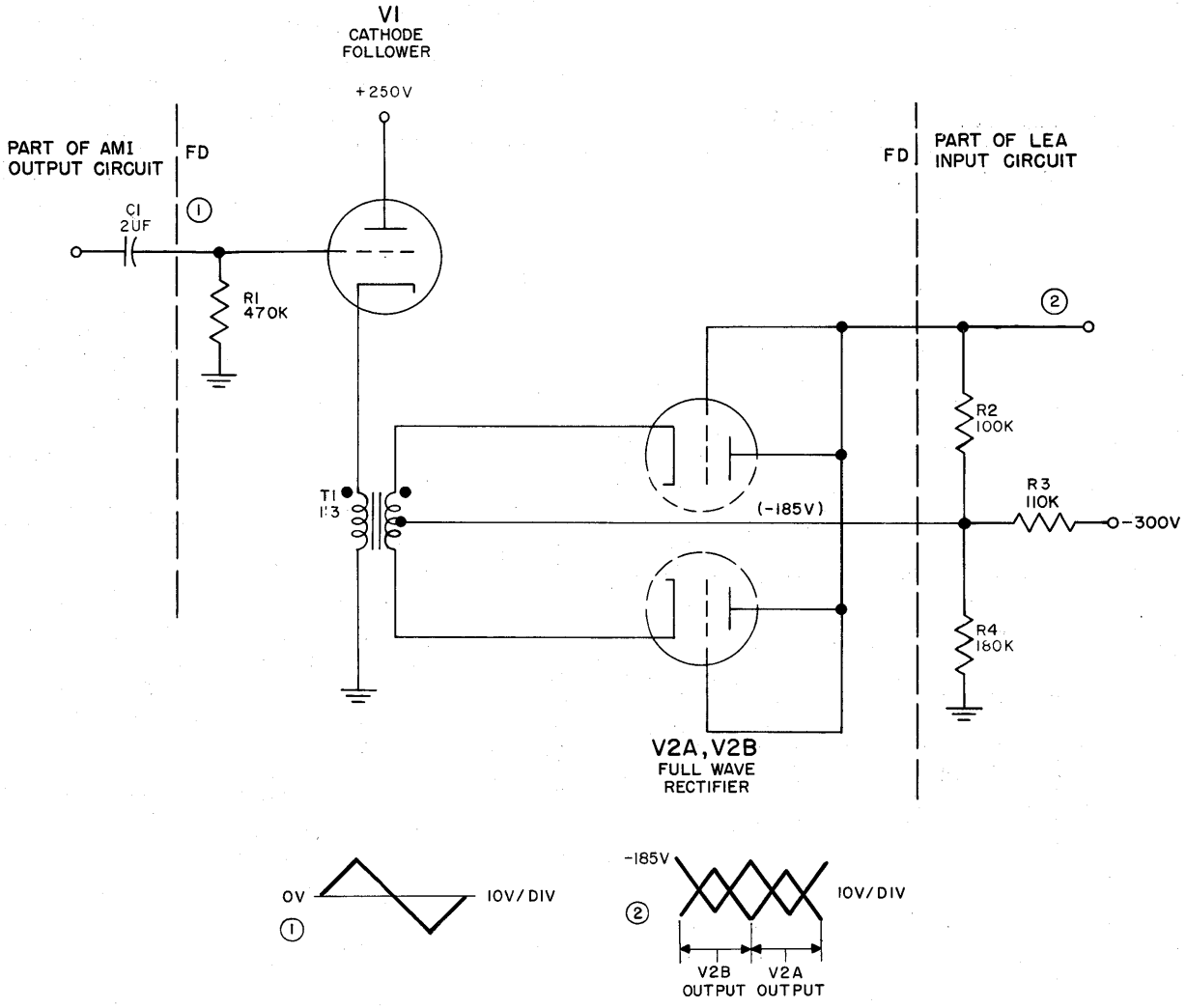


Figure 3–98. Frequency Doubler, Schematic Diagram

a buffer between the high output impedance of the associated input diode matrix and the low input impedance of the amplifier.

The inputs supplied by the diode matrix are either +10 or −30V levels. Assume that the prevailing input level to the BIA is +10V; the voltage appearing at the grid of the input cathode follower is clamped at +5V by diode CR1. This clamping potential is obtained from the voltage divider consisting of resistors R2 and R3. The resulting potential at the cathode of V1 is +5V. The exponential rise noted in waveform C is due to the charge curve of capacitor C2. The grid voltage of V2 is established at −148V by the voltage divider consisting of resistors R5, R6, and R7 returned to the cathode of V3 whose potential is at −240V. Diodes CR2 and CR3 are cut off during this period of operation. The positive spike noted in waveform D at the transition time between the two states of operation for the BIA is due to capacitor C2 charging to the established d-c levels. Since the cathode of V2 is returned to −150V, the grid of V2 is slightly positive with respect to its cathode, causing grid current to flow. In order to avoid exceeding the grid dissipation limit of V2, specifically during the initial period of the C2 charge curve, diode CR4 is placed between the grid and cathode of V2 to absorb a portion of the grid current flow. As a result of the bias level established for V2, its plate voltage at this time is −40V. The voltage divider, comprised of resistors R11 and R12, sets the grid voltage of V3 at −273V. This voltage is held at this level by clamping diodes CR5 and CR6. With the grid voltage at −273V, the resultant cathode potential is −240V. Thus, with a +10V input level to the BIA, a nonstandard level of −240V is established at the output.

When the input level shifts to −30V, the cathode potential of V1 decreases toward −5V. The exponential decrease of this voltage, illustrated in waveform C, is due to the discharge of capacitor C2. The voltage change at the cathode of V1 is coupled through C2 to the grid of V2. The resultant drop in the grid potential of V2 causes the plate voltage of V2 to rise from −40V to +65V. This change of 105V is coupled to the grid of V3 through capacitor C3, causing its grid potential to increase to −170V (diodes CR5 and CR6 are cut off at this time). As a result of this increase, the output cathode potential of V3 rises to −150V. Thus, with a −30V input

Figure 3–99. Input Amplifier, Model B, Logic Block Symbol

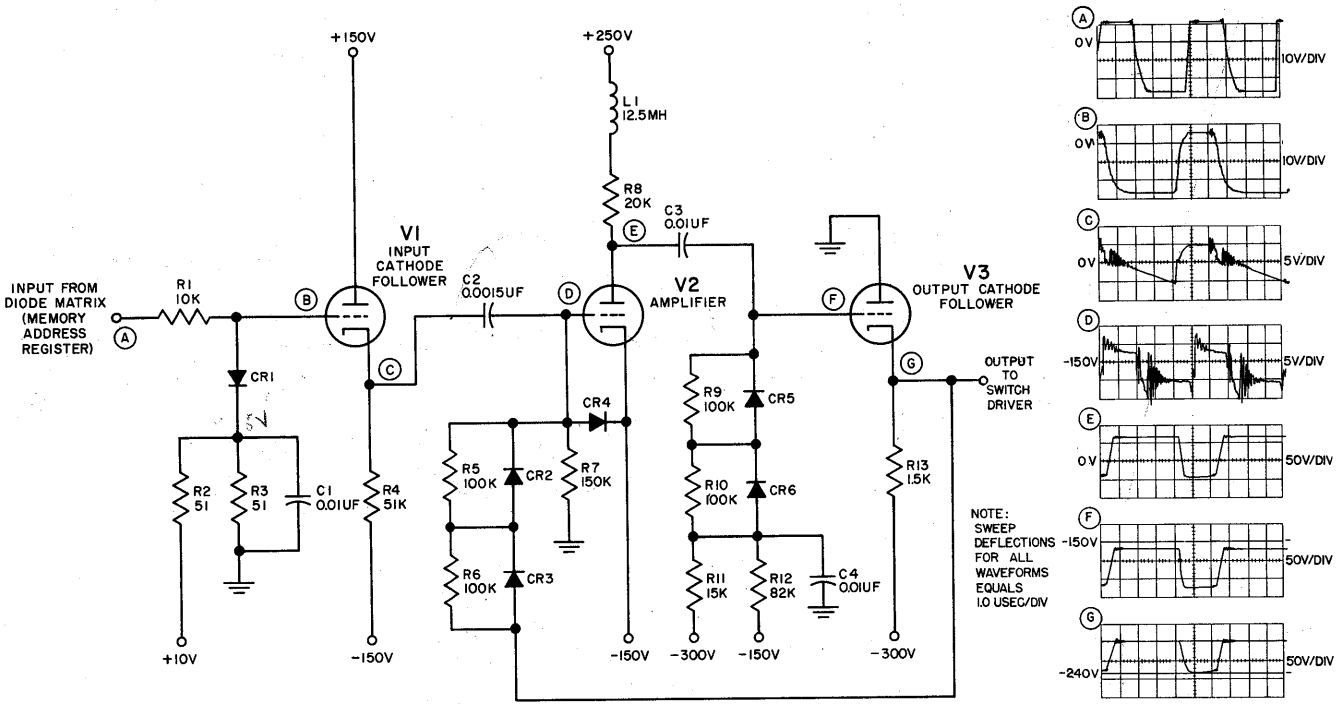


Figure 3–100. Input Amplifier, Model B, Schematic Diagram

TABLE 3–52. INPUT AMPLIFIER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1	Bypass capacitor	R2, R3	Voltage divider
C2, C3	Coupling capacitors	R4	Cathode load resistor for V1
C4	Bypass capacitor	R5, R6	Part of voltage divider (with R7) returned to cathode of V3 and equalizing resistors for CR2 and CR3, respectively
CR1	Crystal diode, clamps V1 grid at +5V	R7	Part of voltage divider (with R5 and R6) and grid-limiting resistor for V2
CR2, CR3	Crystal diodes, clamp V2 grid at upper output level	R8	Plate load resistor for V2
CR4	Crystal diode, grid current bypass for V2	R9, R10	Voltage equalizing resistors for CR5 and CR6, respectively
CR5, CR6	Crystal diodes, clamp V3 grid at −273V	R11, R12	Voltage divider
L1	Peaking coil	R13	Cathode load resistor for V3
R1	Grid-limiting resistor		

level, a nonstandard level of −150V is developed by the BIA and applied to the associated switch drivers. This output level is also fed back to the grid of V2 through CR2 and CR3 to stabilize this upper output level. Diodes CR2 and CR3 remain cut off until the output voltage becomes more positive than the voltage appearing at the grid of V2. When the diodes conduct, the output voltage controls the grid voltage of V2. An increase in the output causes the grid of V2 to become more positive, decreasing the plate voltage of V2. This change is coupled to V3 with a resultant decrease in the grid voltage of V3 and consequently a decrease in the output level. The converse occurs for a decrease in the output voltage. It is in this manner that this degenerative feedback loop stabilizes the upper output level. Diodes CR2 and CR3 are cut off when the lower output level is developed. The negative voltage spike at the grid of V2 (see waveform D) is due to the delay in the feedback signal before CR2 and CR3 are made to conduct. Refer to table 3–52 for the function of detail parts not discussed.

3.40 INVERTER, MODEL B

3.40.1 Definition and Description

The model B inverter (BI) is a logic circuit which produces a negative level when the input is a positive standard level and a positive level when the input is a negative standard level. The logic block symbol for the BI is shown in figure 3–101.

3.40.2 Principles of Operation

Figure 3–102 is the schematic diagram of the BI. Table 3–53 lists the associated detail parts and their functions. The circuit consists of an amplifier and a cathode follower whose output is clamped at −30V and +10V. In special applications, this output is clamped at +15V.

When a −30V level is applied to the grid of V1, the tube is cut off. Diode CR1 conducts, due to the negative potential on its cathode, and clamps the cathode of V1

TABLE 3–53. INVERTER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Speedup capacitor, improves rise and fall time
CR1	Crystal diode clamps V1 cathode at ground
CR2	Crystal diode clamps output at +15V (special application)
CR3	Crystal diode clamps output at −30V
CR4	Crystal diode clamps output at +10V
R1	Plate load resistor for V1
R2	Cathode resistor for V1
R3, R4	Voltage divider network
R5	Cathode load resistor for V2
R6	CR4 current-limiting resistor

at ground. With V1 cut off, the plate voltage rises to +194V, a function of the voltage divider formed by resistors R1, R3, and R4. With +194V at the plate of V1, a potential of 494V appears across the voltage divider consisting of R3 and R4. The resulting voltage division would place the grid of V2 at 30V; however, the grid does not become more positive than +10V. Crystal diode CR4 clamps the cathode of V2 at +10V; a grid current flows through resistors R3 and R1, and grid limiting prevents the grid from becoming more positive than +10V. The output, at the cathode of V2, is a +10V level.

When a positive standard level (+10V) is applied to the grid of V1, the tube conducts. The resulting plate current, maintained at a relatively constant value due to cathode degeneration, develops a voltage across cathode resistor R2. This raises the potential on the V1 cathode and CR1 is cut off. Conduction of V1 reduces its plate voltage to +50V. The potential across the voltage divider is now 350V, placing the grid of V2 at −67V. Cathode follower V2 is now biased beyond cutoff. Diode CR3 conducts, due to the negative potential on its cathode, and clamps the output at −30V.

Diode CR2 is part of a special clamping circuit which becomes operative if the +10V clamping circuit fails. The BI drives from 1 to 15 lines which are connected to the input diode circuits of as many display consoles. If the +15V special clamping circuit was omitted, all the display console input diodes connected to the BI would be destroyed whenever a +10V clamping diode burned out.

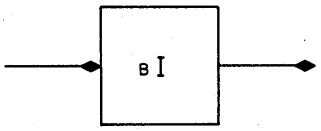


Figure 3–101. Inverter, Model B, Logic Block Symbol

3.41 ISOLATION CIRCUIT, MODEL A

3.41.1 Definition and Description

The model A isolation circuit (AIC) is a nonlogic circuit which allows the 25-μsec positive load-shift-register pulse to set a core but prevents the subsequent −30V level from clearing the same core. The logic block symbol for the AIC is shown in figure 3–103.

3.41.2 Principles of Operation

Figure 3–104 is the schematic diagram for the AIC. The circuit consists of a type Y crystal diode and a 1,500-ohm resistor in series. The AIC performs the above-mentioned function by allowing current to flow only when its anode is more positive than the cathode. This action is made possible by the crystal diode utilized in the circuit. R1 is a current-limiting resistor.

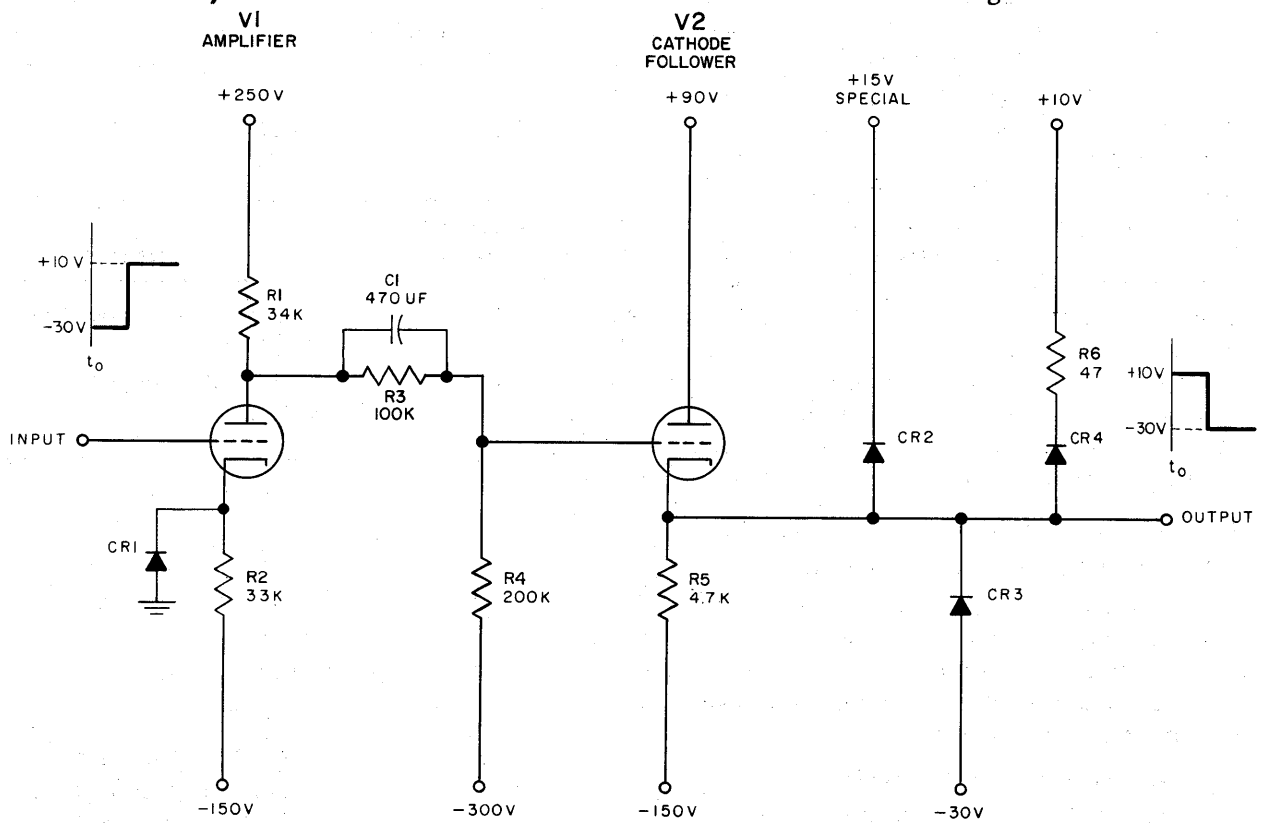


Figure 3–102. Inverter, Model B, Schematic Diagram

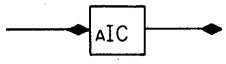


Figure 3–103. Isolation Circuit, Model A, Logic Block Symbol

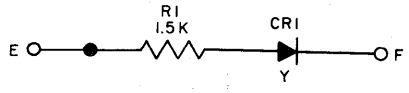


Figure 3–104. Isolation Circuit, Model A, Schematic Diagram

3.42 LEVEL AMPLIFIER

3.42.1 Definition and Description

The level amplifier (LEA) is a nonlogic low-gain amplifier. The logic block symbol of the LEA is shown in figure 3–105. In Input System logic, the LEA is the output stage of the triangular wave generator in the azimuth synchronizing circuit group. The LEA receives a triangular wave (8.5 to 42.5 cps) from the frequency doubler (par. 3.38) and feeds an amplified signal to an automatic gain circuit (par. 3.6) and a phase splitter (par. 3.59).

Figure 3–105. Level Amplifier, Logic Block Symbol

3.42.2 Principles of Operation

Figure 3–106 is the schematic diagram for the LEA. Table 3–54 lists the associated detail parts and their functions. The LEA employs negative current feedback to produce a stable output at the expense of gain.

The unbypassed cathode resistor determines the current through V1. The 30V variation at the grid produces a 30V variation at the cathode. A 30V change at the cathode is produced by a 1.87-ma change in current through R5. A 1.87-ma change through R4 produces an 81V change in plate voltage. Thus, a 30V peak-to-peak input to V1 appears as an 81V peak-to-peak signal at the output voltage divider. The full output voltage is applied to the phase splitter. One-half of the output

TABLE 3–54. LEVEL AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Coupling capacitor
C2	Bypass capacitor
R1	Grid return
R2, R3	Grid-biasing voltage divider
R4	Plate load
R5	Cathode feedback resistor
R6, R7	Output voltage divider

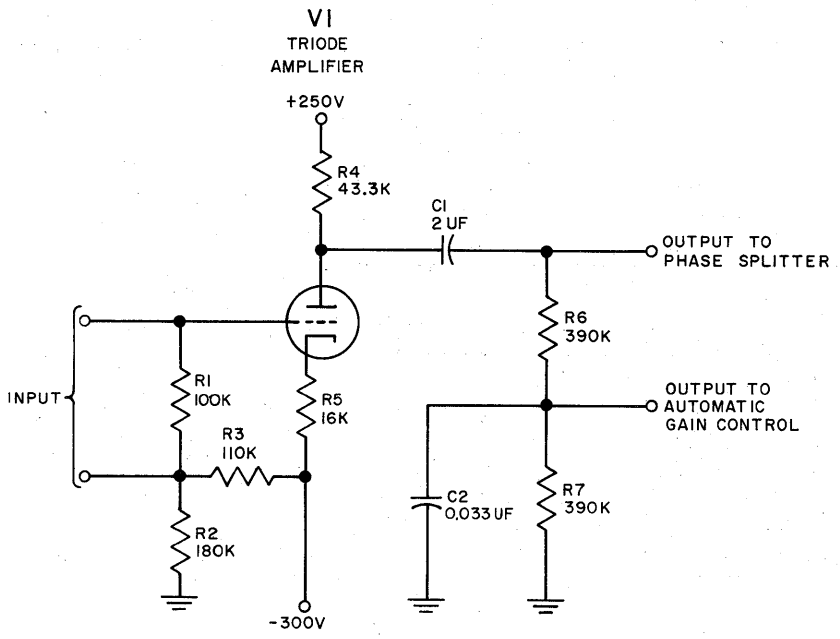


Figure 3–106. Level Amplifier, Schematic Diagram

voltage obtained at the junction of R6 and R7 is applied to the automatic gain control circuit.

The time constant of R2, R6, and R7 is large with respect to the period of the output signal so that the triangular wave is coupled to the succeeding circuits without distortion.

3.43 LEVEL ORIGINATOR, MODEL A

3.43.1 Definition and Description

The model A level originator (ALO) is a nonlogic circuit that produces a standard level output as a function of a nonstandard level input. Figure 3–107 is the logic block symbol of the ALO. In Central Computer logic, the ALO produces a positive standard level output whenever the associated machine printer, punch, or reader) is not ready for operation. At all other times, the output is a negative standard level.

3.43.2 Principles of Operation

Figure 3–108 is the schematic diagram for the ALO. The LO input line is connected to a relay contact which is either at ground or an open circuit. When the input is at ground, resistors R1 and R2 are a voltage divider between +90V and ground. Voltage divider action would set the junction of R1 and R2 at +15V. However, CR1 conducts to clamp the junction and the output of the LO at +10V. Similarly, when the input line is open-circuited, resistors R1, R2, and R3 are a voltage divider between +90V and —150V. Voltage divider action would set the junction of R1 and R2 at —60V. However, diode CR2 conducts to clamp the junction and the output of LO at —30V.

3.44 LIGHT GUN, MODEL B

3.44.1 Definition and Description

The model B light gun (BLG), a nonlogic circuit, is a photoelectric device which is employed to generate a pulse proportional to the light received from a bright point or character on the face of the SD CRT. The logic block symbol for the BLG is shown in figure 3–109.

3.44.2 Principles of Operation

3.44.2.1 Basic Operation

Figure 3–110 is the schematic diagram for the BLG. Table 3–55 lists the associated detail parts and their func-

Figure 3–107. Level Originator, Model A, Logic Block Symbol

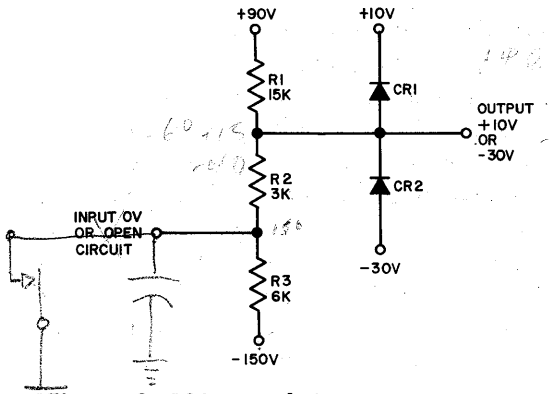


Figure 3–108. Level Originator, Model A, Schematic Diagram

Figure 3–109. Light Gun, Model B, Logic Block Symbol

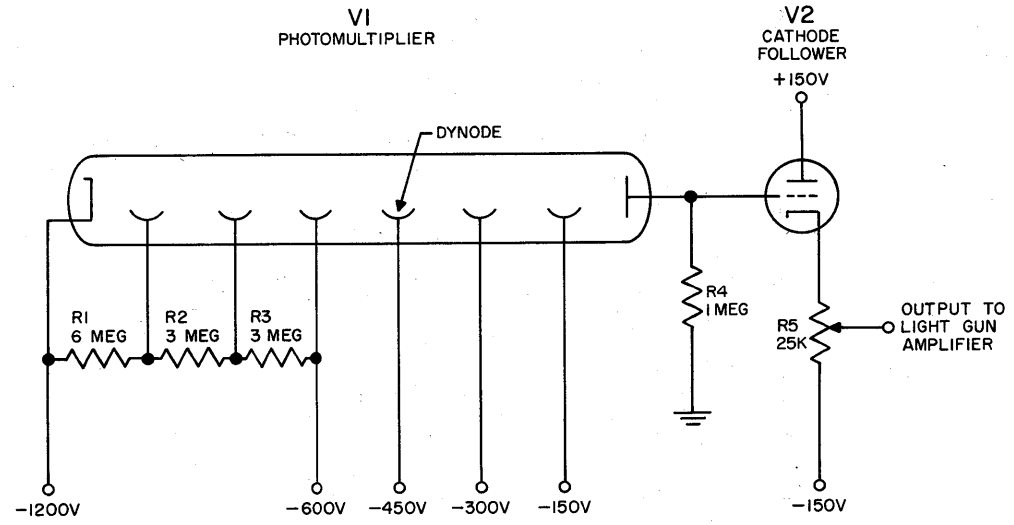


Figure 3–110. Light Gun, Model B, Schematic Diagram

tions. The circuit consists of a photomultiplier tube, a cathode follower, and associated detail parts. The photomultiplier produces electron flow proportional to the incident light falling on its photosensitive cathode. Six dynodes in the photomultiplier are coated with an electron emissive substance. Each dynode emits approximately four times the number of electrons that strike it, effecting a current multiplication from cathode to anode of approximately 3,000. A pulse is developed in the plate circuit of V1 and applied to the cathode follower.

3.44.2.2 Detailed Operation

A —1,200V potential is applied to the cathode of V1. Potentials approaching ground, in successive steps, are applied to the dynodes of V1. The resulting electron multiplication, between the cathode and the plate, develops a negative pulse across plate load resistor R4. The magnitude of this pulse is a function of the light striking the photosensitive cathode of V1. This voltage is coupled directly to the grid of V2. The cathode of V2 follows the grid swing and the resulting negative pulse is fed to the light gun amplifier from the moving arm of potentiometer R5. The amplitude of the output is adjusted by means of R5.

TABLE 3–55. LIGHT GUN, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2, R3	Form voltage divider network
R4	Plate load resistor for V1 and d-c grid return for V2
R5	Output amplitude control
V1	Photomultiplier tube
V2	Cathode follower triode

3.45 LIGHT GUN AMPLIFIER, MODEL B

3.45.1 Definition and Description

The model B light gun amplifier (BLGA) is a nonlogic circuit which amplifies the output pulse of the light gun. The logic block symbol for the BLGA is shown in figure 3–111. The BLGA consists of an amplifier, a 3-way AND circuit, and a pulse generator. For purposes of simplification, the operation of the amplifier section and pulse generator section are described separately.

3.45.2 Principles of Operation

3.45.2.1 Amplifier Section

The schematic diagram of the amplifier section of the BLGA is shown in figure 3–112. Table 3–56 lists the associated detail parts and their functions.

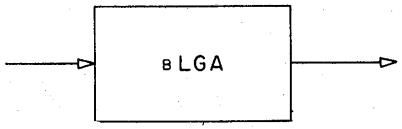


Figure 3–111 Light Gun, Amplifier, Model B, Logic Block Diagram

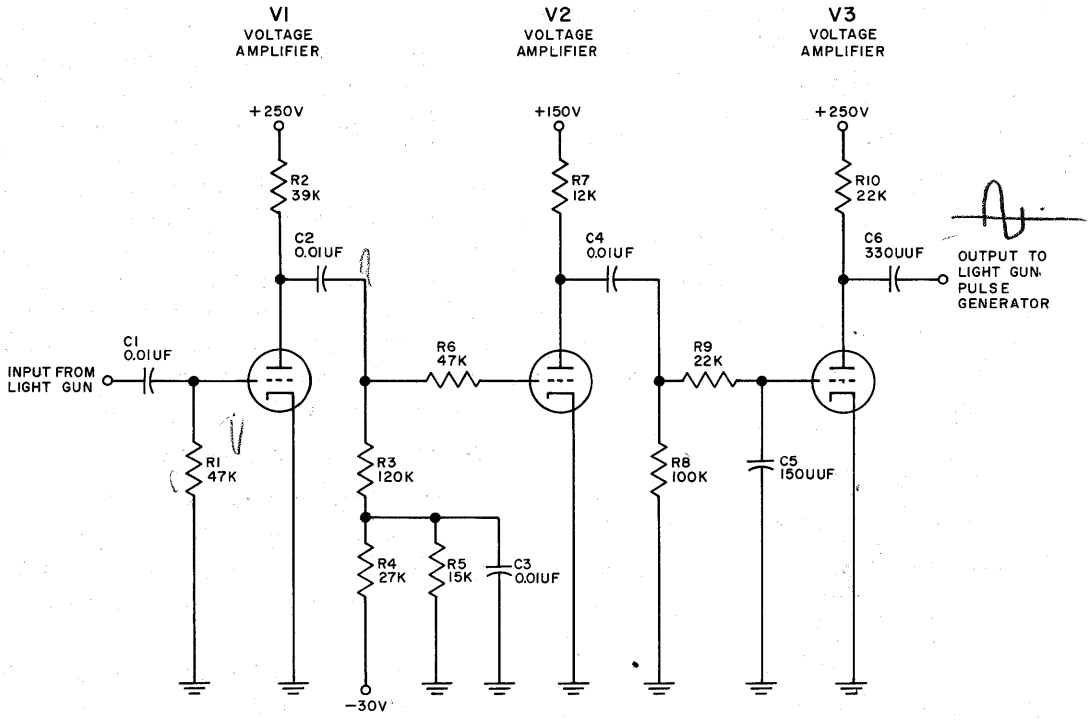


Figure 3–112. Light Gun Amplifier, Model B, Amplifier Section, Schematic Diagram

The negative pulse from the light gun is coupled through capacitor C1 to the grid of V1. The pulse may range in amplitude from 3 to 10V with a duration of 25 to 60 μsec. V1 is normally conducting. The negative-going input pulse reduces the plate current, producing a rise in the plate voltage of V1. The positive-going output pulse is coupled from the plate V1 through C2 to the control grid of V2.

As a result of the bias (—10.7V) developed across resistor R5, V2 is normally cut off. The positive pulse of the grid of V2 overcomes this bias and V2 conducts. Consequently, the plate voltage of V2 drops, developing a negative-going output pulse. This pulse is coupled through C4 to normally conducting V3, raising the plate potential. The output of V3, a positive pulse, is coupled through capactior C6 to the input circuit of the light gun pulse generator.

3.45.2.2 Pulse Generator Section, Basic Operation

The pulse generator section of the BLGA is a logic circuit that develops a 10-μsec pulse. The circuit generates an output when a preceding 3-way AND circuit is conditioned by the coincidence of a positive level, positive gate, and positive pulse. Figure 3–113 is the schematic diagram for the light gun pulse generator. Table 3–57 lists the associated detail parts and their functions.

TABLE 3–56. LIGHT GUN AMPLIFIER, MODEL B, AMPLIFIER SECTION, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input coupling capacitor
C2	Coupling capacitor
C3	Bypass capacitor
C4	Coupling capacitor
C5	Part of low pass filter (with R19)
C6	Output coupling capacitor
R1	Grid return for V1
R2	Plate load resistor for V1
R3	Grid return for V2
R4, R5	Voltage divider
R6	Grid current-limiting resistor for V2
R7	Plate load resistor for V2
R8	Grid-return resistor for V3
R9	Part of low pass filter (with C5)
R10	Plate load resistor for V3

The positive output from the 3-way AND input circuit triggers thyratron V1. When this thyratron conducts, its cathode potential increases. With V1 conducting, the delay line consisting of C12, C13, C14, L2, and L3, which was charged to +250V, discharges. The plate of V1 falls with the delay line until, at the end of 10-μsec (determined by the delay line), the plate potential reaches the extinguishing level, and V1 stops conducting. A 10-μsec positive pulse is developed at the output of the pulse generator.

3.45.2.3 Pulse Generator Section, Detailed Operation

The positive output from the amplifier is clamped at +10V by crystal diode CR1. This is one of three inputs to the AND circuit consisting of crystal diodes CR2, CR3, CR4, and resistor R5. The other inputs to the AND include a +10V level, applied when the light gun trigger S1 is depressed, and the pass light gate from the manual input element. In the absence of any of these inputs, the output of the AND is clamped at —30V by CR5. When the AND circuit is conditioned by these three inputs, the positive pulse is coupled through capacitor C5 to the control grid of normally nonconducting thyratron V1.

Due to the voltage divider comprised of R7 and R11, the control grid of V1 is at —41V. Since the cathode of V1 is tied to —30V, the resulting bias (—11V) is sufficient to hold the grid of V1 below igniting potential. The positive pulse input to the control grid overcomes this bias, firing the thyratron. The plate voltage decreases, causing the delay line, which was charged to +250V, to discharge (this delay line will discharge in 10-μsec). At the end of 10-μsec, the plate voltage is reduced to its extinction potential. Relay K1 is energized when V1 is fired. Indicator I1 is lit and aim light I2 is extinguished, indicating that the thyratron has fired and a 10-μsec positive pulse has been developed. The other set of contacts apply —30V to one side of the relay coil to maintain K1 in the energized state after V1 is extinguished. The delay line and the plate of V1 are held at —30V as long as S1 is depressed and K1 is energized. Releasing switch S1 de-energizes the relay. This extinguishes I1 and causes the aim light, I2, to glow.

3.46 LOGIC DRIVER, MODEL A

3.46.1 Definition and Description

The model A logic driver (ALD) is a nonlogic circuit which produces a continuous sine wave at ground potential. The logic block symbol for the ALD is shown in figure 3–114.

In Output System logic, the ALD is used in the model A data conversion transmitter to drive two 2-way AND circuits.

TABLE 3-57. LIGHT GUN AMPLIFIER, MODEL B, PULSE GENERATOR SECTION, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1	Coupling capacitor	L2, L3	Part of 14 section delay line (with C5, C6, and C7)
C2	Improves response of relay K1	R1	Current-limiting resistor
C3	High-frequency bypass for V1 grid	R2	Part of 3-way AND circuit (with CR2, CR3, and CR4)
C4	High-frequency bypass for V1 screen grid	R3	Part of voltage divider (with R6)
C5, C6, C7	Part of I4 section delay line (with L2 and L3)	R4	Grid return for V1
CR1	Positive clamp for input from light gun amplifier	R5	Grid current-limiting resistor for V1
CR2, CR3, CR4	Part of 3-way AND circuit (with R2)	R6	Part of voltage divider (with R3)
CR5	—30V clamp for AND output	R7	Current-limiting resistor for V1
K1	Relay, operates indicator and aim lights	R8	Parallel damping resistor for K1
L1	Eliminates spike on leading edge of plate pulse	R9	Cathode load for V1
		R10	Screen grid current-limiting resistor
		R11	Isolating resistor
		S1	Light gun trigger switch

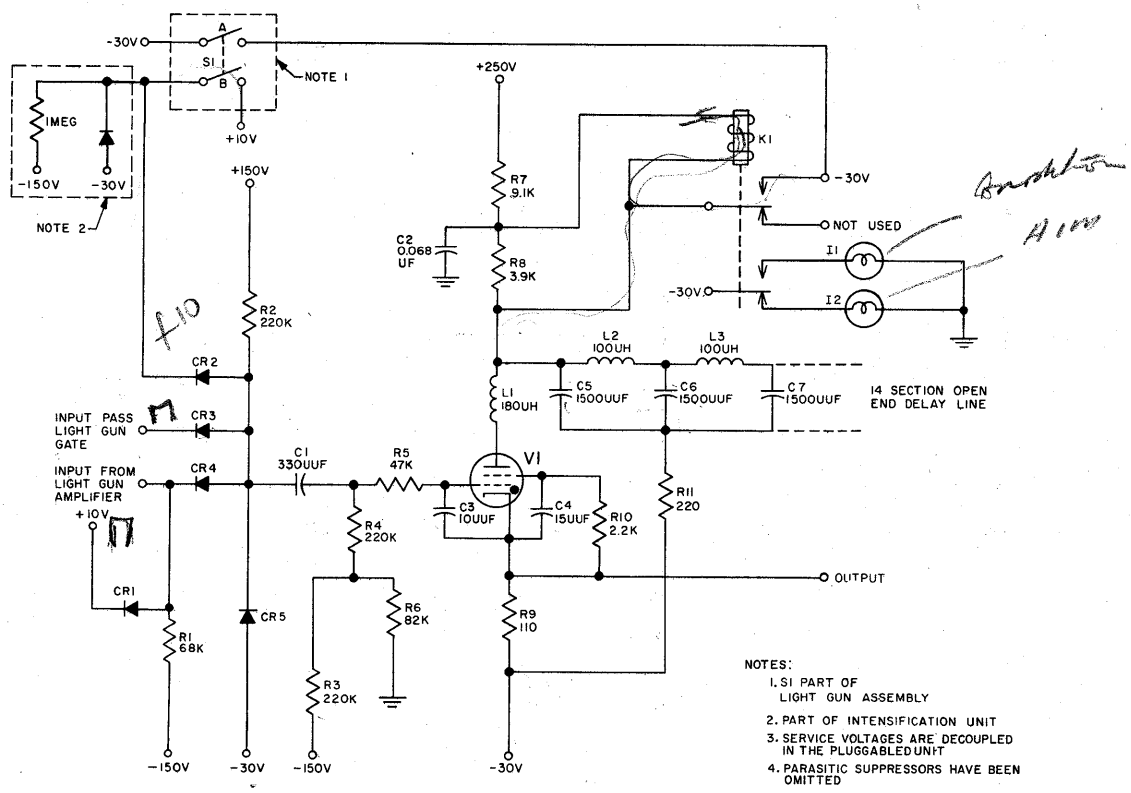


Figure 3-113. Light Gun Amplifier, Model B, Pulse Generator Section, Schematic Diagram

3.46.2 Principles of Operation

Figure 3–115 is the schematic diagram for the ALD. Table 3–58 lists the associated detail parts and their functions. The circuit consists of an ac-coupled cathode follower with an inductive cathode load. The input signal is a continuous sine wave of 1,300 cycles with a peak-to-peak amplitude of approximately 11.5V. The cathode load consists of a 2.5-henry choke whose impedance is more a function of frequency than of d-c current. The choke is connected to the voltage divider consisting of R3 and R4; this connection is made to compensate for the d-c voltage drop across the choke. The values of R3 and R4 are chosen to provide approximately a ground level for the output signal which is identical with the input except that its amplitude is 11.4V.

TABLE 3–58. LOGIC DRIVER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1
R2	Cathode resistor
R3, R4	Voltage divider which compensates for d-c voltage drop across L1
C1	Coupling capacitor
C2	Capacitor bank (four 1-μμf capacitors in parallel) serving as part of cathode load (with L1)
L1	Choke, serving as part of cathode load (with C2)

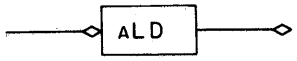


Figure 3–114. Logic Driver, Model A, Logic Block Symbol

3.47 LOGIC GATE

3.47.1 Definition and Description

The logic gate circuit (LGT) is a logic circuit which produces either a 1,300-cycle sine wave or a ground level, depending on its input conditions. The logic block symbol for the LGT is shown in figure 3–116.

3.47.2 Principles of Operation

Figure 3–117 is the schematic diagram for the LGT. Table 3–59 lists the associated detail parts and their

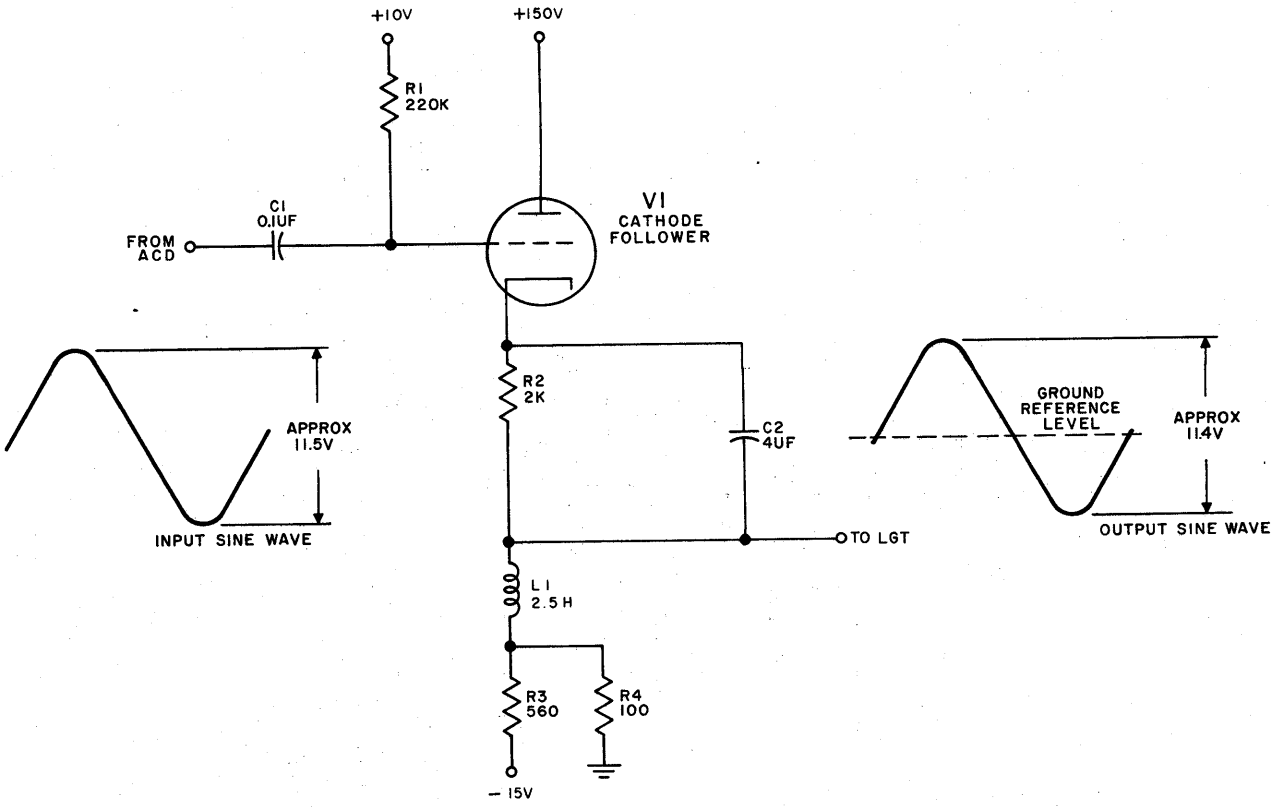


Figure 3–115. Logic Driver, Model A, Schematic Diagram

functions. The inputs to the LGT are taken from a flip-flop which is controlled by data pulses from the output storage section and timing pulses from the output control element. A 1,300-cycle sine wave timing signal is also supplied from the logic driver. Standard AND and OR circuits are used for logical gating. The logic driver supplies current to the AND circuit when the other AND input is up at +10V. The output from the AND circuit is −30V when the input from the flip-flop is −30V and an 11.8V peak-to-peak sine wave when the input from the flip-flop is at +10V.

TABLE 3–59. LOGIC GATE, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Form split cathode load for cathode follower
R3	Load resistor for AND circuit
R4	Load resistor for OR circuit
C1	Compensating capacitor
CR1, CR2	Standard AND circuit
CR3, CR4	Clamps OR circuit input at −30V
CR5, CR6	Standard OR circuit

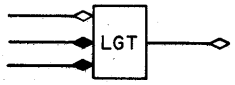


Figure 3–116. Logic Gate, Logic Block Symbol

To remove the sine wave representing sync or data information from the 30V pedestal, the AND circuit output is fed to its associated OR circuit which also receives a ground or −30V level input from the OR driver cathode follower. The cathode follower uses a split cathode load resistance in its cathode in order to obtain an output of either ground or −30V. When the output of the AND circuit is at −30V, the cathode follower output is at ground potential. Consequently, the OR circuit output is at ground when no data or sync signals are present. When data or sync signals are present, the OR circuit output consists of 12V peak-to-peak gated sine waves at ground reference level.

3.48 MAPPER INTENSIFICATION CIRCUIT, MODEL A

3.48.1 Definition and Description

The model A mapper intensification circuit (AMIC) is a logic circuit which controls the intensity of the

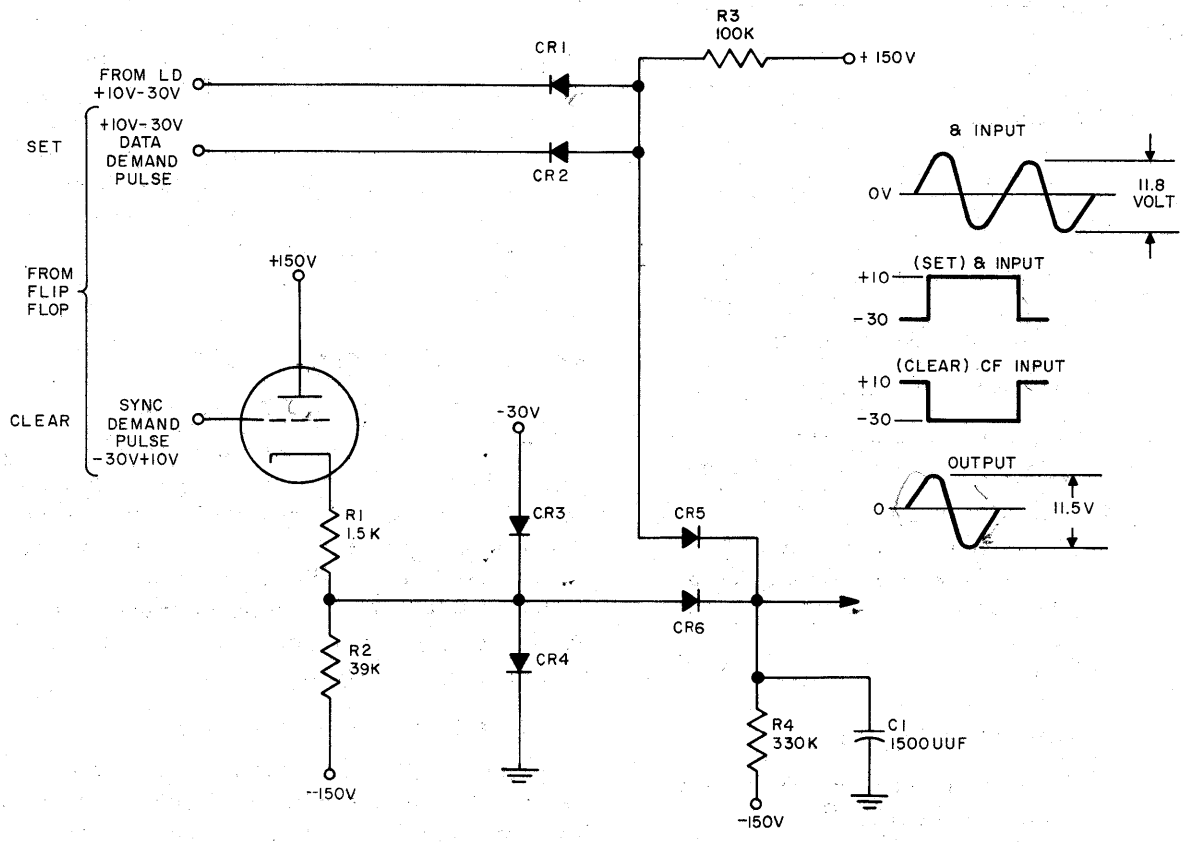


Figure 3–117. Logic Gate, Schematic Diagram

mapper CRT. A second function of the AMIC is to control the contrast between the raw targets and the reintensified targets. The logic block symbol for the AMIC is shown in figure 3–118.

Figure 3–118. Mapper Intensification Circuit, Model A, Logic Block Symbol

3.48.2 Principles of Operation

3.48.2.1 Basic Operation

Figure 3–119 is the schematic diagram of the AMIC. Table 3–60 is the associated list of detail parts and their functions. The AMIC consists of a model BSS and an OR circuit used in conjunction with level and amplitude controlling devices. Upon receipt of a raw target-data standard pulse, the single-shot multivibrator is activated and produces a 43-μsec intensify pulse. This pulse passes through a contrast control circuit which controls the pulse amplitude and is then applied to an OR circuit. The output of the OR circuit first passes through a cutoff control circuit and causes a spot to be produced on the face of the CRT. This spot which is produced by the 43-μsec intensify pulse is of normal brightness. If the mapper console operator does not mask out this target signal, the spot is picked up by a photomultiplier tube and this signal is sent to the input and shifting logic. In the input and shifting logic, a flip-flop produces a 180-μsec pulse which is then added to the 43-μsec pulse in the OR circuit. The combined pulse is then modified and applied to grid 1 of the CRT, causing the target spot to be reintensified.

TABLE 3–60. MAPPER INTENSIFICATION CIRCUIT, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Potentiometer which forms part of CONTRAST control (with CR2)
R2	Current-limiting resistor for CR3
R3	Part of OR circuit (with CR3, CR4)
R4, R7	Form voltage divider which varies plate voltage of V1A with R6 as bias control potentiometer
R8	Bias resistor for CRT grid 1
C1	Coupling capacitor which isolates OR circuit output from CRT grid 1 output
CR1	Diode crystal which prevents one-half of OR circuit from going below −30V
CR2	Part of CONTRAST control (with R1)
CR3, CR4	Form OR circuit (with R3)
CR5	Serves as clamper which prevents other half of OR from going below −30V

3.48.2.2 Detailed Operation

The OR circuit formed by crystal diodes CR3, CR4, and resistor R3 passes intensifying or reintensifying pulses. The output of the CR3 portion of the OR circuit is determined by potentiometer R1 which sets the changing level of CR2. This level controls the amplitude of the pulse going through CR3 but does not affect the pulse going through CR4. At the maximum setting of R1 (+10V) the intensify pulse is of the same amplitude as that of the reintensify pulse. Diode CR5 prevents the voltage at the other portion of the OR circuit from going below −30V.

Coupling capacitor C1 is necessary since the outputs of the OR circuit and grid 1 of the CRT are at different d-c levels and must be isolated. The grid bias of the CRT is provided through resistor R8 and V1A in the following manner. Voltage divider R4, R5, R6, and R7 varies the plate voltage of V1A, which in turn allows control of current in R8. The voltage drop across R8 provides the proper bias for CRT grid 1. This variable bias is necessary to compensate for inherent cutoff characteristics of different CRT's. Diode V1B serves as a clamper which prevents grid 1 from going excessively positive in the event potentiometer R1 and potentiometer R6 are simultaneously out of adjustment.

3.49 MAPPER SWEEP GENERATOR

3.49.1 Definition and Description

The mapper sweep generator (MSG) is a logic circuit which develops a sawtooth signal output from an azimuth pulse input. The logic block symbol for the MSG is shown in figure 3–120. In Input System logic, the MSG is used in the GFI mapper console. The circuit utilizes a 5-μsec positive pulse to trigger a generator which then provides a sawtooth current to deflect the electron beam radially at a linear rate.

3.49.2 Principles of Operation

Figure 3–121 is the schematic diagram for the MSG. Table 3–61 lists the detail parts and their functions. The circuit consists of a thyratron sawtooth generator, a cathode follower, a feedback amplifier, and a yoke driver.

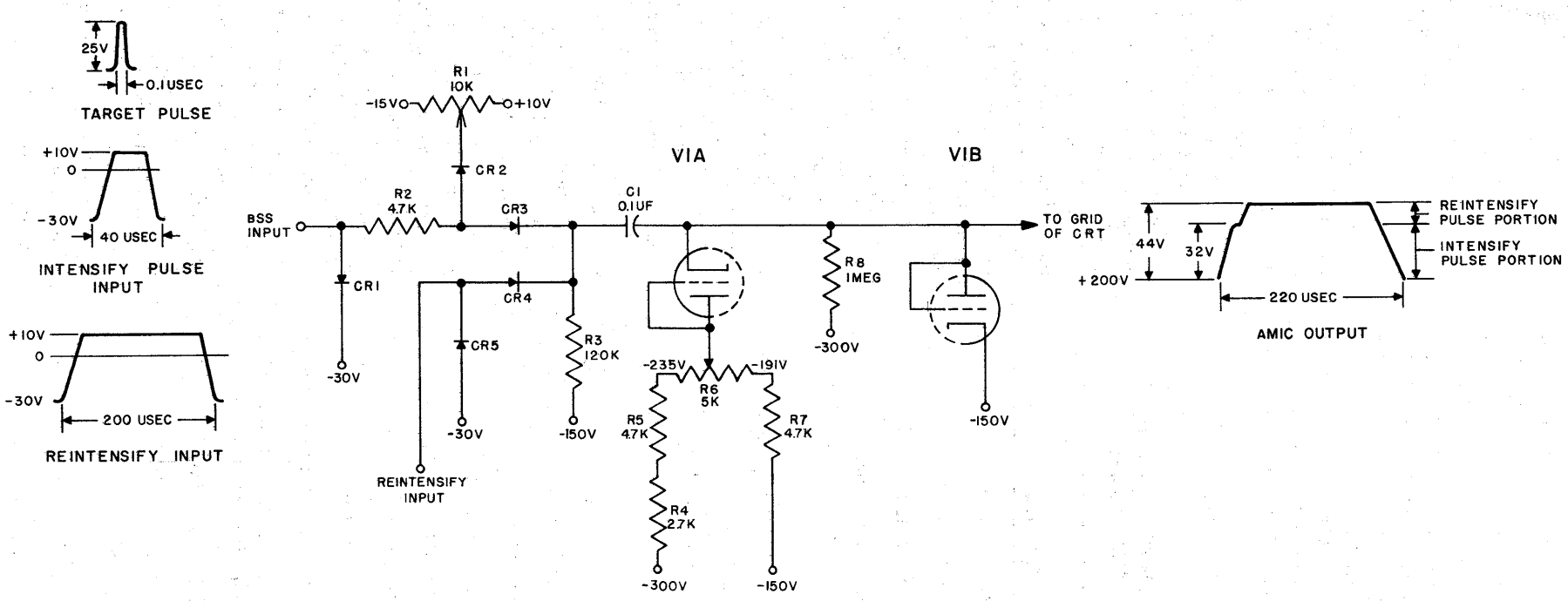


Figure 3–119. Mapper Intensificatior Circuit, Model A, Schematic Diagram

The generation of a sawtooth wave is caused by the charge and discharge of capacitor C2. When no signal is applied to the grid of V1, the tube is cut off because of the effective grid bias of —14V to —19.5V depending on the setting of R5. Meanwhile, C2 charges through R6, R7, and the resistor network in the cathode of V1. The capacitor charge, however, is limited to +10V because V2B is clamped through CR1 to +10V. (The grid circuit of V2B acts as another diode in series with CR1.) Since the screen grid of yoke driver V4 is also connected to the +10V clamp and the control grid is connected to a point of approximately —150V potential, the yoke driver tube normally operates at approximately zero grid bias and conducts heavily. Maximum current in the tube is controlled by adjustment of R22, so that without an azimuth signal applied, the electron beam is deflected just beyond the edge of the CRT screen.

TABLE 3—61. MAPPER SWEEP GENERATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Grid-limiting resistor for V1
R2	Grid return for V1
R3, R4, R5	V1 bias-developing network
R6	Sweep slope potentiometer in V1 plate load circuit (with R7, R8, L1)
R7	Part of V1 plate load (with R6, R8, L1)
R8	Part of V1 plate load (with R6, R7, L1)
R9	V1 screen grid return
R10, R11	Determines lower limit of C2 discharge (with V2A)
R12, R13, R14	Voltage divider network
R15	V3A grid return resistor
R16	V3A, V3B grid bias resistor
R17	V3 cathode resistor
R18	V4 plate load resistor
R19, R20, R21	Bleeder network in V4 plate circuit
R22, R23	Cathode resistors for V4, with R22 as current adjust potentiometer
C1	Input coupling capacitor
C2	V1 output wave shaper
C3	Bypass capacitor
CR1	Clamps C2 charge at +10V through V2B

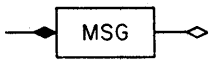


Figure 3—120. Mapper Sweep Generator, Logic Block Symbol

The application of an azimuth pulse to the grid of V1 fires this thyratron and causes a quick discharge of C2 through the parallel network of R8 and L1, and tube V1 itself. Discharge of the capacitor is limited to the voltage value present at the plate of diode V2A. The associated voltage drop is applied to the grid of cathode follower V2B. This tube is thereby driven to near cutoff, and its output is directly coupled to the screen grid and the control grid of yoke driver V4, which is also driven near cutoff. This rapid decay of V4 plate current causes the yoke to "fly back" the beam to the center of the CRT.

Thyratron V1 stops conducting after the discharge of C2. This is due to the negative-going voltage from the discharge of the capacitor and is ensured by the action of inductance L1, which provides a "kick" at the plate to bring the thyratron plate voltage to its cutoff level. At that time, C2 begins to charge through R6, R7, and cathode resistors R10 and R11. Because of the small value of R3, R4, and R5, the effect of this total resistance upon the charging time constant is negligible; this constant, therefore, is mainly established by C2 and the total resistance of R6 and R7. The rate of charge of C2 can thus be controlled with the adjustment of R6.

Although the trailing edge of the sawtooth wave at the input of cathode follower V2B represents the exponential charge of C2, only the most linear position of the exponential is utilized because of the +10V clamp, which limits the rise to approximately 25 percent of the total charging voltage. This linear rise appears at the output of V2B and controls the gradually increased conductivity in yoke driver V4, which causes the yoke to deflect the beam to the edge of the CRT.

Feedback amplifier V3 (two triode sections parallel-connected) is employed to sense variations in the —150V and —300V sources and to provide a signal which compensates for these variations. By means of the feedback amplifier, the cathode and grid voltages of yoke driver V4 are not affected by transients and allowable ripple in the sources mentioned. As an explanation, assume that the —150V source momentarily drops 2V. The effect on yoke driver V4 is to make the cathode more negative, with the result that the grid becomes more positive with respect to the cathode, thus decreasing the effective grid

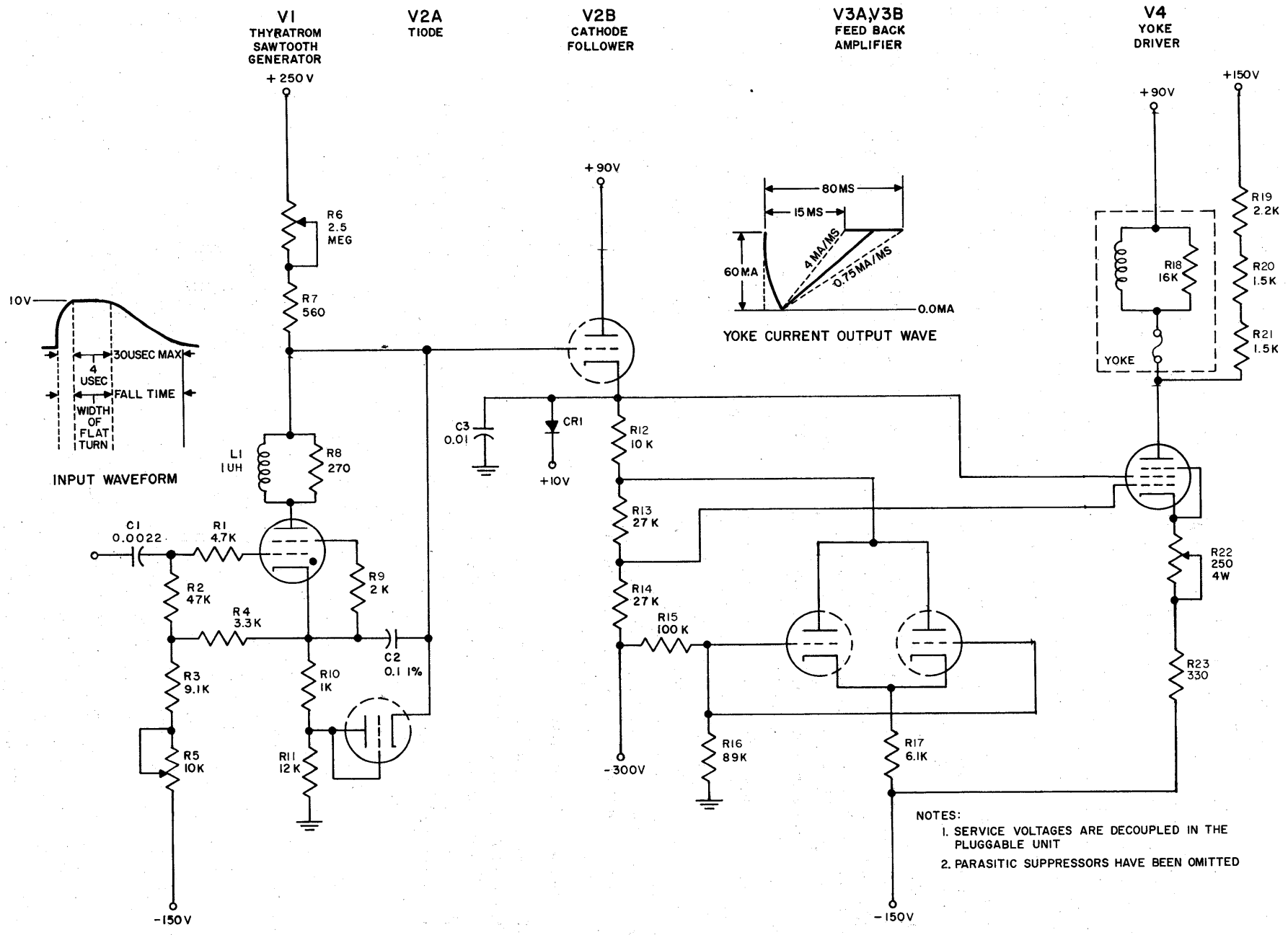


Figure 3–121. Mapper Sweep Generator, Schematic Diagram

bias of the tube. At the same time, the cathodes of feedback amplifier V3, also being connected to the —150V source, will increase conductivity in this tube, which will cause its plate voltage to drop. As a result, the voltage at the junctions of R12-R13 and R13-R14 also decreases. The grid of yoke driver V4, being connected to the latter junction, will decrease in voltage accordingly. By having the proper gain in V3, a voltage decrease at the grid of V4 will be made to correspond with a voltage decrease at the cathode, which will preserve the effective grid bias in spite of variations in the —150V line.

Voltage variations in the —300V source affecting grid voltage at yoke driver V4 are also applied to the grids of feedback amplifier V3.

In this case, the —300V source goes more negative and decreases the conductivity in V3, which raises the voltage at the junction of R12-R13 and R13-R14. Thus, again, by having the proper gain in the feedback amplifier, the voltage decrease in the grid of yoke driver V4 caused by a decrease in source voltage is cancelled out by the action of the feedback amplifier.

A bleeder network in the plate circuit of V4 causes approximately 15 ma of current to flow through the yoke in opposition to the current being supplied by the tube. Allowing the tube to conduct at approximately 15 ma, and then balancing the current through the yoke to zero at flyback in conjunction with the bleeder (+90V at the junction of R21 and R18), serves to keep the tube operating within its linear region at all times.

3.50 MATCHING AMPLIFIER, MODEL A

3.50.1 Definition and Description

The model A matching amplifier (AMA) is a non-logic circuit which performs the function of impedance matching. There are two types of MA's. Type 1 is used to match the impedance of the all-channel driver (par. 3.1) to a 600-ohm line, and type 2 matches the logic gate circuits (par. 3.47) to a 600-ohm line. Both MA circuits are identical except that type 1 uses a coupling capacitor in its input, and, in type 2, the capacitor is replaced by a jumper. The logic block symbol for the MA is shown in figure 3–122.

3.50.2 Principles of Operation

Figure 3–123 is the schematic diagram for the matching amplifier. Table 3–62 lists associated detail parts and their functions. The AMA is a cathode follower type circuit which has a 5:1 stepdown transformer in the cathode circuit. As in all cathode follower circuits, there is no phase shift between the input and output signal. A sinusoidal current through the tube, caused by a sinu-

TABLE 3–62. MATCHING AMPLIFIER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1
R2	Bias resistor to assure linear operation of V1
C1	Coupling capacitor for type 1 input
C2	Bypass capacitor for R2
T1	Stepdown transformer serving as cathode follower load

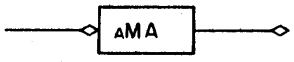


Figure 3–122. Matching Amplifier, Model A, Logic Block Symbol

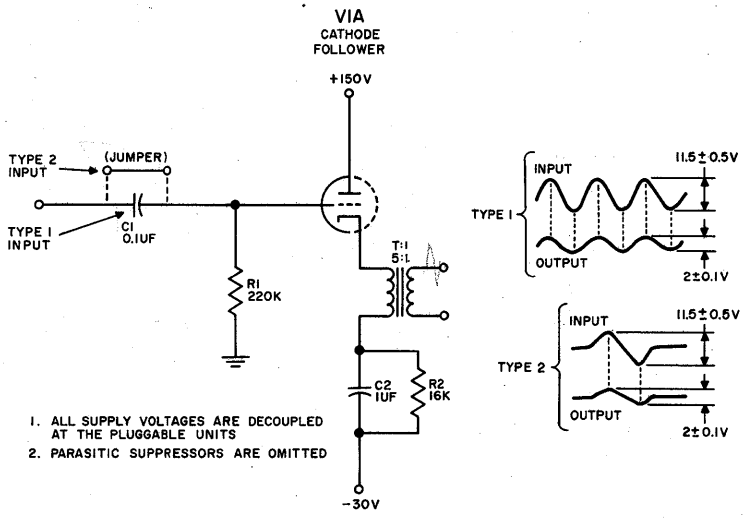


Figure 3–123. Matching Amplifier, Model A, Schematic Diagram

soidal voltage input, produces a sinusoidal voltage at the output terminals of transformer T1. The output of this circuit for an input signal of 11.5V (peak-to-peak) is approximately 2V.

The input signal to the AMA, type 1, is a 1,300-cps sine wave, 11.5 ± 0.5V peak-to-peak and the output, when terminated with 600 ohms, is a continuous 1,300 sine wave, 2V peak-to-peak. Type 2 has input and output signals of the same frequency and magnitude but instead of being continuous they are gated.

3.51 MATRIX OUTPUT AMPLIFIER

3.51.1 Definition and Description

The matrix output amplifier (MOA) is a logic d-c amplifying circuit which provides signal inversion and a shift in output signal level to either partially condition or decondition a core memory driver. There are 128 MOA circuits used in each core memory element in the Central Computer. The logic block symbol for the MOA is shown in figure 3–124.

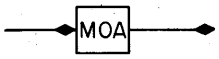


Figure 3–124. Matrix Output Amplifier, Logic Block Symbol

3.51.2 Principles of Operation

Figure 3–125 is the schematic diagram of the MOA. Table 3–63 lists associated detail parts and their functions. The circuit consists of a d-c amplifier (V1), a cathode follower (V2), and associated circuits.

TABLE 3–63. MATRIX OUTPUT AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Voltage divider network
R3	Part of plate load (with L1)
R4	Damping resistor
R5	V2 cathode load
C1	Input compensating capacitor
L1	Choke serving as peaking coil in V1 plate load
CR1	Crystal diode prevents V2 grid from becoming more than 1V positive with respect to cathode.

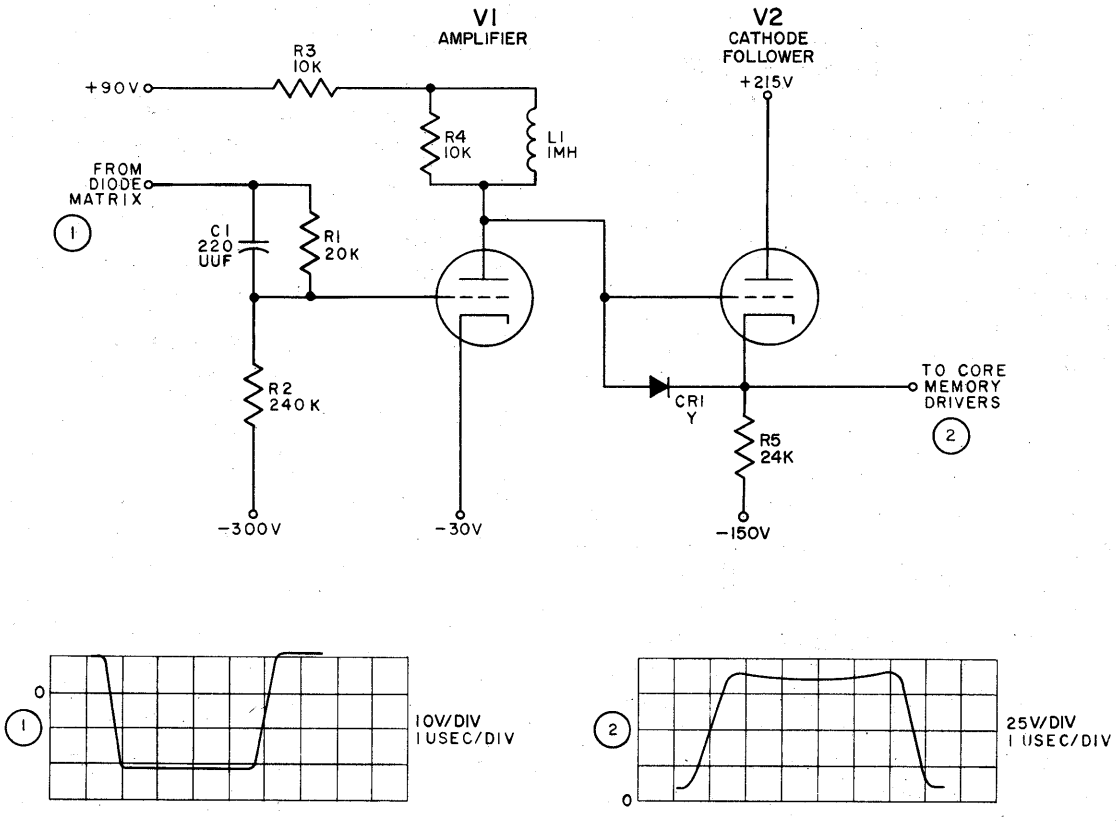


Figure 3–125. Matrix Output Amplifier, Schematic Diagram

The input signal is applied to the voltage divider network consisting of R1 and R2. When the signal is at +10V, the divider network functions to lower the signal level applied to the grid of V1. Because of a high positive grid bias on V1, grid current flows in this tube, causing it to conduct heavily and resulting in the plate voltage dropping from +90V to approximately +10V.

When the input signal is a −30V level the grid signal applied to V1 is −50V. Consequently no plate current flows in this tube, making the output rise to approximately +90V.

The operation of V2 is that of a standard cathode follower circuit. (Refer to T.O. 22, *Basic Circuits.*)

3.52 MEMORY GATE GENERATOR

3.52.1 Definition and Description

The memory gate generator (MGG) is a logic vacuum tube AND circuit and power amplifier which controls the read or write generation pulses of a selected one of 32 core memory drivers in the Central Computer. The logic block symbol for the MGG is shown in figure 3–126.

3.52.2 Principles of Operation

3.52.2.1 Basic Operation

Figure 3–127 is the schematic diagram of the MGG. Table 3–64 lists associated detail parts and their functions.

The input signal to the suppressor grids of V1 and V2 is a d-c level of either +10V or −30V. When the suppressor grid is at the −30V level, the tubes are completely cut off, regardless of the signal applied to the control grid. When the suppressor grid is at the +10V level, the tubes are partially conditioned and plate conduction will occur when a positive pulse signal is applied to the control grids. The voltage divider consisting of R1 and R2 keeps the plates of V1 and V2 at +180V when the tube is cut off and at +40V when the tubes are conducting. The output voltage of V1 and V2 is fed to the control grids of V3 and V4.

3.52.2.2 Detailed Operation

With no inputs to tubes V1 and V2, the voltage at both the suppressor grid and the control grid is −30V, insuring that the tube is below cutoff. When partially selected, the suppressor grid is at the +10V level. The input to the control grid of these tubes is a-c coupled through capacitor C1 and the combination of resistors R4, R5, and crystal diodes CR1 and CR2. This input supplies a positive pulse to the grid when a particular memory gate generator is selected; the input levels obtained are between −30V and +10V. When the input signal goes positive from the −30V level to the +10V level, the capacitor cannot change instantaneously and therefore the 40V signal is applied to the control grids of tubes V1 and V2. Because the input signal is positive, crystal diodes CR1 and CR2 do not conduct. Therefore, the effective resistance coupling the input is R4 and R5 in series. Thus for a positive pulse input, the time constant of the coupling network is C1 times R4 plus R5, giving a resultant time constant of approximately 102 μsec. Since the normal input pulse length is 2 to 3 μsec, the time constant is very much larger than the pulse duration and very little charge is built on C1.

When the input signal goes from the +10V level to the −30V level, the signal on the control grids of V1 and V2 falls 40V. However, during the time that the input signal is at +10V, the capacitor picks up some charge, and a small negative overshoot will be obtained as the grid signal falls toward −30V. When this happens, the time constant of the resistor-capacitor coupling will be greatly reduced because the forward resistance of CR1 and CR2 will come into play, since a positive voltage will be applied to the plates of the diodes with respect to the cathodes. The plate voltage of the diodes is stabilized at −30V; however, if some negative overshoot exists, the voltage on the cathodes of the diodes will be somewhat greater than −30V in the negative direction, and the diodes will be in a position to conduct. Resistors R4 and R5, which parallel the diodes, are effectively shorted out, and the resultant time constant is slightly greater than 0.1 μsec. The time constant now is a very small percentage of the overall pulse duration and therefore C1 will charge very rapidly, to stabilize the control grid input signal at −30V.

TABLE 3–64. MEMORY GATE GENERATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Voltage divider
R3	V1 and V2 suppressor grid isolation resistor
R4, R5	Equalizing resistors for CR1 and CR2
R6, R7, R8, R9 R10, R11	Resistor network which determines value of cathode resistance; with R7 as potentiometer which provides for adjustment of cathode resistance to vary current flowing through selected CMD
C1	Input coupling capacitor
CR1, CR2	Input clamping diodes
S1	Selects portions of resistor network for cathode resistance

The output voltage of V1 and V2, which is normally at the +180V level, is supplied to the control grids of cathode followers V3 and V4 which are connected in parallel. Under these conditions, the cathode current, flowing through the common cathode resistor in the cathode follower circuit, produces an output of approximately +180V, because, since the tube is at maximum conduction, very little cathode bias buildup is present.

When the input to V3 and V4 falls to the +40V level, the cathodes tend to follow that fall. However, since the memory gate generator is used to supply current to one of 32 core memory drivers, and the input to the selected CMD is at approximately a +90V level, the cathode of the MGG is caught at a level in the vicinity of +90V. As the MGG output falls, the core memory driver comes into construction, a current pulse is generated in the core memory driver, and the cathode follower switches plate control from the plates of tubes V3 and V4 to the plate of the core memory driver. Tubes V3 and V4 are cut off, and all current flowing through the cathode resistors of the memory gate generator is under direct control of the selected core memory driver.

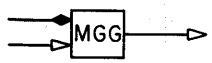


Figure 3–126. Memory Gate Generator, Logic Block Symbol

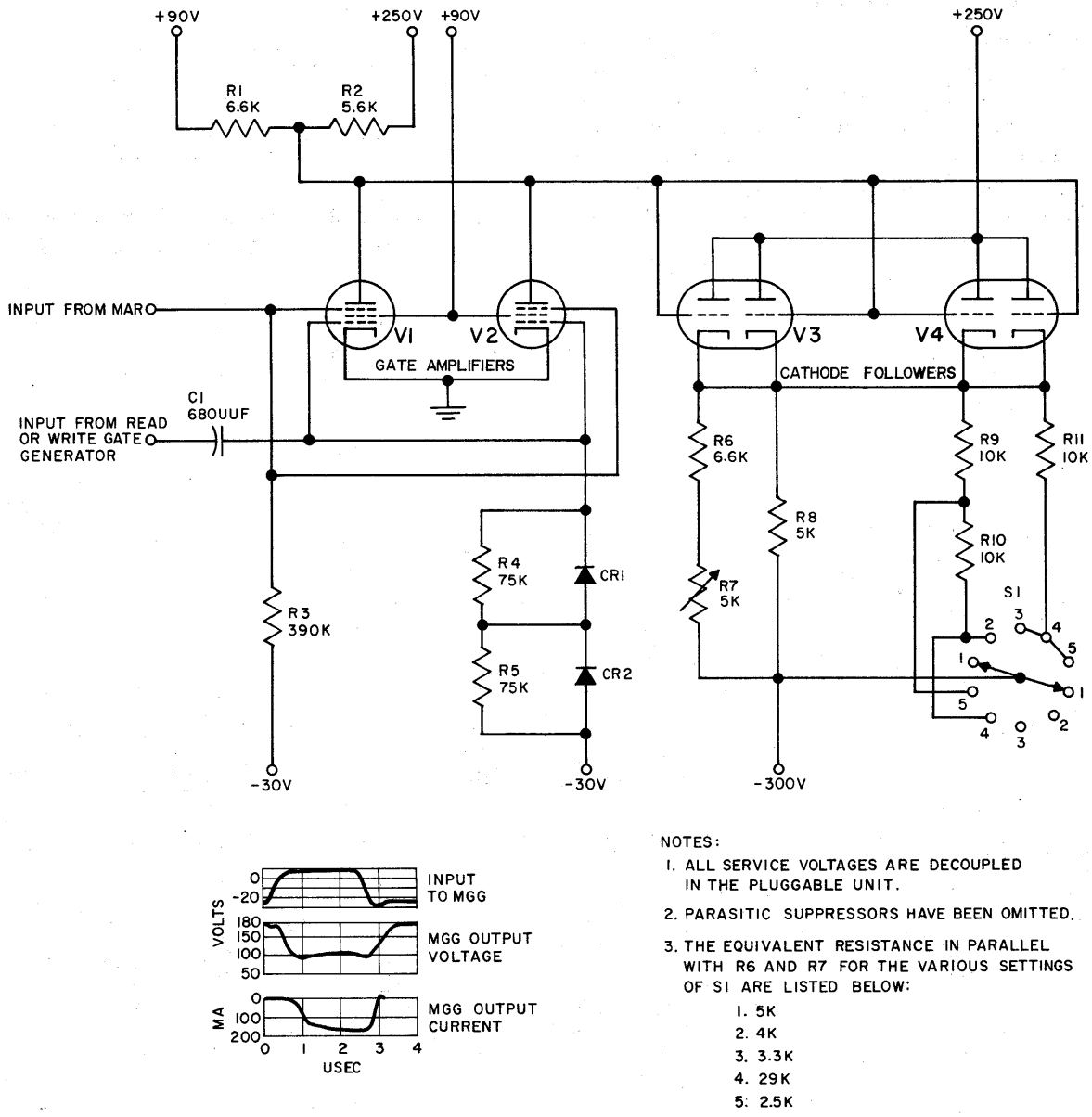


Figure 3–127. Memory Gate Generator, Schematic Diagram

3.53 MESH LEVEL CONTROL AND ERASURE UNIT, MODEL A

3.53.1 Definition and Description

The mesh level control and erasure unit, model A (AMLC), is a nonlogic circuit which provides the following voltages for the DD CRT:

a. Two adjustable levels to the collector and storage meshes to permit stable storage of the display
b. A negative gate to the collector mesh for erasing the display
c. A periodic pulse to the collector and storage meshes to improve contrast during the display.

The logic block symbol for the AMLC is shown in figure 3–128.

3.53.2 Principles of Operation

3.53.2.1 Basic Operation

The schematic diagram of the AMLC is shown in figure 3–129. Table 3–65 lists associated detail parts and their functions. The AMLC breaks down into three circuits: the erasure circuit consisting of a gate generator and a cathode follower, the mesh level control circuit consisting of the level adjustments, and the output circuit which contains the coupling network to the mesh elements.

Triode-connected pentode V1 is held beyond cutoff by a negative standard level during quiescent operation. The output of the erasure circuit (cathode of V2) is applied to the voltage divider containing the collector mesh level potentiometer (R11) and storage mesh level potentiometer (R13). These potentiometers are adjusted to the proper levels for application to the mesh elements. Periodically, as determined by the DD timing cycle, the contrast gate is applied to the mesh elements through the coupling network located in the output circuit; this produces an increase in the ratio of character-to-background brightness.

To produce an erase gate, a ground level is applied to the input of the AMLC. A negative gate output is

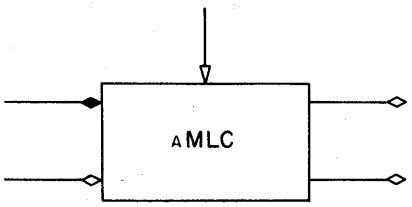


Figure 3–128. Mesh Level Control and Erasure Unit, Model A, Logic Block Symbol

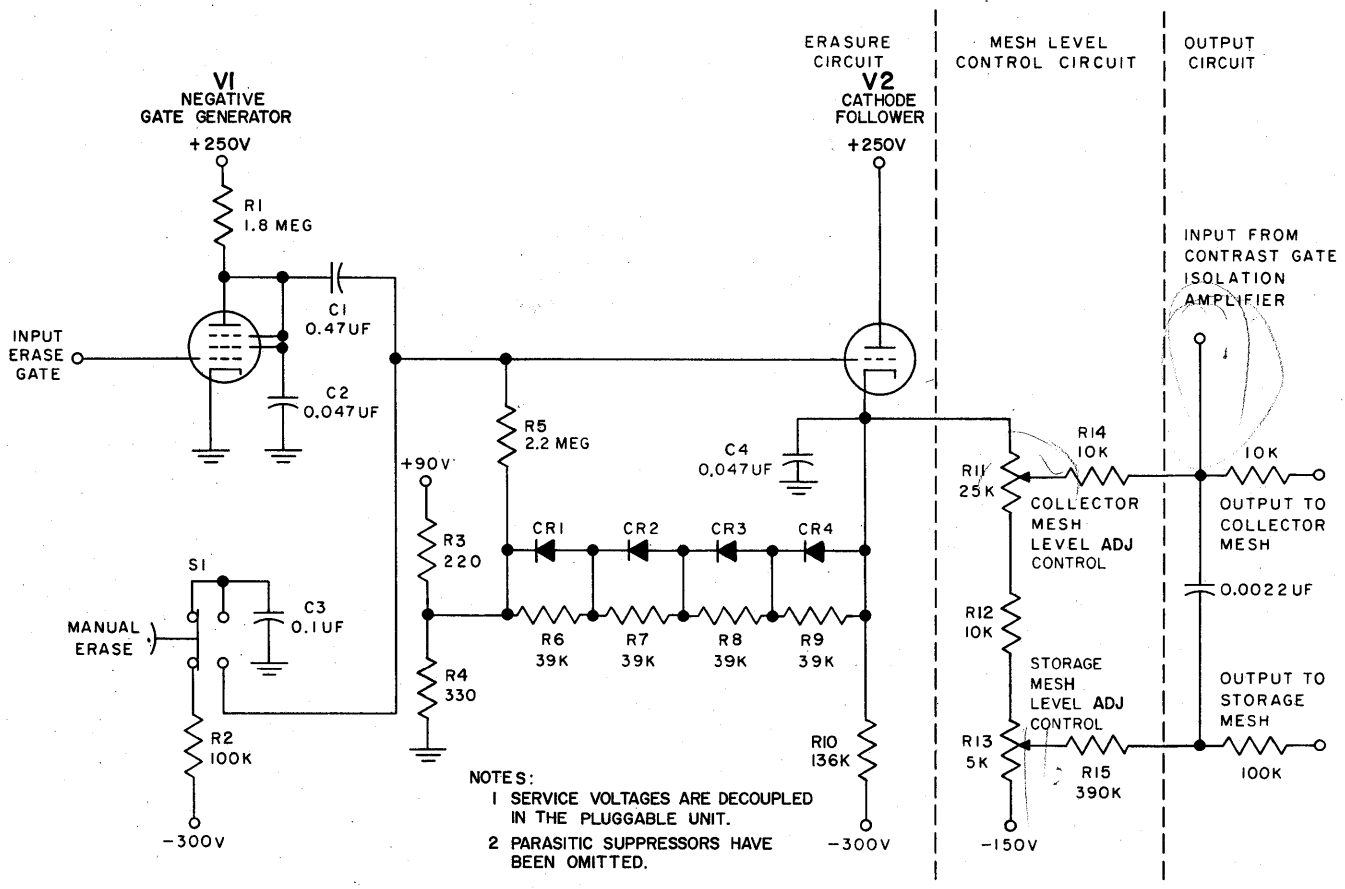


Figure 3–129. Mesh Level Control and Erasure Unit, Model A, Schematic Diagram

generated at the output of V1 and coupled to the grid of V2 by C1. The cathode potential of V2 follows the gate applied to the grid. The negative gate at the cathode of V2, when applied to the voltage divider which contains R11, decreases the potential at the collector mesh, and as a result, erases the display. Erasure occurs during this negative gate time. A negligible portion of the gate is superimposed on the d-c level of the storage mesh.

3.53.2.2 Detailed Operation

During quiescent operation of the AMLC, V1 is held below cutoff by a −30V level at the input. With V1 cutoff, C2 is charged to the plate supply voltage of V1. Because the voltage divider consists of R3 and R4, the grid potential of cathode follower V2 is +50V. The cathode follower conducts heavily, bringing the cathode of V2 to +50V. The cathode is clamped at +50V by the action of the four crystal diodes (CR1, CR2, CR3, and CR4) in series which return the cathode to the voltage divider (R4 and R5).

The voltage divider which includes the collector mesh level control and storage mesh level control is connected between the cathode (+50V) of V2 and −150V. The potential applied to the collector mesh is varied between +50V and −70V as a function of the setting of potentiometer R11. A voltage between −130V and −150V, determined by R13 adjustment, is applied to the storage mesh.

When the contrast gate is applied, the potential on the mesh elements is increased, resulting in a greater contrast between the display characters and background.

When the 2,400-μsec erase gate is applied to the AMLC, V1 conducts, permitting C2, which was charged to +250V, to discharge rapidly through the low resistance of V1. When V1 is again cutoff (end of 2,400-μsec), C2 once again charges to +250V through R1. The charge time is much longer than the discharge time due to the greater resistance in the charge path. The negative gate developed across C2 is coupled through C1, to the grid of V2. The cathode potential of V2 follows the gate applied to the grid, falling to −145V. This negative gate decreases the potential at the collector mesh, interrupting the flow of flood gun electrons through the storage mesh, and hence blanking the face of the DD CRT.

The display can be erased manually by depressing the MANUAL ERASE pushbutton switch S1. This operation connects the grid of V2 to capacitor C3. C3, which was charged to −300V, develops a negative potential on the grid of V2. This in turn causes the cathode potential of V2 to decrease, resulting in the erasure of DD CRT.

TABLE 3–65. MESH LEVEL CONTROL AND ERASURE UNIT, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Coupling capacitor
C2	Part of negative gate generator (with V1 and R1)
C3	Provides negative gate for manual erase (with R2)
C4	Increases fall time of negative gate at cathode of V2
CR1-CR4	Clamps V2 cathode at +50V
R1	Plate load resistor for V1 and part of negative gate generator (with V1 and C2)
R2	Charging resistor for C3
R3, R4	Voltage divider
R5	Grid return resistor for V2
R6-R9	Equalizing resistors for CR1-CR4, respectively
R10	Cathode load resistor for V2
R11, R12, R13	Voltage divider with R11 as collector mesh level control and R13 as storage mesh level control
R14	Protects collector mesh against current surges
R15	Protects storage mesh against current surges

3.54 MILLER INTEGRATORS, MODELS A AND B

3.54.1 Definition and Description

The Miller integrator (MI) is a logic circuit that generates a triangular wave voltage as a function of input voltage level shifts. There are two models, A and B, of the Miller integrator. See figure 3–130 for the MI logic block symbol.

Both Miller integrators are employed in the Input System. The AMI is the heart of the triangular wave generator circuit group in the azimuth synchronizing circuit of the gap-filler input (GFI) element. The input square wave is amplitude limited by the AGC circuit, paragraph 3.6, to ensure a constant amplitude triangular wave output by the AMI. This triangular wave output is fed to a frequency doubler, paragraph 3.38. The triangular wave is utilized by the azimuth motor drive circuit group to produce the a-c driving power which rotates the yoke in the GFI mapper console.

The BMI is used in the north synchronizer as a timing device. Whenever the yoke north in the mapper console lags radar north by 10 degrees or less, the yoke is double-speeded to bring yoke north into coincidence with radar north. The BMI output is used to control the length of the double-speed interval.

3.54.2 Principles of Operation

3.54.2.1 Miller Integrator, Model A

Figure 3-131 is the schematic diagram of the AMI. Table 3-66 lists the associated detail parts and their functions.

The input signal to the AMI is a square wave with a frequency of 4.25 to 21.25 cps and an amplitude of 5 to 25V. With no signal input, the AMI grid is at −150V and the cathode is returned to −146V by the action of voltage divider R6 and R7. The resultant current causes V1 plate voltage to fall to +150V. Capacitor C2, connected between the plate at +150V and the grid at −150V, charges to 300V. At this point of operation, the quiescent point, +0.7V applied to the grid will drive V1 to maximum conduction, 1.5 ma, and −0.7V applied to the grid will drive V1 to cutoff. Thus, with the input signal specified above, V1 is alternately driven into maximum conduction and no conduction.

Assume that input voltage shifts from −30V to +10V. The voltage at the junction of R1 and C1 will follow and be clamped at the level applied to the cathode of CR2 by the AGC circuit. This voltage rise applied to the grid of V1 causes grid current to flow through R2, limiting the rise at the grid. The limited rise at the grid is amplified and inverted at the plate of V1. However, C2 cannot instantaneously discharge to accommodate this reduction in voltage across it. Therefore, the grid voltage rises and the plate voltage falls at a rate determined by the discharge of C2. Grid voltage rise, approximately 1V, is a small fraction of plate voltage fall, approximately 30V and the overall effect is one of linear plate voltage fall. The discharge path is through V1, C2, R2, and R3.

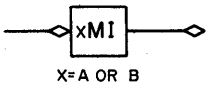


Figure 3–130. Miller Integrator, Models A and B, Logic Block Symbol

TABLE 3–66. MILLER INTEGRATOR, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Coupling capacitor
C2	Integrating capacitor
C3	Output coupling capacitor
CR1, CR2	Clamping diodes
R1	Diode current limiting
R2	Grid limiting and integrating circuit resistor
R3	Grid return
R4	Plate load
R5	Screen grid return
R6, R7	Voltage divider

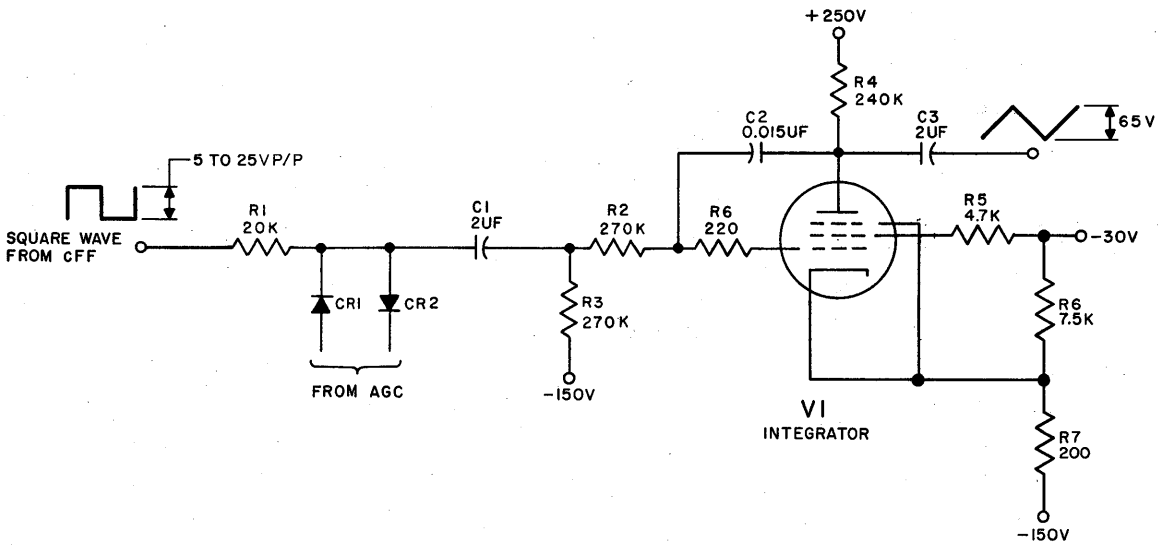


Figure 3–131. Miller Integrator, Model A, Schematic Diagram

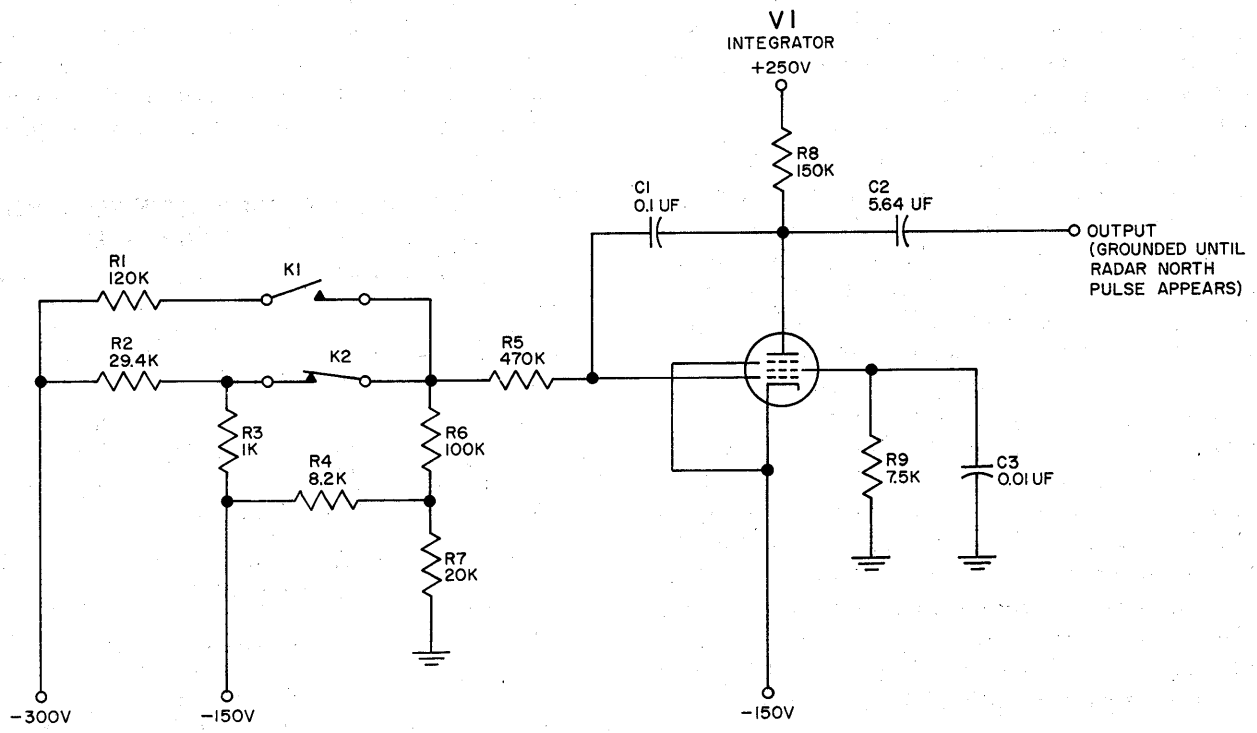
When the input voltage shifts from +10V to −30V, diode CR1 clamps the negative level at the value developed by the AGC circuit. This negative shift would cut V1 off. Without C2 in the circuit, V1 plate voltage would rise to +250V. However, plate voltage change is determined by C2. The charging path is R4, C2, R2, and R3.

The charging and discharging currents are constant. Therefore the fall of output voltage will take as long as the rise of output voltage producing a triangular wave (see waveform 2, fig. 3–131). It must be remembered that C2 never charges or discharges completely to the values of voltage being developed across it. The input voltage continually interrupts the action. For this reason the Miller integrator output tends to decrease in amplitude as input frequency increases. The level supplied by the AGC circuit neutralizes this tendency by limiting the lowest frequency signal amplitude to 5V and the highest frequency signal amplitude to 25V.

3.54.2.2 Miller Integrator, Model B

Figure 3-132 is the schematic diagram for BMI. Table 3–67 lists associated detail parts and their functions. The input circuit of the BMI consists of resistors and relays. The states of the relays determine the resistor configuration which in turn sets the d-c level applied to the grid. The table in the schematic lists the d-c voltage levels applied to the grid of V1 under the three relative positions of yoke north and radar north. The corresponding states of the contacts of relays K1 and K2 are also listed.

As with model A, an output is generated by the BMI when V1 is successively driven to maximum conduction and no conduction. This sequence occurs whenever the yoke north lags radar north by 10 degrees or less. When radar reaches north, relay K2 opens and the ground on the output line is removed. Relay K1, normally open, remains open and the grid of V1 is raised to −110V by voltage divider R4 and R7. Tube V1 is immediately



INPUT	YOKE	RADAR	*K1	*K2
−190V	NORTH	NORTH	CLOSED	OPEN
−157V	NORTH	APPROACHING NORTH	CLOSED	CLOSED
−110V	APPROACHING NORTH	NORTH	OPEN	OPEN

*RELAY K1 CONTACTS NORMALLY OPEN, CLOSE WHEN YOKE REACHES NORTH.

**RELAY K2 CONTACTS NORMALLY CLOSED, OPEN WHEN RADAR REACHES NORTH.

Figure 3–132. Miller Integrator, Model B, Schematic Diagram

TABLE 3–67. MILLER INTEGRATOR, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Integrating capacitor
C2	Output coupling capacitor
C3	Screen bypass
K1, K2	Bias-controlling relay contacts
R1-R4	Voltage divider
R5	Grid limiting
R6, R7	Voltage divider, grid return
R8	Plate load
R9	Screen load

driven into conduction. As with AMI, the plate voltage falls at the rate of discharge of integrating capacitor C1. The discharge path is R6, R5, and V1. What would have been a sharp fall in voltage becomes a linear fall which is coupled to the next circuit by C2. When the yoke reaches north, relay K1 contacts close and grid voltage falls to —190V. Once again, because of C1, V1 plate voltage rises linearly at the charging rate of the integrating capacitor. The 40V difference between the grid and cathode appears across R5 and diminishes at a linear rate as C1 charges through R8, R5, and R6.

Thus for the period during which radar has reached north and the yoke is approaching north, the BMI generates a linear fall of voltage. After the yoke has reached north, the BMI generates a rise in voltage which returns the circuit to its quiescent state. The constant charging and discharging currents ensure that the period of rise shall equal the period of fall. Consequently, the triangular wave generated represents a time interval two times the lag of yoke north behind radar north. A double-speed acceleration applied to the yoke in this period will enable the yoke to catch up with the radar.

3.55 MISSING-PULSE DETECTOR, MODEL A

3.55.1 Definition and Description

The model A missing-pulse detector (AMPD) is a logic circuit which is used in the magnetic tape system of the Central Computer. The AMPD provides a constant, positive d-c output as long as standard pulses are applied to it. When the pulses are discontinued or occur at a too low rate of repetition, the output falls to a constant negative d-c level. With proper delay and spacing, the AMPD will indicate the absence of one pulse in an interrupted train of pulses. The logic block symbol for the AMPD is shown in figure 3–133.

3.55.2 Principles of Operation

Figure 3–134 is the schematic diagram of the AMPD. Table 3–68 lists associated detail parts and their functions.

With no signal applied, the AMPD maintains an output d-c level of —30V. This condition results from the cutoff bias which is provided to the grid of V1 by a voltage divider between the —300V and —150V supplies. The plate of V1 tries to rise to +150V, but the grid of V3 draws current and clamps the V1 plate, setting its upper limit at approximately ground potential. Since V3 conducts heavily, its plate voltage drops. This causes the voltage level at the output of the AMPD to fall until clamped to —30V by CR2.

Assume that a single standard pulse is applied to the AMPD. This pulse is coupled to the grid of V1, causing the tube to conduct. Capacitor C2, which is normally at ground potential, shorts any quick variation in voltage and consequently charges very rapidly in a negative direction by passing the full conduction current of V1. When C2 has charged to —30V, V2 begins to conduct and passes all the tube current of V1, except for the small current passed by the V1 plate load and the current necessary to keep C2 charged to —30V for the dura-

TABLE 3–68. MISSING-PULSE DETECTOR, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Voltage divider
R3	Part of timing circuit in V1 plate load (with C2)
R4	Grid-limiting resistor
R5	V3A plate load and part of voltage divider (with R6, R8)
R6	Part of voltage divider (with R5, R8)
R7	V3B plate load resistor
R8	Part of voltage divider (with R5, R6)
R9	V3B cathode output resistor
CR1	Clamping diode for +10V output
CR2	Clamping diode for —30V output
C1	Input coupling capacitor
C2	Part of timing circuit (with R3)
C3	Speedup capacitor
C4	Compensating capacitor
C5	Feedback coupling capacitor

tion of the pulse. When the voltage across C2 falls from ground to —30V, V3A cuts off, its plate voltage rises, and the MPD output level rises until it is clamped at +10V by CR3. V3A remains cut off as long as its grid is more negative than —6V. Since the fall time at V3 is very short, the positive feedback has very little effect in improving the speed of the circuit.

As the input pulse dies, V1 cuts off and C2 begins to charge from —30V toward +150V through R3. When C2 has charged to —6V, V3A begins to conduct. During the first instant of conduction, the plate voltage of V3A is lowered slightly, causing the plate voltage of V3B to rise slightly. This slight rise at V3B plate is coupled to the grid of V3A. Thus, the first instant of conduction in V3A is the trigger that starts the regenerative feedback action. V3A is quickly brought into full conduction and the output falls, returning the circuit to its steady-state condition. C2 offers no opposition to the feedback action. The feedback circuit improves the fall time by a factor of 7.

Now assume that a steady train of standard pulses is applied to the AMPD input. If the time between pulses is less than the delay time as set by the values of R3 and C2, the output will be a steady +10Vdc level since C2 must begin to charge from —30V toward +150V after each pulse. If the pulses occur at such a rate that the time between them is greater than the delay time of the AMPD, the circuit will be allowed to return to its stable state after each pulse.

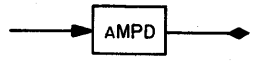
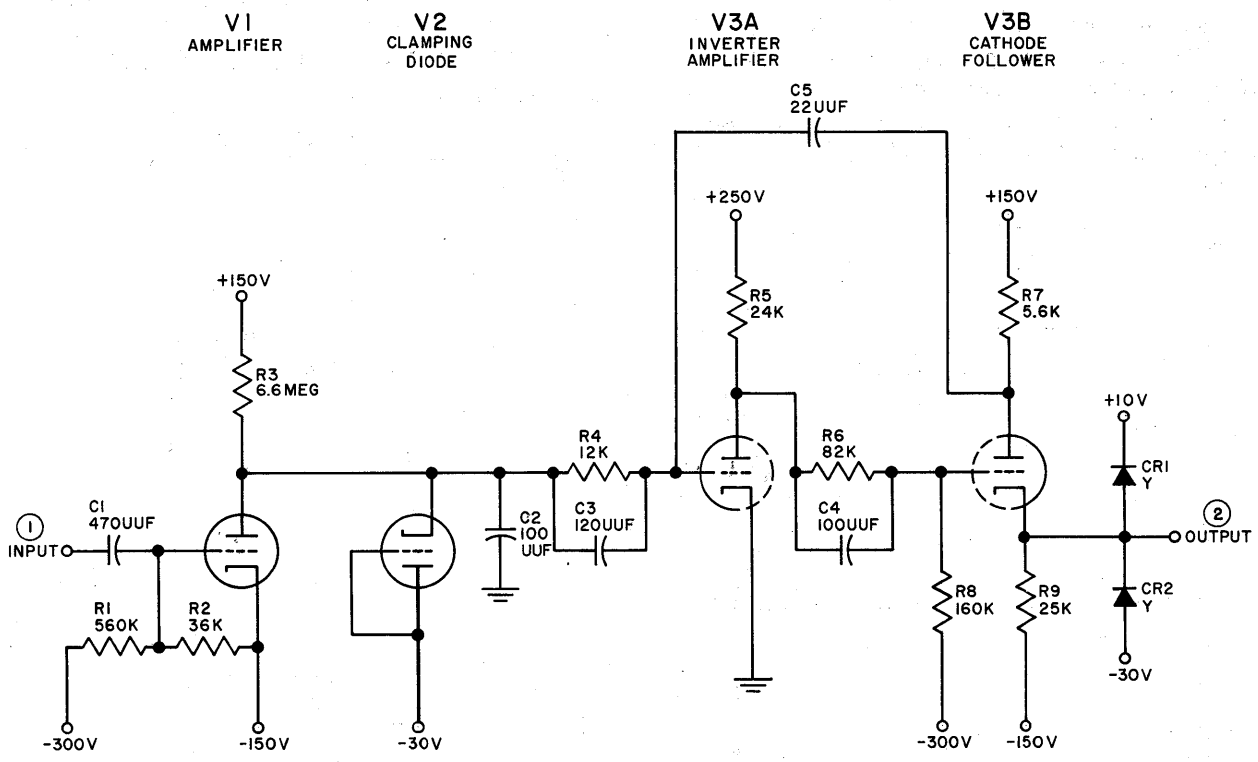


Figure 3—133. Missing Pulse Detector, Model A, Logic Block Symbol



NOTES:
1. ALL SUPPLY VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

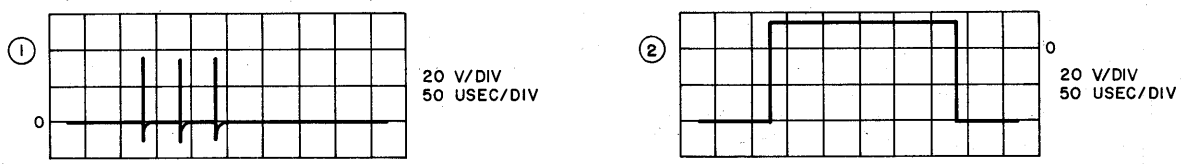


Figure 3—134. Missing Pulse Detector, Model A, Schematic Diagram

3.56 MULTIPLIER

3.56.1 Definition and Description

The multiplier (MUL) is a logic circuit which produces an output voltage proportional to the product of two input voltages. The logic block symbol for this circuit is shown in figure 3–135.

In Input System logic, two multipliers are used in the analog section of the LRI monitor control unit. One produces an output proportional to the product of the range and sine of the target azimuth. The other produces an output proportional to the product of range and cosine of the azimuth.

3.56.2 Principles of Operation

3.56.2.1 Basic Operation

Figure 3–136 is the block diagram of the multiplier. The method of multiplication is illustrated in table 3–69, where e_1 and e_2 are the analog signal inputs. Input stages alter these inputs by a factor K so that the output is Ke_1 or Ke_2, as the case may be. The operational amplifier next in the signal path receives e_1 and a portion of Ke_1 (or e_2 and a portion of Ke_2) to produce a difference output which is $(k-1)e_1$ or $(k-1)e_2$.

Thus,

$$B_1 = (K-1)e_1$$

$$B_2 = Ke_1$$

$$B_3 = Ke_2$$

$$B_4 = (K-1)e_2$$

A 2-mc triangular wave (S) from the oscillator and waveshaper is added to B_1 and B_2 to produce $\frac{E}{2} + (K-1)e_1$, and $\frac{E}{2}$ is the average value of S. These two signal voltages are designated $B_{1'}$ and $B_{2'}$, respectively.

Four new signal voltages are generated in the diode network by taking the average values of $B_{1'} - B_3$ (for C_1), $B_{2'} - B_3$ (for C_2), $B_{2'} - B_4$ (for C_3), and $B_1 - B_4$ (for C_4). Two more signals are generated by dividing A (a known factor) into the sums of C_1 and C_3 (for D_1) and C_2 and C_4 (for D_2). Finally, two more operational amplifiers are utilized to produce an output which is D_1 minus D_2 divided by a second known factor B. Factors A and B are circuit constants determined by resistance values which keep the output voltage within reasonable limits.

The manner in which the proportional product is computed is illustrated by the numerical development of two cases in table 3–69. Note that the multiplier scale factor (Sf) is equal to 100 times AB. Thus,

$$\frac{e_1 e_2}{Sf} = \frac{(C_1 + C_3) - (C_2 + C_4)}{AB}$$

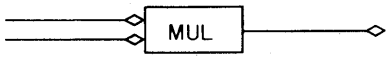


Figure 3–135. Multiplier, Logic Block Symbol

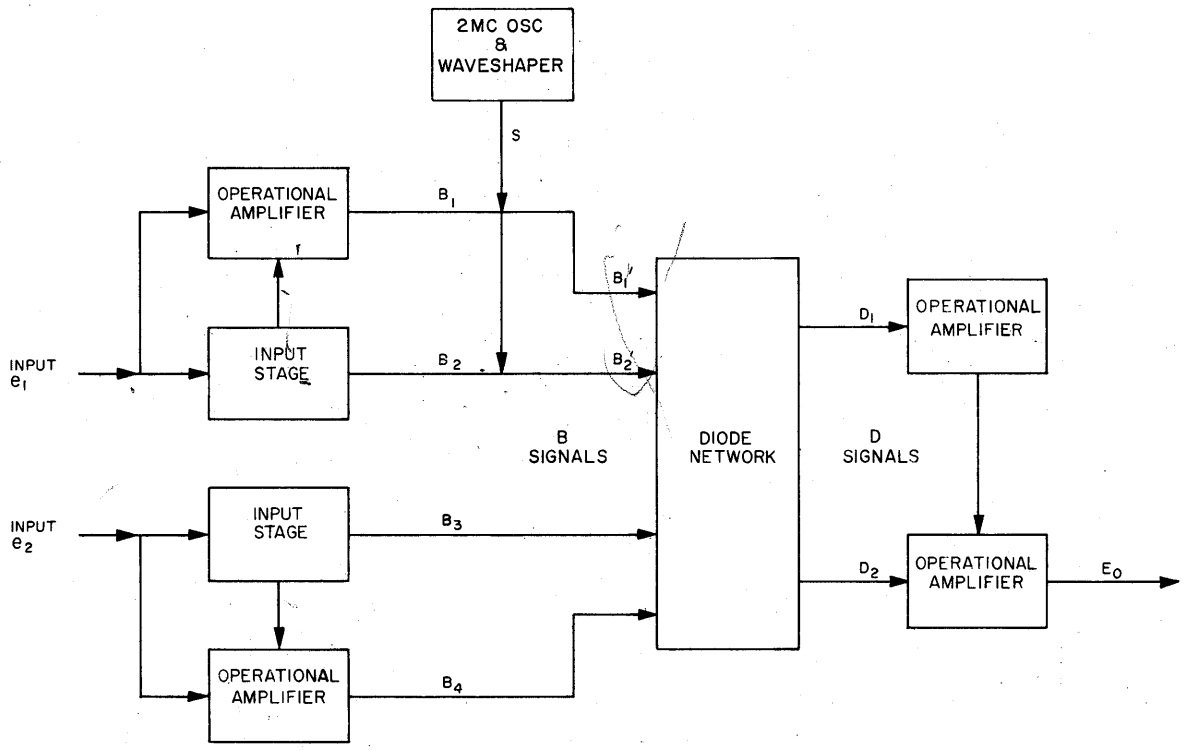


Figure 3–136. Multiplier, Block Diagram

TABLE 3-69. NUMERICAL EXAMPLE OF MULTIPLIER FUNCTION

Circuit Constants: K (*gain of cathode follower*) $= 0.6$

E (*amplitude of 2-mc wave*) $= 100V$ *peak-to-peak*

Sf (*scale factor*) $= 25$

AB (*calibrated resistance factor*) $= 0.25$

CASE 1	CASE 2
Input: $e_1 = 5V$	Input: $e_1 = 20V$
$e_2 = 10V$	$e_2 = 5V$
Output: $\frac{e_1 e_2}{25} = E_o$	Output: $\frac{e_1 e_2}{25} = E_o$
Derivation:	Derivation:
$B_{1'} = S + B$	$B_{1'} = 42V$
$= \frac{E}{2} + (K-1)e_1$	
$= \frac{100}{2}(-2) = 48V$	
$B_{2'} = S + Ke_1$	$B_{2'} = 62V$
$= \frac{100}{2} + 3 = 53V$	
$B_3 = Ke_2 = 6V$	$B_3 = 3V$
$B_4 = (K-1)e_2 = -4V$	$B_4 = -2V$
$C_1 = \frac{E}{2}\left(\frac{B_{1'} - B_2}{E}\right)^2$	$C_1 = 7{,}605V$
$= \frac{100}{2}\frac{42}{100}^2 = 8{,}820V$	
$C_2 = \frac{E}{2}\left(\frac{B_{2'} - B_3}{E}\right)^2 = 11{,}045V$	$C_2 = 17{,}405V$
$C_3 = \frac{E}{2}\left(\frac{B_{2'} - B_4}{E}\right)^2 = 16{,}245V$	$C_3 = 20{,}480V$
$C_4 = \frac{E}{2}\left(\frac{B_{1'} - B_4}{E}\right)^2 = 13{,}520V$	$C_4 = 9{,}680V$
$D_1 = \frac{C_1 + C_2}{A} = \frac{25.065}{A}$ *volts*	$D_1 = \frac{28.085}{A}$ *volts*
$D_2 = \frac{C_2 + C_4}{A} = \frac{24.565}{A}$ *volts*	$D_2 = \frac{27.085}{A}$ *volts*
$E_o = \frac{D_1 - D_2}{B} = \frac{0.5}{AB}$ *volts*	$E_o = \frac{1}{AB}$ *volts*
$E_o = 2V$	$E_o = 4V$

3.56.2.2 Detailed Operation

Figure 3–137 is the schematic diagram of the input stage, and figure 3–138 is the schematic diagram of the operational amplifier portion of the multiplier. Table 3–70 lists associated detail parts and their functions.

The input stage is a cathode follower and voltage divider network. Input signal e_1 or e_2 is applied to the grid of V1 through voltage divider R1 and R2; the output is developed across the bleeder network R5, R6, and R7. The output developed is Ke_1 or Ke_2, where K represents the fractional gain of V1 and attenuation due to the voltage divider R1 and R2. When e_1 or e_2 is zero, the output is also zero; calibration for this point is affected by potentiometer R7. A portion of Ke_1 or Ke_2 is applied to one input of the operational amplifier and e_1 or e_2 is applied to the other input through coupling network C1, R4. The first stage of this circuit is a differential amplifier, and the output is a function of the difference between the two inputs. This difference output drives a high-gain pentode amplifier (V2) which drives a cathode follower (V3). The output, $(K-1)e_1$ or $(K-1)e_2$, is taken from the cathode of V3.

The d-c amplifier, V2, uses a large amount of negative feedback from V3 for linearity and stability. Note that the value of resistor R1 in the cathode circuit of V3 differs with the amplifier application to accommodate the different input voltage ranges.

Signals B_1 and B_2 are augmented by the output of the 2-mc oscillator and waveshaper shown in figure 3–139. In this circuit, V1A and associated components constitute the oscillator, and V1B and associated components function as a d-c restorer for the oscillator output. This output serves as a switching signal for the constant current generator, V3, which produces the required 100V peak-to-peak triangular wave.

The four B signals generated from e_1 and e_2 are fed to the multiplier diode network shown in figure 3–140. This circuit averages the differences between pairs of B inputs to produce four C signals, which, in turn, are paired and reduced to the two D signals. Outputs D_1 and D_2 are reduced to a single signal by two more operational amplifiers (see fig. 3–138), arranged as a difference-taking circuit (fig. 3–141). Resistors R1, R3, and R5 function as parasitic suppressors. Resistors R2 and R4 perform the same function as R6 in fig. 3–138. The output is a function of D_1 and D_2 and thus is proportional to the product of e_1 and e_2.

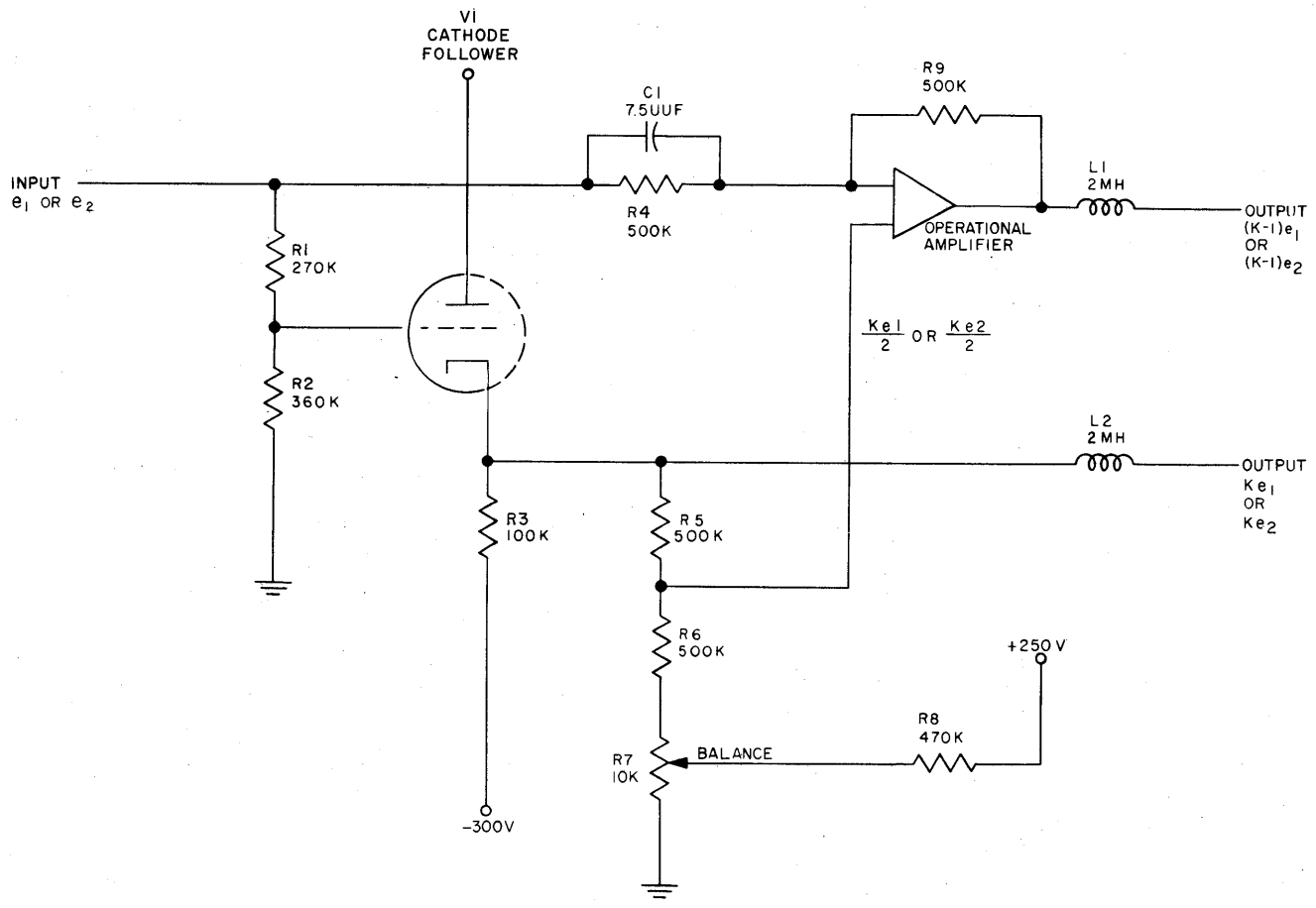


Figure 3–137. Multiplier, Input Voltage Divider Network, Schematic Diagram

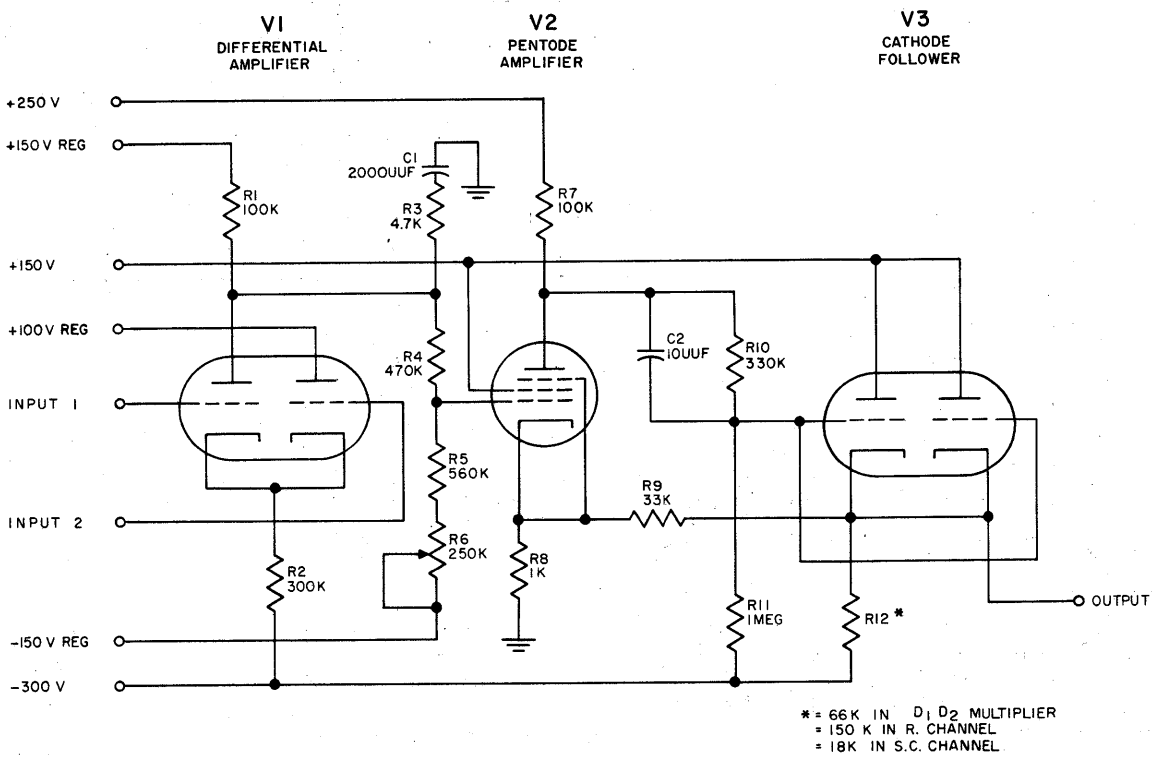


Figure 3–138. Multiplier, Operational Amplifier, Schematic Diagram

TABLE 3–70. MULTIPLIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
	INPUT VOLTAGE DIVIDER NETWORK
R1, R2	Input voltage divider for V1
R3	V1 cathode resistor
R4	Part of input coupling network (with C1) to operational amplifier
R5, R6	Voltage divider (with R7)
R7	Balance control and part of voltage divider (with R5 and R6)
R8	Voltage-dropping resistor
R9	Current-limiting resistor
C1	Part of input coupling network (with R4) to operational amplifier
L1, L2	Peaking coils
	OPERATIONAL AMPLIFIER
R1	V1A plate load
R2	V1 cathode resistor
R3	Part of V2 grid return network (with C1)
R4, R5	Voltage divider (with R6)
R6	Gain control and part of voltage divider (with R4 and R5)
R7	V2 plate load
R8	V2 cathode resistor
R9	Feedback resistor from output to V2
R10	Part of voltage divider (with R7 and R11) and d-c coupling resistor
R11	Part of voltage divider (with R7 and R10)
R12	V3 cathode resistor
C1	Part of V2 grid return network (with R3)
C2	Speedup capacitor
	2-MEGACYCLE OSCILLATOR
R1	Bias resistor for V1A
R2	Part of coupling network (with C3 and C4)
R3	Bias resistor for V2
R4	Part of V2A plate load (with V2B)
C1, C2	Part of tank circuit (with L1)
C3, C4	Part of coupling network (with R2)
L1	Part of tank circuit (with C1 and C2)
CR1	Clamping diode

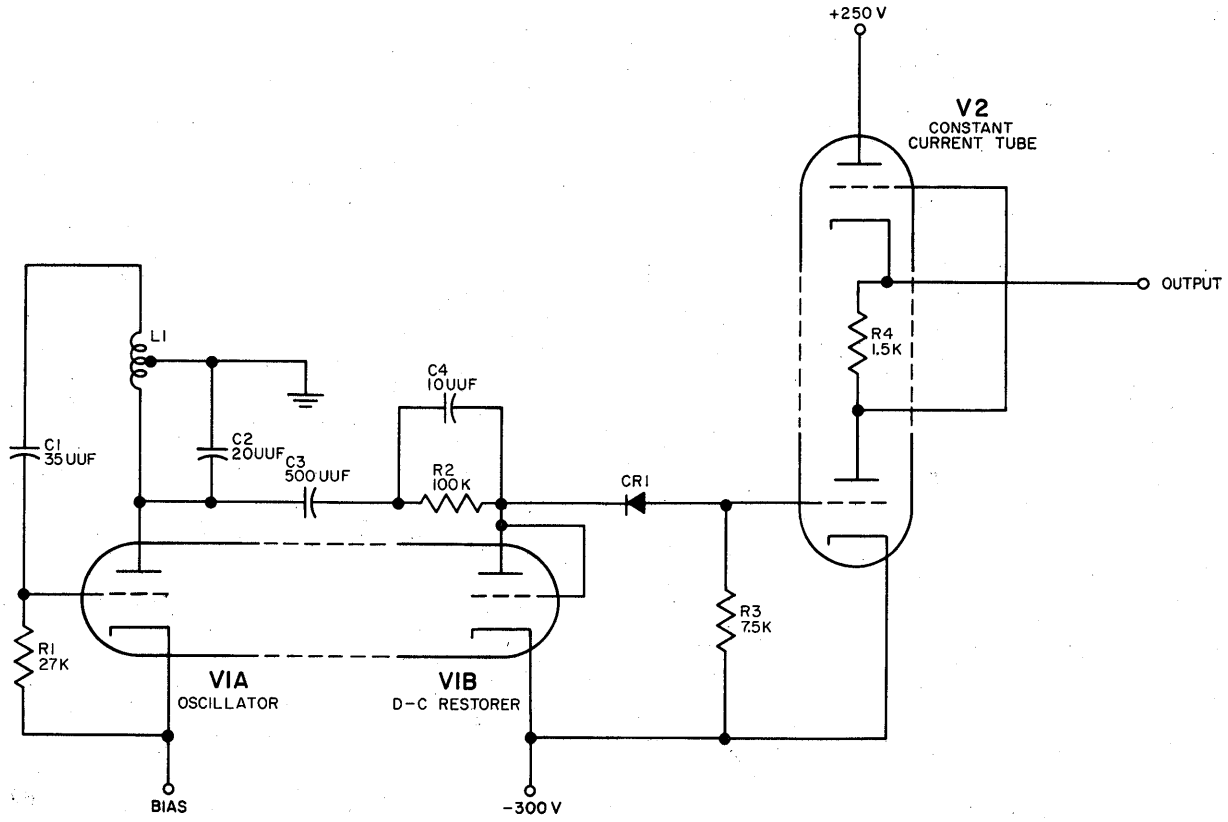


Figure 3–139. Multiplier, 2-Megacycle Oscillator, Schematic Diagram

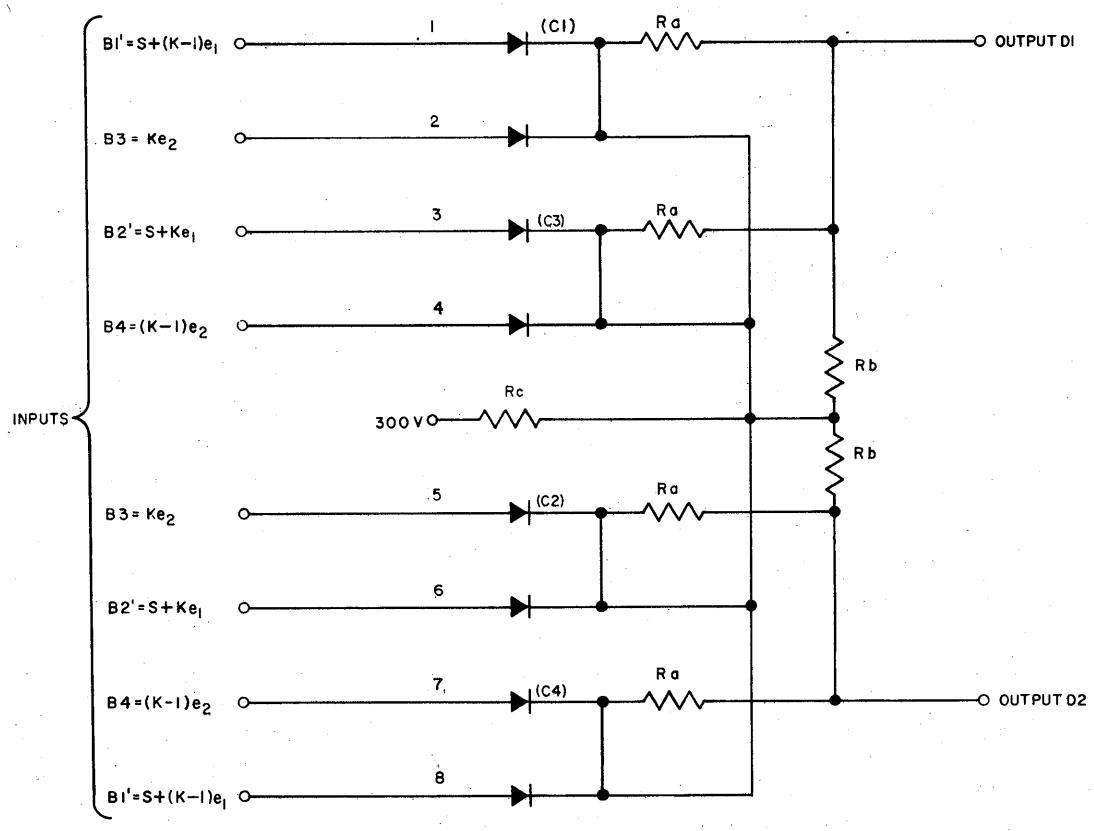


Figure 3–140. Multiplier, Diode Network, Schematic Diagram

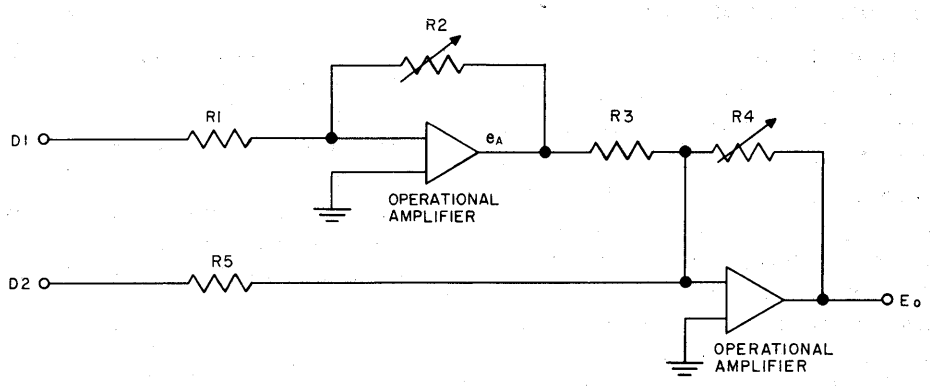


Figure 3–141. Multiplier, Difference Circuit, Schematic Diagram

3.57 NEGATIVE "OR" CIRCUIT

3.57.1 Definition and Description

The negative OR is a logic circuit which furnishes a negative output whenever either of the two input voltages changes in the negative direction.

In Central Computer logic, the negative OR is used in the character register of the tape element. It allows the tape flip-flop to be set either by a pulse read from the tape or by a write echo pulse which appears during the write operation. The circuit will pass only negative pulses and is insensitive to positive pulses.

The logic block symbol for the negative OR circuit is shown in figure 3–142.

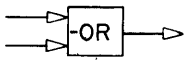


Figure 3–142. Negative OR Circuit, Logic Block Symbol

3.57.2 Principles of Operation

Figure 3–143 is the schematic diagram of the negative OR. The circuit consists of two resistance-capacitance coupling networks connected to a common output through crystal diodes.

The input signal to the negative OR may be applied to either of the two inputs to the circuit. Only one of the inputs is pulsed at any one time. In the no-signal condition, both inputs are at a high positive level. Capacitors C1 and C2 are charged to a potential equal to the applied voltage, and no current flows through load resistors R1 and R2. When one of the inputs is pulsed, the negative-going edge of the pulse is differentiated by the RC network and passed to the output of the diode.

In a similar manner, the positive-going edge of the input pulse results in a positive voltage across the load resistor associated with that input. The crystal diodes prevent the positive halves of the signals across the resistors from appearing at the output.

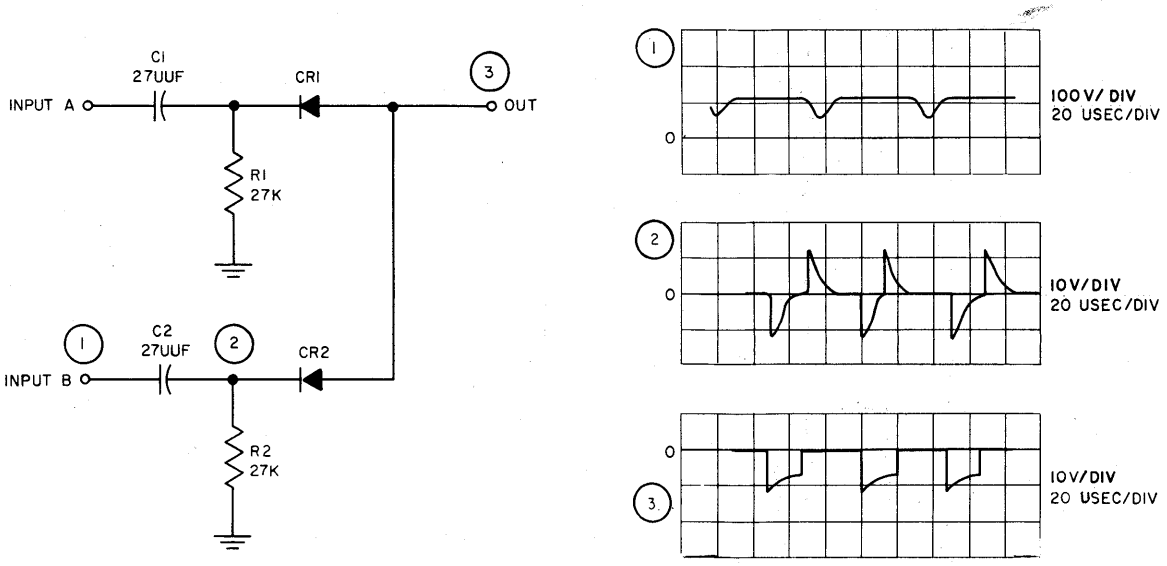


Figure 3–143. Negative OR Circuit, Schematic Diagram

3.58 OPTICAL FREQUENCY GENERATOR

3.58.1 Definition and Description

The optical frequency generator, OFG, produces a 100-kc sine wave timing signal. Figure 3–144 is the logic block symbol for the OFG.

The OFG is used in the Drum System. Physically, the OFG consists of an optical transducer, a photomultiplier, and an output circuit. The optical transducer is the source of a white light with an intensity that varies at a sinusoidal rate. This varying light is converted into an electrical sinusoidal signal by the electronic portion of the OFG. The following discussion covers the operation of the electronic circuit. A detailed discussion of the light source or optical transducer appears in manual 3-42-0, *Theory of Operation, Drum System.*

3.58.2 Principles of Operation

The electronic portion of the OFG consists of a photomultiplier tube and an output cathode follower stage (fig. 3–145). Table 3–71 lists associated detail parts and their functions. The photomultiplier tube contains a cathode, six dynodes, and an anode. The cathode is coated with a substance that emits electrons in proportion to the amount of light illuminating the substance. The dynodes are coated with a substance that

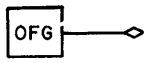


Figure 3–144. Optical Frequency Generator, Logic Block Symbol

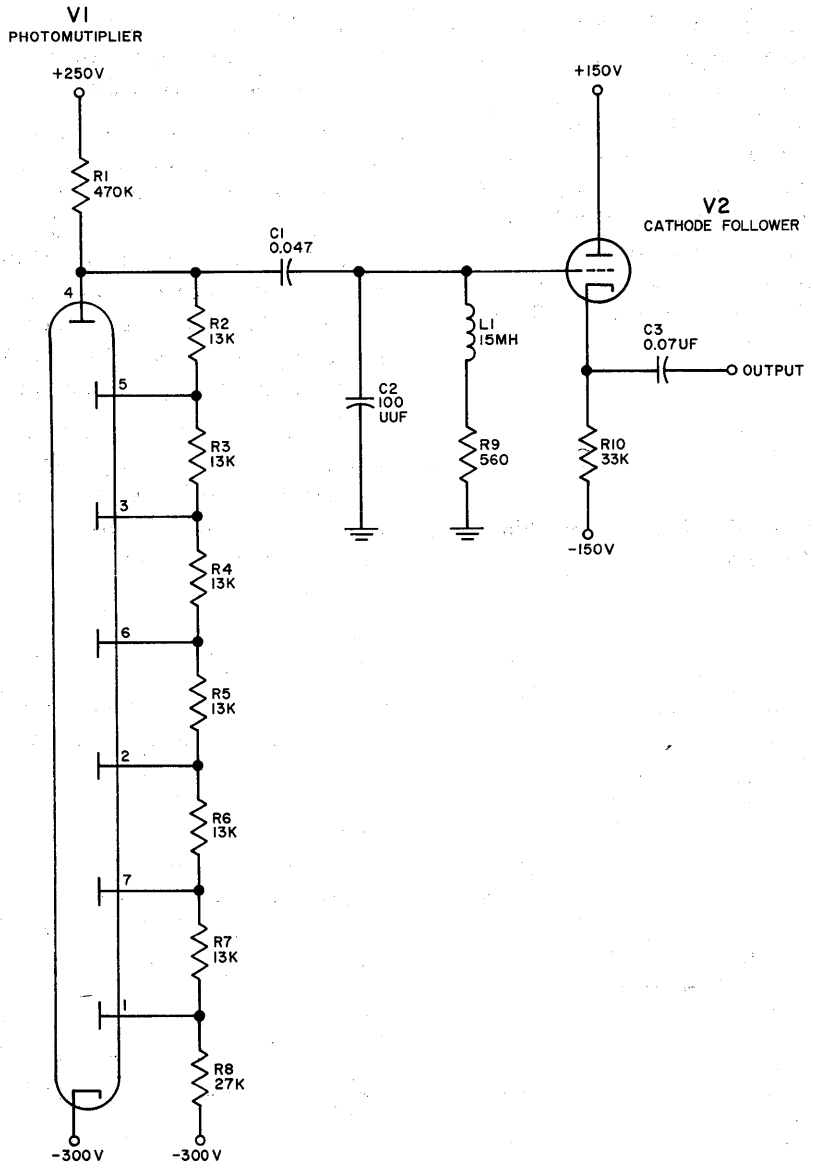


Figure 3–145. Optical Frequency Generator, Electronic Portion, Schematic Diagram

emits electrons when impinged upon by other electrons. This characteristic of giving off electrons is called secondary emission. When secondary emission exceeds the number of incident electrons, amplification occurs. The coating on the dynodes ensures that such an amplification will take place.

Each dynode pin 1, 7, 2, 6, 3, and 5 is successively tied to a higher voltage by means of voltage divider R2 through R8. Electrons emitted by each dynode in succession are attracted by the dynode connected to the next higher voltage level. Thus, the electrons emitted by the cathode of V1 are attracted to dynode 1, pin 1. Electrons emitted by dynode 1 are attracted to dynode 2, pin 7. Secondary electrons are attracted to each of the dynodes at pins 2, 6, 3, and 5 in that order. For every electron that strikes a dynode, several secondary electrons are released. The secondary electrons from dynode 6 are collected by the anode, pin 4. Since the amount of light striking the cathode varies at a sinusoidal rate, then the amount of electrons emitted by the cathode and the number of secondary electrons collected by the anode also vary at a sinusoidal rate. The output of V1 is a 100-kc sine wave. This signal is applied to the grid of V2. A low-Q resonant circuit from grid to ground acts as a bandpass filter. A low-Q filter was selected to provide a bandpass range of 92-108 kc, ensuring sufficient tolerance to accommodate slight deviations in the frequency of incident light intensity variation. Frequencies above and below these limits are bypassed to ground by the filter. As a result, the output is relatively free of distorting noise and harmonics.

The sine wave output of V1 is coupled through cathode follower V2 to the timing pulse generator (par. 3.82). Cathode follower V2 isolates the photomultiplier from the timing pulse generator.

TABLE 3–71. OPTICAL FREQUENCY GENERATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input coupling capacitor
C2	Part of bandpass filter (with L1 and R9)
C3	Output coupling capacitor
L1	Part of bandpass filter (with C2 and R9)
R1	Plate load
R2-R8	Voltage divider
R9	Part of bandpass filter (with C2 and L1)
R10	V2 cathode load resistor

3.59 PHASE SPLITTER

3.59.1 Definition and Description

The phase splitter (PS) converts a low frequency (8.5 to 42.5 cps) triangular wave input signal into two output signals of the same frequency but in phase quadrature (90 degrees out of phase with respect to each other). The logic block symbol for the PS is shown in figure 3–146.

The PS is part of the azimuth motor drive circuit group in the Input System. The input signal is obtained from the level amplifier (par. 3.42). The PS output signals are applied to two power amplifier driver circuits (par. 3.62).

3.59.2 Principles of Operation

Figure 3–147 is the schematic diagram for the PS. Table 3–72 lists associated detail parts and their functions.

The PS consists of a driver which is transformer-coupled to a phase-splitting network. The driver is cathode follower V1. The phase-splitting network is connected across the secondary of T1. Transformer T1 is designed to pass frequencies as low as 4 cps without attenuation or delay and is used as a coupling device in the PS. The use of standard resistor capacitor coupling at low frequencies (8.5 to 42.5 cps) is undesirable because the delay introduced by such coupling is excessive.

The input signal to the PS is a triangular wave. As shown in figure 3–148, the triangular wave is composed of sine waves. The fundamental has the same frequency as the triangular wave. The additional sine waves are odd harmonics of this fundamental. The phase relationship between the waves is important. The fifth, ninth, thirteenth, etc., harmonics are in phase with the fundamental. The third, seventh, eleventh, etc., are 180 degrees out of phase with the fundamental. Figure 3–148 illustrates the composite waveform obtained when the first two odd harmonics with the specified amplitudes are added to the fundamental. The addition of the higher odd harmonics sharpens the peaks and makes the transition between peaks a straight line.

The phase-splitting network consists of two sets of resistor-capacitor networks. Each set has a bandpass range from 8 to 120 cps and phase shift capabilities differing by 90 degrees. The networks can pass the third harmonic of the highest fundamental frequency (42.5 cps) applied to V1. Therefore, the triangular shape of the input signal should appear at the output throughout the

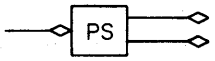


Figure 3–146. Phase Splitter, Logic Block Symbol

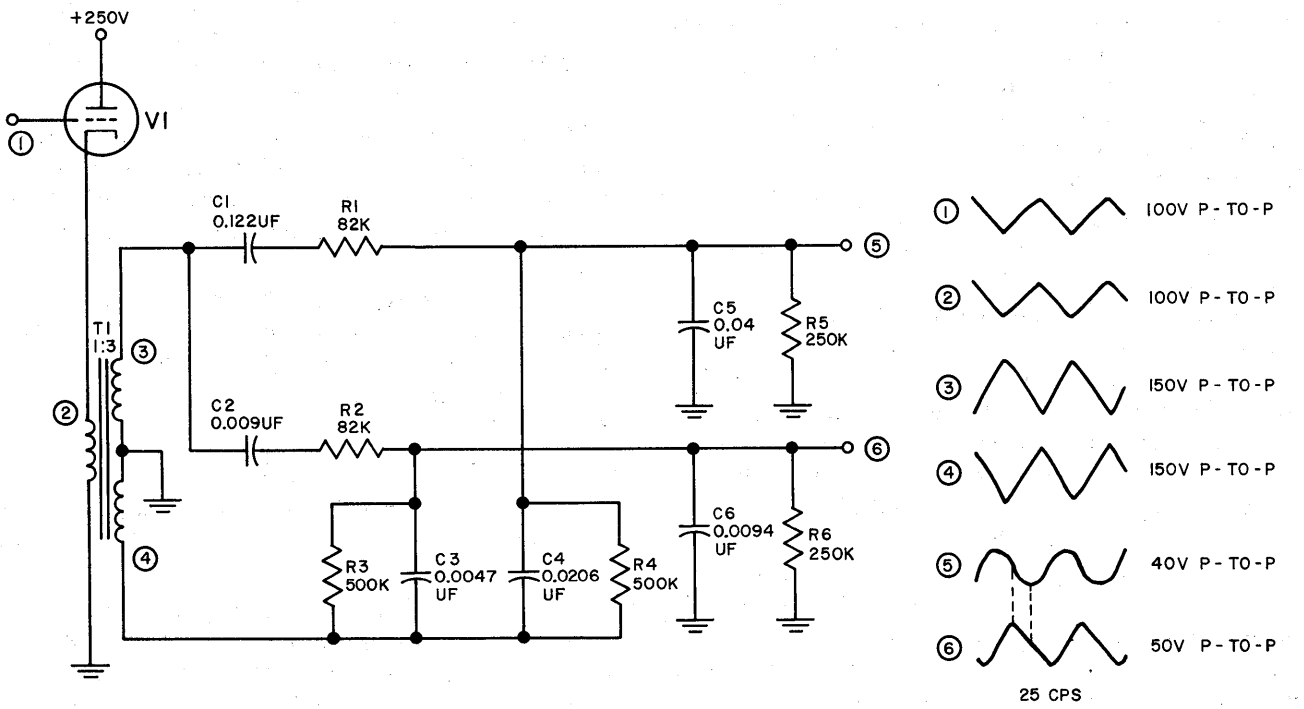


Figure 3–147. Phase Splitter, Schematic Diagram

range of applied frequencies. In figure 3–147, for a fundamental of 25 cps, output waveform 6 is a triangular wave and output waveform 5 is not. The sinusoidal appearance of waveform 5 is due to the difference in phase angle shift between the harmonics and the fundamental introduced by the applicable network.

3.60 PHOTOTUBE AMPLIFIER, MODEL A

3.60.1 Definition and Description

The model A phototube amplifier (AFOA) is a nonlogic circuit which amplifies the output of the photomultiplier circuit. The logic block symbol for the AFOA is shown in figure 3–149. In Input System logic, the FOA receives the raw synchronized target data from the phototube network, amplifies this data, clamps it, and applies it to the counter section.

TABLE 3–72. PHASE SPLITTER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1-C6	Phase-splitting network capacitors
R1-R6	Phase-splitting network resistors
T1	Stepup coupling transformer
V1	Cathode follower

3.60.2 Principles of Operation

Figure 3–150 is the schematic diagram and the associated waveforms of the AFOA. Table 3–73 lists associated detail parts and their functions. The circuit con-

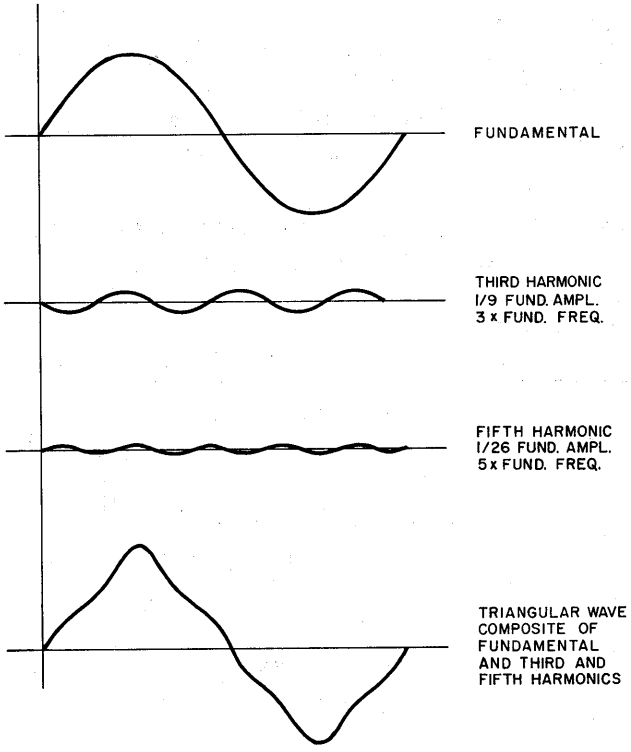


Figure 3–148. Triangular Wave

sists of a single-stage amplifier with a diode limiter and a cathode follower output.

The input signal to the phototube amplifier is the negative pulse output from the photomultiplier tube.

Figure 3–149. Phototube Amplifier, Model A, Logic Block Symbol

This negative input applied to the grid of V1 causes a rise in plate voltage which is coupled through C3 and the contacts of switch SW-1 to the grids of cathode followers V3 and V4. The output of V1 is also coupled through C3 to diode limiter V2. This causes no effect during the negative excursion of the input signal because the voltage at the junction of C3 and C5 makes the cathode of V2 more positive than the plate, making the tube nonconductive. A rise in grid voltage at V3 and V4 causes current to flow through the common cathode load (R9), raising the voltage at the cathode. The output of

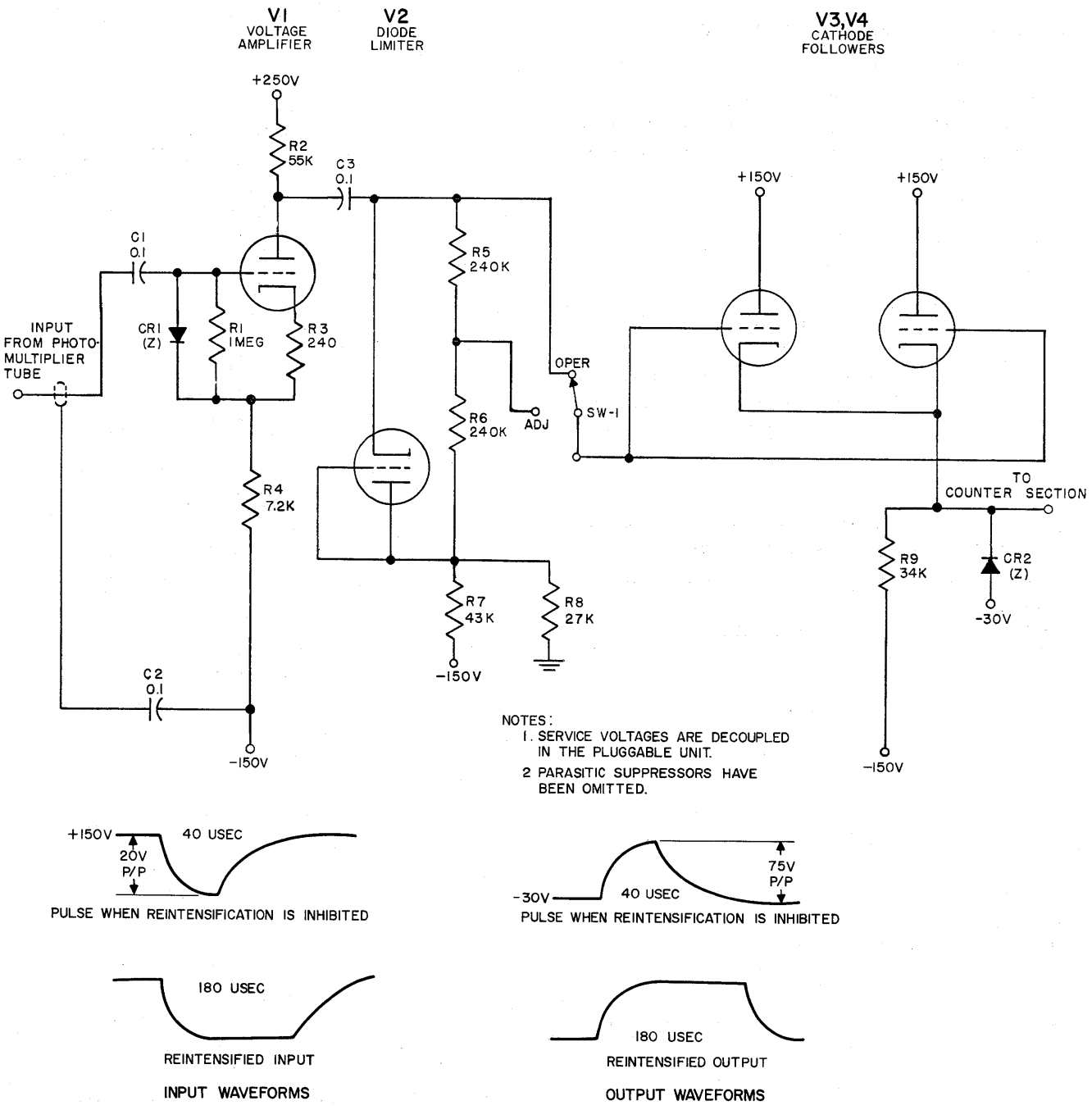


Figure 3–150. Phototube Amplifier, Model A, Schematic Diagram

the cathode follower is a positive pulse employed to trigger the excess target counter.

In addition to performing its counter-triggering function, the pulse is extended from 40 μsec to 180 μsec and returned to the mapper intensification circuit as a reintensify signal.

Through the combined operation of crystal diode CR1 and diode limiter V2, positive input signals to amplifier V1 produce no output from this circuit. The low forward resistance of CR1 shunts any positive input signal around grid resistor R1. V2 prevents the voltage at the grids of V3 and V4 from going below —58V.

3.61 PHOTOTUBE MULTIPLIER, MODEL A

3.61.1 Definition and Description

The model A phototube multiplier (AFN) is a non-logic circuit which allows the normal blue flashes of the mapper display to be detected and converted into electrical impulses. The logic block symbol for the AFN is shown in figure 3–151.

3.61.2 Principles of Operation

Figure 3–152 is the schematic diagram of the AFN. The circuit consists of an end-window type 10-stage multiplier phototube, with a spectral response predominantly in the visible region.

The input to the photomultiplier tube consists of a 40-μsec light pulse obtained from the face of the CRT. Application of the input signal causes the cathode to emit electrons.

TABLE 3–73. PHOTOTUBE AMPLIFIER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Coupling capacitor
C2	Bypass capacitor
C3	Coupling capacitor
R1	V1 grid resistor
R2	V1 plate load resistor
R3, R4	V1 cathode resistors
R5, R6	Voltage divider
R7, R8	Voltage divider
R9	Cathode resistor for V3, V4
CR1	Crystal diode which shunts positive signals around R1
CR2	Crystal diode which clamps cathode follower negative output to —30V

The nonsignal bias at the cathode of the photomultiplier tube is —1,500V (adjustable to vary the gain of the stage). The anode voltage is +150V. With the light pulse striking the specially coated cathode of the phototube, electrons are emitted from the cathode and strike the first dynode. The dynodes are specially coated

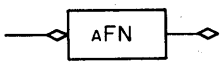


Figure 3–151. Phototube Multiplier, Model A, Logic Block Symbol

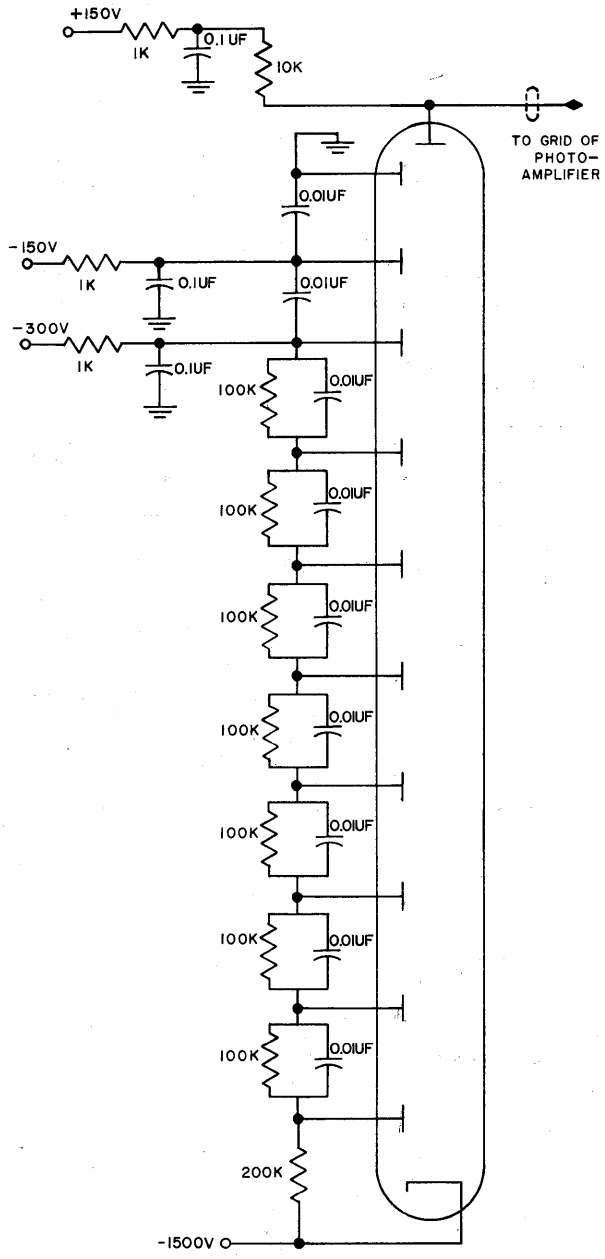


Figure 3–152. Phototube Multiplier, Model A, Schematic Diagram

to permit high secondary emission and have voltage-dropping resistances arranged between them so that each dynode is about 150V more positive with respect to the cathode than the one preceding it. The secondary emitted electrons from the first dynode strike the more positive second dynode, which in turn emits more secondary electrons. The last three dynodes, D8, D9, and D10, emit the greatest portion of these secondary electrons and are progressively connected to —300V, —150V, and ground. The overall action of the dynodes results in a large stream of electrons reaching the phototube anode, thus producing a high gain through the tube.

3.62 POWER AMPLIFIER DRIVER

3.62.1 Definition and Description

A power amplifier driver (PAD) is a logic circuit which generates two equal sinusoidal voltage outputs 180 degrees out of phase with each other. The logic block symbol for the PAD is shown in figure 3–153.

3.62.2 Principles of Operation

Figure 3–154 is the schematic diagram for the PAD. Table 3–74 lists associated detail parts and their functions. The circuit consists of a cathode follower circuit coupled to a balanced network through a stepup transformer.

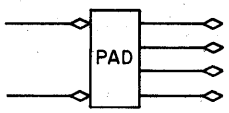


Figure 3–153. Power Amplifier Driver, Logic Block Symbol

There are two identical power amplifier drivers in the azimuth motor drive circuitry. One power amplifier driver is connected to the ϕ output of the phase splitter (par. 3.59) and the other to the ϕ + 90-degree output of the same circuit. Since each power amplifier driver provides two balanced outputs at 180-degree phase difference, it follows that one power amplifier driver provides ϕ and ϕ +180-degree voltage signals and the other, ϕ +90-degree and ϕ +270-degree voltage signals. The following discussion describes one of these two identical power amplifier drivers, the one connected to the ϕ output of the phase splitter.

TABLE 3–74. POWER AMPLIFIER DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Part of phase-shifting network (with C1)
R2, R3	Voltage divider network which sets level of output voltage at —180V
R4, R5	Impedance matching resistors
C1	Part of phase-shifting network (with R1)
T1	Special coupling device which transfers input voltage to PAD circuit with no attenuation of voltage

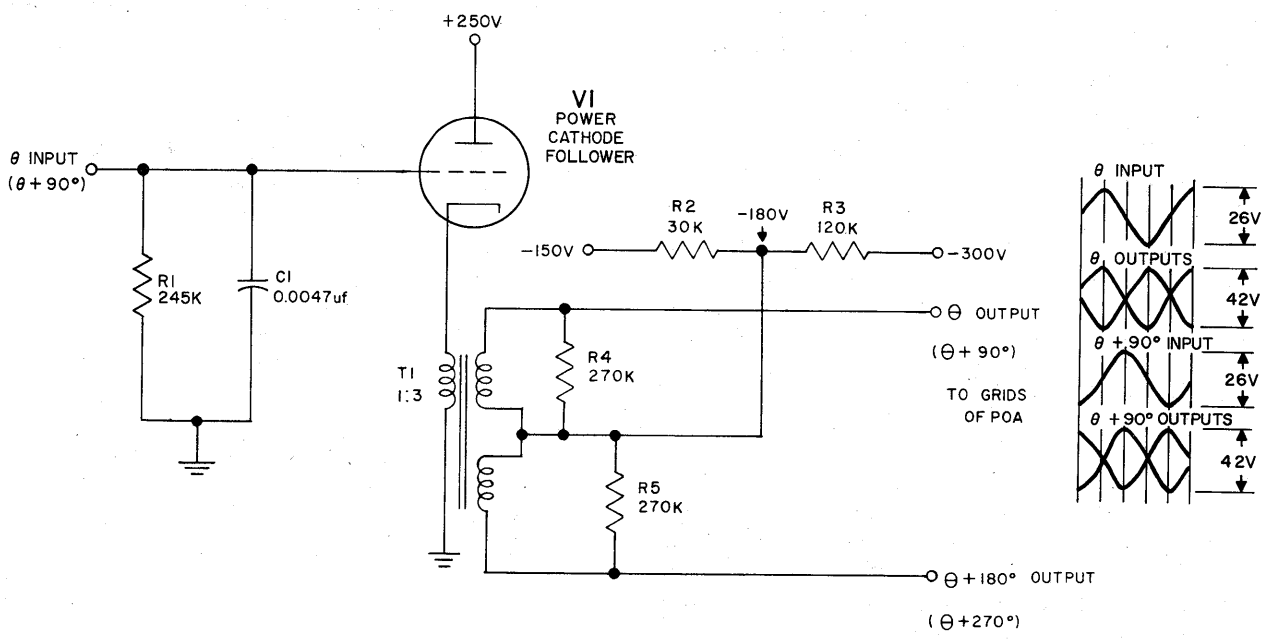


Figure 3–154. Power Amplifier Driver, Schematic Diagram

The approximate sinusoidal azimuth signal from the phase splitter becomes fully sinusoidal at the output of the power amplifier driver. The signal from the phase splitter is applied to the grid of cathode follower V1. The primary of transformer T1 is connected in series with the cathode of V1 which causes the input signal to induce a voltage in the secondary of the same transformer. The center tap of T1 secondary winding is connected to a point of approximately +180V potential. The center-tapped secondary separates the output into two equal voltage signals at 180-degree phase difference.

3.63 POWER CATHANODE, MODEL A

3.63.1 Definition and Description

The model A power cathanode (APCA) is a non-logic circuit designed to drive relatively large capacitor loads at rapid transition times. It provides an in-phase standard level output with considerable power amplification and unity voltage gain upon application of a standard level input.

The APCA is used in the 256² memory primarily to condition the digit plane drivers. The logic block symbol for this circuit is shown in figure 3–155.

3.63.2 Principles of Operation

3.63.2.1 Basic Operation

Figure 3–156 is the block diagram of the APCA. Functionally, the power cathanode is divided into a power amplifier section, consisting of V1A, V1B, V2B, and V3A, and a pulse amplifier section composed of V2A, V4A, and V3B. The input to the power amplifier portion is a differential amplifier (V1A and V1B) which amplifies the difference between the input signal level and a degenerative voltage feedback from output cathode follower V3A. This current arrangement maintains the output level within prescribed limits of either +8V to +12V, or −25V to −30V. Tube V2B is a conventional cathode follower which couples the voltage output of the differential amplifier to power cathode follower V3A.

The pulse amplifier section makes possible the very rapid transition of the output waveform in response to a change in level of the input. For a capacitive load of 0.006 μf, a complete transition from one level to the other is effected in 0.5 μsec under normal conditions. Smaller capacitive loads result in somewhat faster transition times.

Fast rise and fall times are dependent upon how quickly the output load capacitance can be charged each time there is a shift in level at the input. It is the function of the pulse amplifier section to aid in the charging of the load capacitance. The input to this section consists of a differentiating network which, concurrent with a shift in input level, produces an in-phase sharp pulse of voltage. This voltage pulse is amplified and inverted by V2A, and then applied through cathode follower V4A to arrive at the grid of V3B 180-degrees out of phase with the voltage level at the grid of V3A; that is, a negative pulse occurs during rise time and a positive pulse during fall time. The negative pulse almost cuts off V3B so that nearly all of the current supplied by V3A is supplied to the load capacitance. This output load capacitance (heretofore charged at −30V) rapidly charges to +10V through V3A, allowing the output level to rise quickly to +10V. Conversely, if the voltage level at the input of V3A is falling, the voltage pulse at the grid of V3B is positive. This positive pulse causes V3B to conduct heavily in order to rapidly charge the load capacitance, previously charged to +10V, to −30V. Tube V3B, therefore, may be considered a variable impedance, functioning only at the precise moment there is a change in level at the input of the power cathanode circuit. When the input level is rising, V3B is almost cut off and presents a high impedance, permitting the load capacitance to charge quickly through V3A. When the input level is falling, V3B presents a low resistance charging path for the load capacitance.

3.63.2.2 Detailed Operation

The schematic diagram of the APCA, is shown in figure 3–157. Table 3–75 lists associated detail parts and their functions. With a −30V level at the grid of V1A, the voltage at the cathodes of V1A and V1B is approximately −27V. The second input to the differential amplifier is of approximately −28V and is applied to the grid of V1B. This potential is obtained at the junction of resistors R23 and R27 in the cathode circuit of V3A. The difference in the two voltages applied to V1B results in a net bias of −1V, resulting in a +90V level at the plate. This voltage and diode CR1 determine

Figure 3–155. Power Cathanode, Model A, Logic Block Symbol

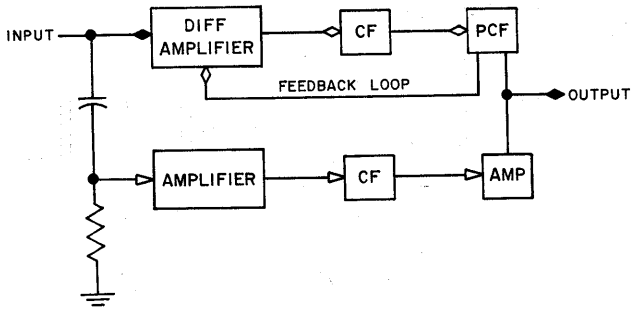
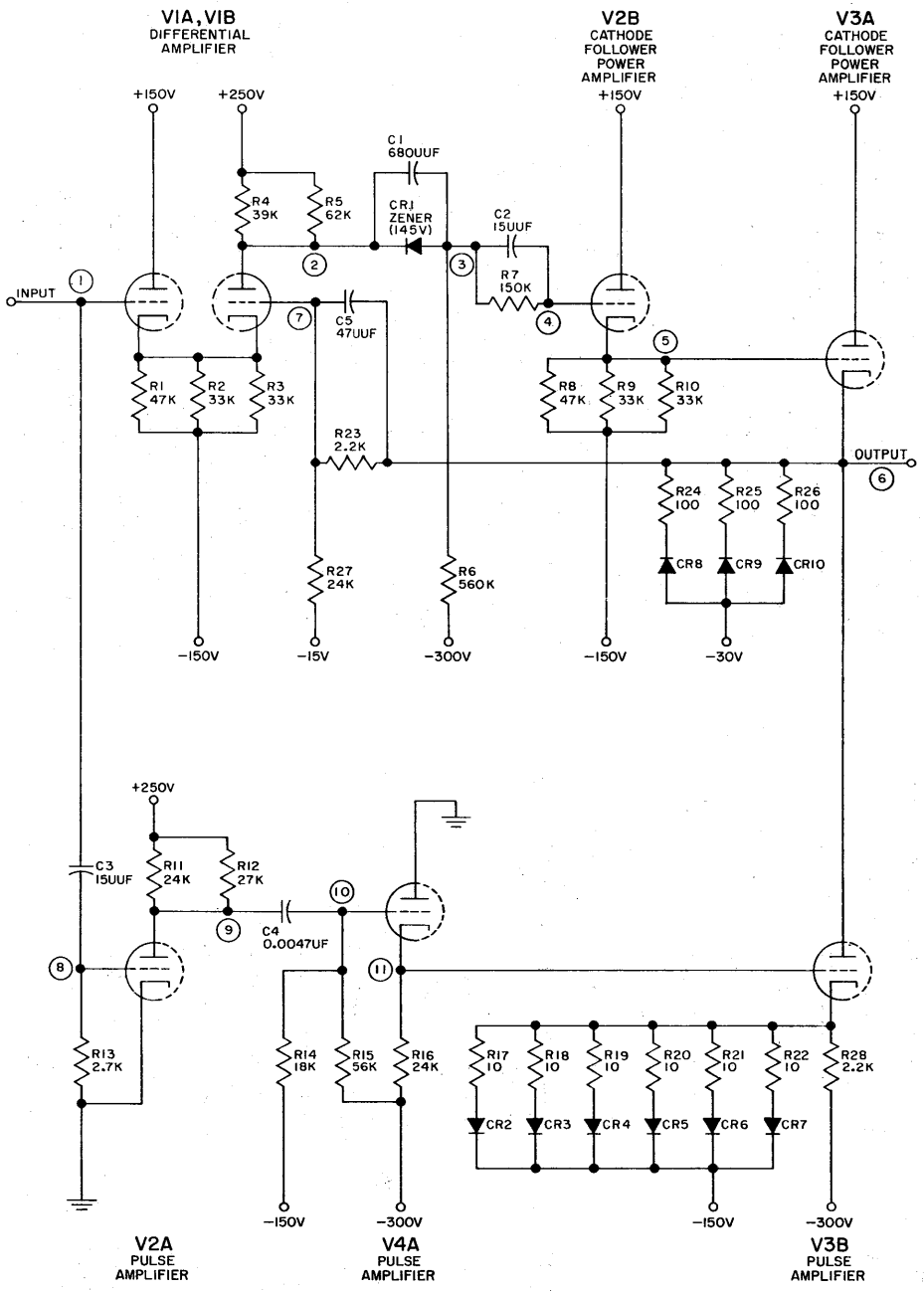


Figure 3–156. Power Cathanode, Model A, Block Diagram



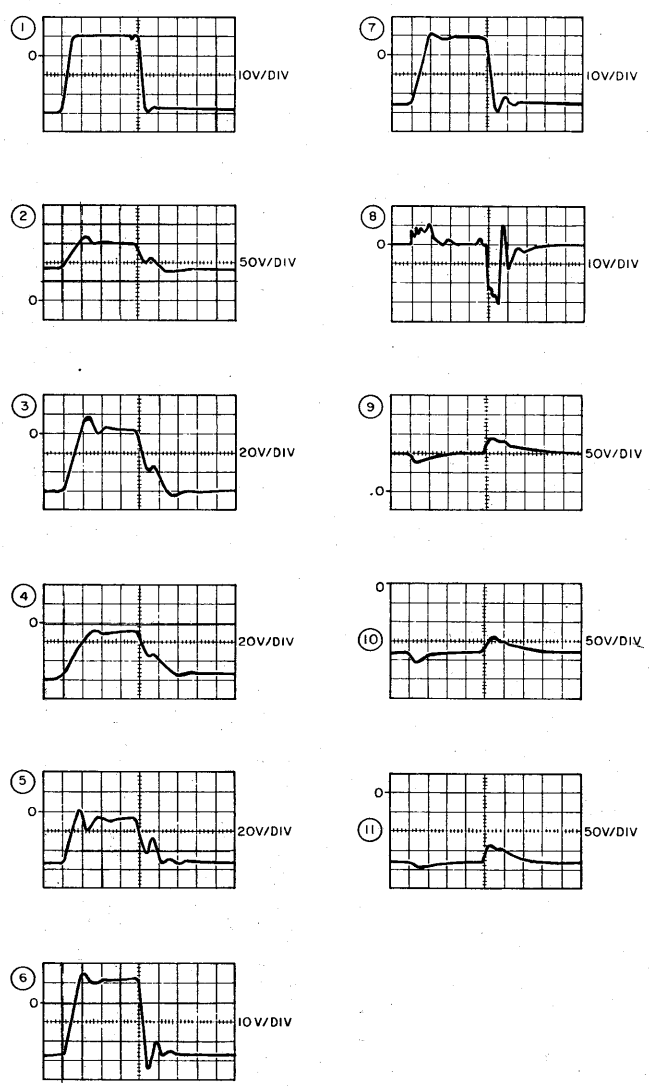


Figure 3–157. Power Cathanode, Model A, Schematic Diagram

the voltage at the grid of V2B. In any case, when the plate voltage of V1B is +90V, the voltage applied through R7 to the grid of V2B is —50V. Approximately the same potential is present at the cathode of V2B and, because of the common connection, at the grid of V3A. With an input of approximately —50V, the output voltage of V3A is approximately —30V. Diodes CR8 to CR10 prevent the output level from attaining a negative potential greater than —32V. Slight variations above and below an ideal output of —30V are compensated for by the operation of the differential amplifier. If, for example, the output level drifts in a less negative direction, the grid of V1B will increase proportionately. As a consequence, conduction through V1B will increase, and its plate voltage will drop below +90V. This small negative swing in plate voltage is applied through V2B to the grid of V3A to adjust its conduction and restore the output level to —30V. A similar analogy may be drawn for the case where the output voltage drifts slightly in a more negative direction.

When the input level at the grid of V1A is +10V, the output level of the APCA rises accordingly. When the level shifts, both the power amplifier and pulse amplifier sections are operative, the latter only momentarily. Thus, the cathodes of V1A and V1B rise to +10V, and the voltage fed back to the grid of V1B is +8V. The resulting —2V bias produces an output level at the plate of V1B of +140V. The potential at the grid and cathode of V2B and at the grid of V3A is approximately —5V.

At times other than the transition periods, V3B is biased at approximately —20V, the difference between a cathode potential of —160V and a grid potential of —180V obtained at the cathode of V4A. The grid level of V4A, which is obtained from voltage divider R14 and R15, is at approximately —186V.

During the transition period, the rise time is differentiated by C3 and R13. The product of this operation is a positive-going pulse which, after amplification and inversion by V2A, appears as a —25V pulse superimposed on the —186V at the grid of V4A. The cathode of V4A follows the input grid voltage. Because the grid of V3B is d-c coupled to the cathode of V4A, tube V3B is driven toward cutoff by the large negative pulse of voltage. At this time, the input to V3A is —5V and that tube conducts heavily, affording a low resistance charge path for the load capacitance. The net result is a swift charging of the load capacitance and a steep rise in output level.

When the input conditions are reversed, that is, when the level is shifting from positive to negative, the pulse applied to the grid of V3B is positive. The positive pulse allows V3B to conduct heavily. In this fashion, a rapid fall time is obtained since the capacitance is charged through a relatively low impedance. When V3B is conducting heavily, it draws approximately 600 ma of current. This large cathode current is obtained by clamping the cathode at —150V and driving the grid positive with respect to the cathode.

TABLE 3–75. POWER CATHANODE, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2, R3	V1A, V1B, cathode bias resistors
R4, R5	V1B plate load resistors
R6	CR1 current-limiting resistor
R7	V2B current-limiting resistor
R8, R9, R10	V2A cathode load
R11, R12	V2A plate load
R13	V2A bias resistor
R14, R15, R16	V4A bias resistors
R17-R22	Current-limiting and equalizing resistors for diodes CR2-CR7
R23	Feedback resistor between output and V13 grid
R24, R25, R26	Current-limiting and equalizing resistors for CR8, CR9, CR10
R27	Grid return for V13
R28	V3B cathode resistor
CR1	Coupling diode
CR2-CR7	Clamping diodes
CR8, CR9, CR10	Clamping diodes
C1, C2	Compensating capacitors
C3, C4	Coupling capacitors
C5	Compensating capacitor

3.63.3 Circuit Refinements

Diode CR1 in the plate circuit of V1B affords a distinct advantage over conventional d-c coupling techniques. Its advantage lies in the fact that the d-c voltage swing necessary to produce an effective signal at the input of the succeeding stage is less than that required when standard d-c coupling methods are employed.

3.64 POWER CATHODE FOLLOWERS

3.64.1 Definition and Description

The power cathode follower (PCF) is a nonlogic circuit that amplifies power. It is essentially a modified cathode follower circuit designed to satisfy the com-

paratively large power requirements of specific types of loads. Its high-input and low-output impedance makes the circuit particularly useful as an isolating device, driving low-impedance loads from a high impedance source. Circuit features are incorporated into the PCF to regulate the output levels and to maintain or shape the output waveform. The logic block symbol for the PCF is shown in figure 3–158.

There are 25 models of the PCF employed in AN/FSQ-7 and AN/FSQ-8 equipment, each adapted to the driving requirements of its respective load. For example, some PCF's are specifically designed to amplify pulse power, others to amplify level power; some PCF's are employed to drive only resistive loads, others to drive only capacitive loads, and still others to feed resistive-capacitive loads. Each of the 25 models belongs to one of two general groups: standard PCF's and special PCF's. The models are listed in table 3–76; the special PCF's are denoted by an asterisk adjacent to the model designation.

All of the 18 standard PCF's have the same general circuit configuration; each circuit consists of an input differential amplifier section and an output cathode follower section (see fig. 3–159). Degenerative feedback is employed between the sections to stabilize the output voltage. The output is clamped at its lower level. The most significant difference between the standard PCF's is the number of parallel sections in the output cathode follower section. If the rated plate current of a single tube is insufficient to provide required power output, one or more triode sections are added in parallel. The next most significant difference between these models is the value of cathode output resistors. A large cathode output resistance is desirable when driving a resistive load; a small cathode output resistance would make for a fast fall time where a capacitive load is fed. A compromise value is used for a resistive-capacitive load.

The seven special PCF's are standard PCF's which have been modified for specific applications. These modifications are discussed in paragraph 3.64.2.3.

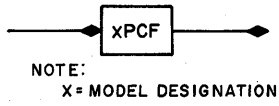


Figure 3–158. Power Cathode Followers, Logic Block Symbol

3.64.2 Principles of Operation

3.64.2.1 General Analysis

All PCF's, both standard and special, consist of an input differential amplifier and an output cathode follower section (fig. 3–159). Specific models employ degenerative feedback to stabilize the output voltage and output clamping to protect subsequent circuits. The feedback is applied to the differential amplifier, and in effect, adjusts the voltage applied to the cathode follower section, maintaining the PCF output at a constant level for a given input level.

Figure 3–160 is a simplified schematic diagram of a differential amplifier; the circuit consists of a cathode follower (V1) and an amplifier (V2). The inputs (input 1) to the cathode follower section of the differential amplifier are usually +10V and –30V levels. The output of V1 is direct-coupled to the cathode of V2 (common cathode resistor R2 is used). The other input (input 2) to amplifier V2 is a portion of the output voltage of the PCF. Amplifier V2 amplifies the difference in potential between its grid and cathode.

If the PCF output voltage should rise for a given input, the feedback to the grid of V2 becomes more positive and the plate voltage drops. This decrease in plate voltage is applied to the cathode follower section of the PCF and is sufficient to return the PCF output to its established level. Should the output voltage decrease, the reverse action occurs, again restoring the circuit to balance. It is in this manner that the differential amplifier functions as a regulating device, maintaining the output constant within specified limits for a given input voltage.

3.64.2.2 Standard Power Cathode Followers

Since all the standard PCF's are basically the same, only the model A (APCF) will be discussed in detail.

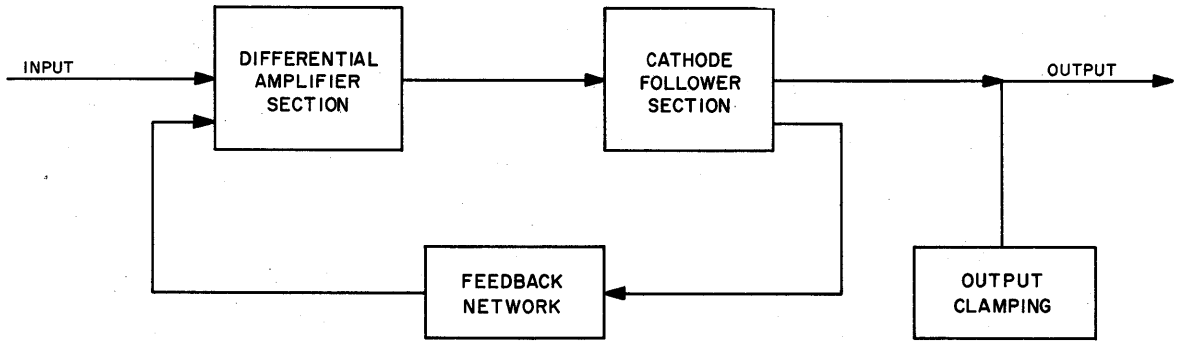


Figure 3–159. Power Cathode Follower, Block Diagram

Table 3–76 lists the model distinguishing features and input-output levels for each standard PCF (the special PCF's listed in table 3–76 will be discussed later). The major column heading STAGE COMPLEMENT lists the number of stages that comprise the differential amplifier and output cathode follower sections and the effective output resistance. Note that only the number of paralleled output cathode followers, value of output resistance, and output levels differ for each standard PCF model.

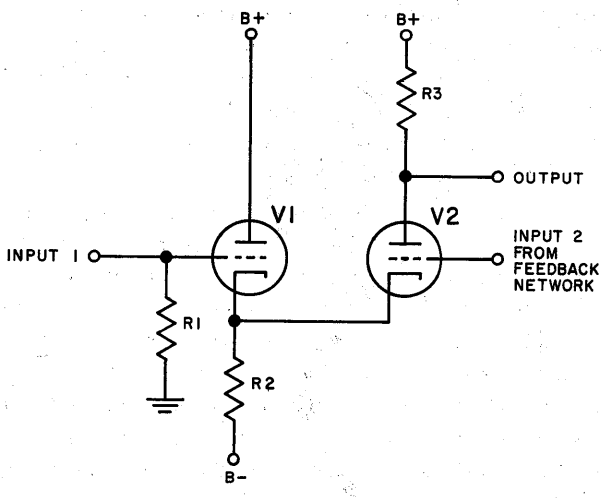


Figure 3–160. Differential Amplifier, Simplified Schematic Diagram

Figure 3–161 is the schematic diagram for the APCF; table 3–77 lists the detail parts and their function. The nominal inputs to the APCF are +10V and −30V levels. With the input at +10V, the common cathodes of V1 and V2 are approximately +11V. Assuming that there is an output voltage of +13.5V at the cathode of V3, the grid of V2 is set at a voltage (+7V) determined by the attenuating network composed of resistors R6 and R7. The resultant voltage at the grid of V2 drives the tube close to cutoff, raising the plate potential to +194V. A proportionate voltage is applied to the grid of the output circuit through voltage divider network R3 and R4 (+10V), causing V3 to conduct heavily and maintaining the output voltage at +13.5V.

If the output voltage drifts below +13.5V, the voltage at the grid of V2 falls. This causes a reduction in plate current of V2 and a resultant increase in the plate potential of V2 and the grid of V3. With a more positive grid, the plate current through V3 increases, causing the output voltage to rise to +13.5V. Similarly, if the output voltage drifts positive, the grid of V2 becomes more positive, increasing conduction and lowering the plate potential of V2 and the grid potential of V3. This reduces the plate current of V3 and causes the output voltage to fall to +13.5V.

Assume that the input level is now −30V; the common cathode potential of V1 and V2 is approximately −26V. With an output of −32V (balanced condition), the voltage fed back to the grid of V2 is −28V. The resultant bias on the grid of V2 causes the plate voltage

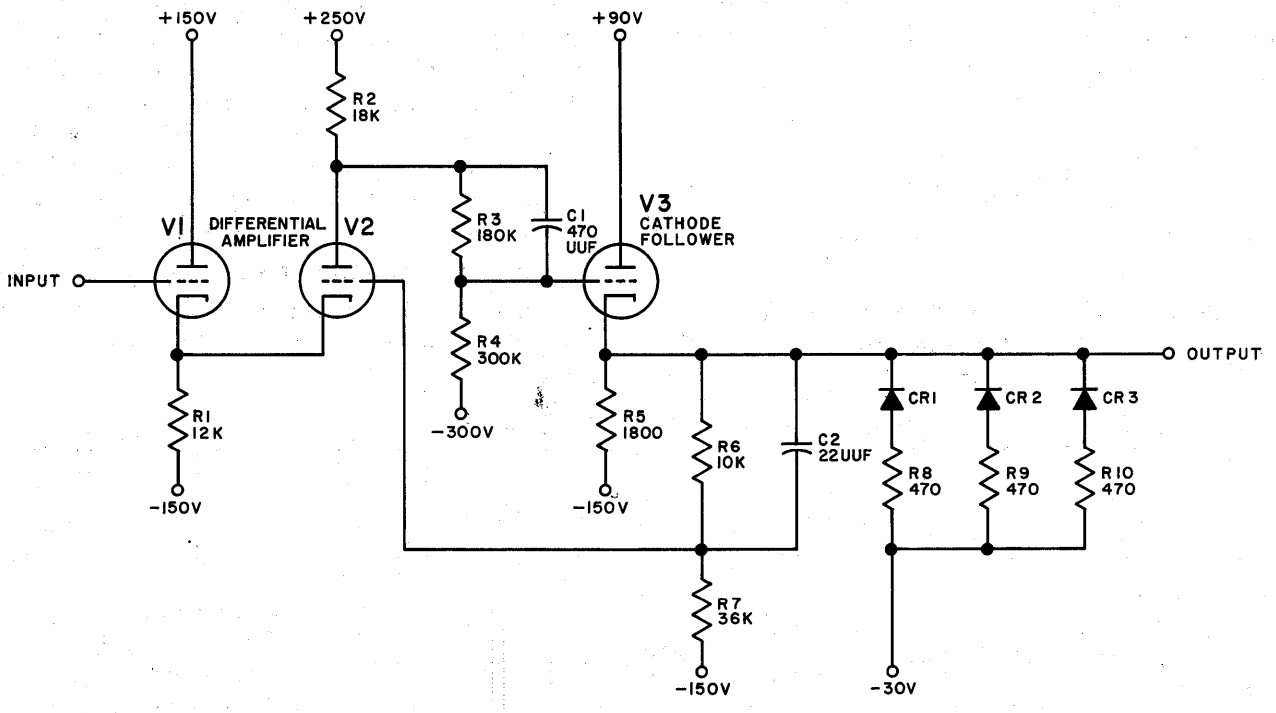


Figure 3–161. Power Cathode Follower, Model A, Schematic Diagram

TABLE 3–76. POWER CATHODE FOLLOWER, MODEL-DISTINGUISHING CHARACTERISTICS

	INPUT LEVELS		STAGE COMPLEMENT						OUTPUT LEVELS	
				DIFFERENTIAL AMPLIFIER			OUTPUT SECTION			
MODEL	UPPER (volts)	LOWER (volts)	INPUT CATHODE FOLLOWER	CATHODE FOLLOWER	AMPLIFIER	INTER-MEDIATE DRIVER	CATHODE FOLLOWER	OUTPUT RESISTANCE	UPPER (volts)	LOWER (volts)
A	+10	−30	—	1	1	—	1	1.8K	+12.75 ±2.75	−32.5 ±2.5
B	+10	−30	—	1	1	—	1	1.8K	+12.75 ±2.75	−16 ±1
*C	+10	−30	1	—	—	—	8	3.7K	+12 ±2	−25 ±5
*E	+10	−30	2	2	2	1	3	600	+6.5 ±1.5	−24 ±4
F	+10	−30	—	1	1	—	2	27K	+12.75 ±2.75	−30.5 ±3.5
G	+10	−30	—	1	1	—	4	27K	+13.4 ±3.4	−30 ±4
H	+10	−30	—	1	1	—	3	900	+13.5 ±1.5	−24 ±4.0
J	+10	−30	—	1	1	—	3	700	+12.0 ±2.0	−32 ±2
K	+10	−30	—	1	1	—	1	450	+13.0 ±3.0	−29 ±3
N	+10	−30	—	1	1	—	4	450	+5.5 ±5.5	−24.5 ±4.5
P	+10	−30	—	1	1	—	4	600	+13.0 ±4.0	−30 ±5.0
*Q	+10	−30	1	2	2	—	4	1.8K	+12.55 ±1.25	−30 ±3.0
R	+10	−30	—	1	1	—	10	200	+5.5 ±5.5	−24 ±4.0
S	0	−15	—	1	1	—	8	900	+3.35 ±3.35	−23 ±3.0
T	+10	−30	—	1	1	—	2	980	+12 ±2.0	−26.5 ±5.5
U	0	−24	—	1	1	—	2	3K	+5.0 ±5.0	−30.5 ±1.5
V	0	−24	—	1	1	—	2	1.8K	+5.0 ±5.0	−30.5 ±1.5
W	+10	−30	—	1	1	—	3	640	+12 ±2.0	−30.5 ±2.5
Y	+10	−30	—	1	1	—	6	320	+5.0 ±5.0	−16 ±1.0
Z	+10	−18	—	1	1	—	3	900	+8.0 ±5.0	−16 ±1.0
*AA	+10	−30	—	—	1	—	1	1.8K	+12.5 ±2.5	−31.5 ±1.5
*DD	+10	−30	—	1	1	—	4	900	−27	−61.5 ±6.0
FF	+10	−30	—	1	1	—	2	1.2K	+12.0 ±3.0	−30 ±2.0
**GG	+10	−21	1	**	**	—	1	3.2K	+12.5 ±2.5	−30
*HH	+10	−30	—	2	2	1	5	360	+12 ±2.0	−33 ±3.0

Special power cathode followers
***Grounded grid amplifier used instead of differential amplifier*

of V2 to fall to +100V. As a result of voltage divider R3 and R4, the grid voltage of V3 equals −50V and an output voltage of −32V is developed at the cathode of V3. Changes in this output level are fed back to the grid of V2, causing the output to be restored to its normal level in the same manner as described above.

Capacitor C1 compensates for the transition time loss caused by voltage divider R3 and R4. Capacitor C2 is a speedup capacitor in the feedback network which reduces positive and negative overshoot in the circuit. Clamping diodes CR1, CR2, and CR3 protect subsequent circuits should the +90V supply fail and also clamp the lower output level at approximately −32V.

Refer to table 3−77 for the function of detail parts not discussed.

3.64.2.3 Special Power Cathode Followers

The special PCF's are modified standard PCF's. Therefore, since the fundamental building block of these PCF's is a standard PCF, the special PCF's will only be discussed in terms of their modifications with respect to the APCF discussed earlier. A summary of model distinguishing features and input-output levels is listed in table 3−76 (special PCF's are designated with an asterisk) and should be referred to during the following discussion.

The CPCF consists of an input cathode follower which feeds a PCF output section made up of eight paralleled cathode followers. The CPCF does not employ an input differential amplifier section and therefore does not contain a feedback loop.

TABLE 3−77. POWER CATHODE FOLLOWER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Speedup capacitor
C2	Feedback capacitor (speedup) reducing positive and negative overshoot
CR1, CR2, CR3	Output clamping diodes
R1	Common cathode resistor for V1 and V2
R2	Plate load resistor for V2
R3, R4	Voltage divider
R5	Cathode resistor for V3
R6, R7	Feedback voltage divider network
R8, R9, R10	Current limiting and equalizing resistors for CR1, CR2, and CR3, respectively

The EPCF is employed as a pulse power amplifier instead of a level power amplifier. The input stage is an isolation cathode follower comprising two triodes in parallel whose output is capacitively coupled to a differential amplifier. The output of the differential amplifier is applied to the output cathode follower section through an intermediate driver stage.

Special QPCF also employs an input isolation cathode follower whose output is capacitively coupled to a differential amplifier. The differential amplifier section employed in the QPCF differs from the one used in the APCF; the amplifier portion consists of two amplifiers instead of one. Feedback from the output is applied to both of these amplifiers. One amplifier has a regulative effect upon the output when the signal is at an up level and cut off when the signal is at a down level. Conversely, when the output is at a down level, the other amplifier provides regulation and is cut off on the up level. As a result of this dual feedback, clamping diodes are not employed in the output circuit.

The AAPCF is identical to the APCF with the exception of the input stage. The input stage is composed only of the amplifier portion of a differential amplifier. However, the AAPCF must be driven by a model B cathode follower. When used together with this cathode follower, the AAPCF is identical to the APCF.

The DDPCF is similar to the QPCF in that a dual feedback loop is employed. Differences between the two models extends to different output levels and circuit complement.

Special GGPCF does not employ a differential amplifier but instead contains an input cathode follower feeding a grounded grid amplifier. The grounded grid amplifier provides undistorted amplification without polarity inversion. The output of the grounded grid amplifier is capacitively coupled to the cathode follower output stage. Feedback is not employed in the GGPCF. Both the up and down output levels are clamped, instead of only the down level as in the APCF.

The most significant difference between the HHPCF and the APCF is the use of an additional stage. The HHPCF employs a cathode follower driver between the differential amplifier and output cathode follower section. The grid and cathode circuits of this stage contain clamping diode networks to improve response time of the circuit, to clip overshoots, and to diminish the effect of loading by subsequent circuits.

3.65 POWER INVERTER

3.65.1 Definition and Description

The power inverter (PI) is a nonlogic circuit which produces a power pulse. The logic block symbol for the PI is shown in figure 3−162.

3.65.2 Principles of Operation

Figure 3—163 is the schematic diagram of the power inverter. Table 3—78 lists associated detail parts and their functions. The circuit consists of three stages: a voltage amplifier which provides signal inversion, a cathode follower which power-amplifies the inverted signal, and a feedback amplifier which provides clamping action. With no input signal applied, tube V1A conducts. When the input signal is applied, the grid of V1A is driven negative, and the tube is cut off. With the tube cut off, the plate voltage rises, and at the same time C3 in the output circuit begins to charge toward the plate supply voltage. The rise in plate voltage of V1A, which

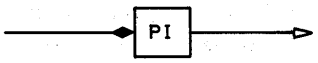


Figure 3—162. Power Inverter, Logic Block Symbol

TABLE 3—78. POWER INVERTER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	V1A grid resistor	R12, R13, R14	Current-limiting and equalizing resistor for CR4, CR5, and CR6
R2	V1 plate load resistor	CR1	Clamps V1A grid at —130V
R3, R4	Voltage divider	CR2, CR3	Part of V2 grid-biasing network (with R8, R9)
R5	V1A cathode resistor	CR4-CR6	Clamps output at —30V
R6	V1B cathode resistor	C1	Input coupling capacitor
R7	Part of low frequency bypass network (with C2)	C2	Part of low-frequency bypass network (with R7)
R8, R9	Part of V2 grid-biasing network (with CR2, CR3)	C3	V1 output waveshaping capacitor
R10, R11	V2 cathode load resistors	C4	Coupling capacitor between V1 and V2

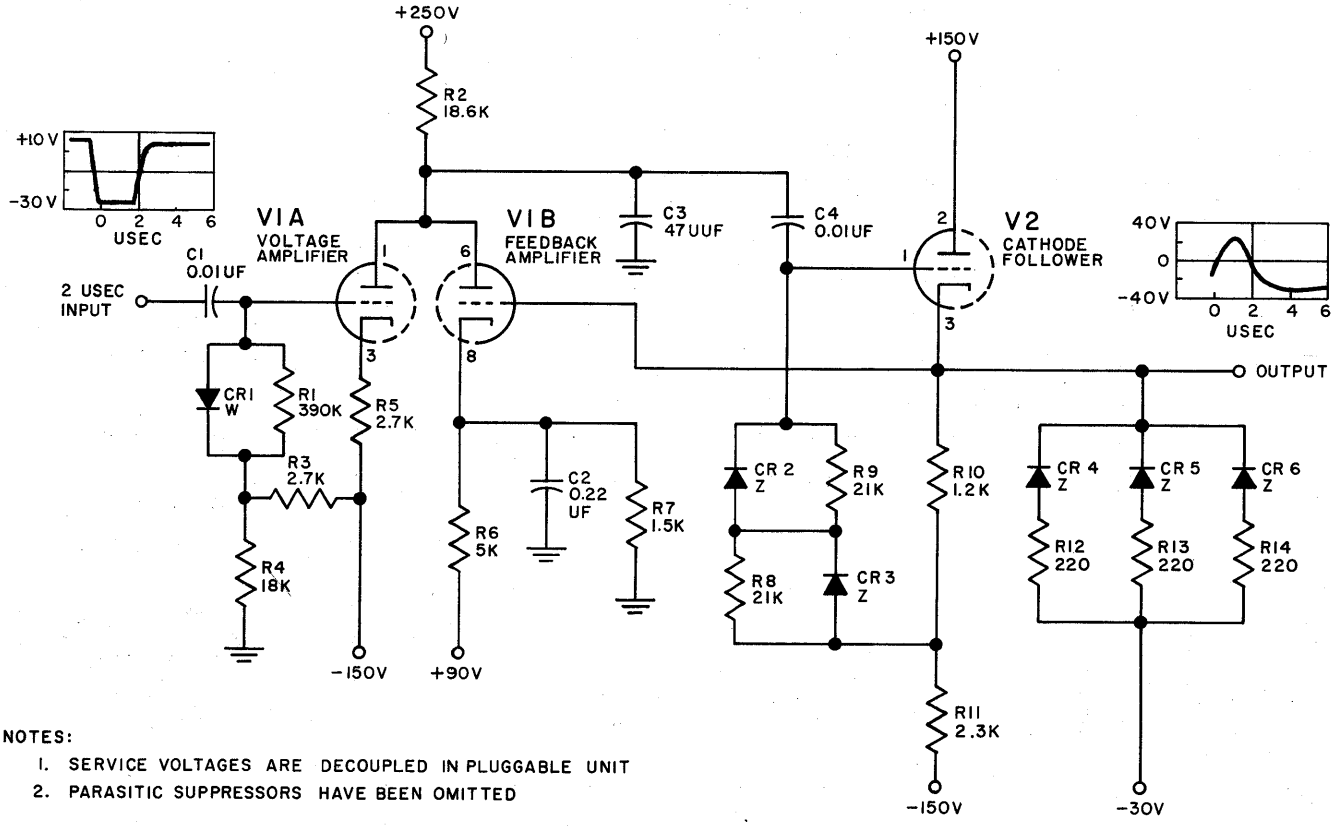


Figure 3—163. Power Inverter, Schematic Diagram

is coupled to the grid of cathode follower V2, causes a rising output voltage in V2 which is fed back to the grid of V1B, the feedback amplifier. V1B conducts, preventing further charging of C3 and thereby clamping the upper level of the cathode follower output voltage.

The plate supply for V1A and V1B is +250V. The cathode supply is −150V for V1A and +90V for V1B; the level at the grid of V1A is approximately −130V because of a voltage divider network between the grid and the −150V supply. When the negative 2-μsec pulse is applied to the grid of V1A, the grid level swings to approximately −170V, cutting off the tube. At this point, the plate voltage on V1A rises and C3 begins to charge through the plate load resistance toward the +250V supply. When the level of the voltage across C3 reaches +145V, the plate of V1B rises to the same potential as the capacitor. Simultaneously, the rise in plate voltage of V1A, which is coupled through C4 to the grid of cathode follower V2, overcomes the bias on V2, and the tube conducts. The rise in current through the cathode load of V2 causes a rising voltage across the load. This rising voltage is directly coupled to the grid of V1B. When the level of the rising grid voltage reaches +17V, V1B conducts. This action prevents further conductivity increase in V2. Thus the cathode follower output voltage is clamped to +17V at its upper level.

When the input pulse to V1A is terminated, V1A once again conducts. This causes a fall in the plate voltage which is coupled to the grid of V2, cutting V2 off. With V2 cut off, two actions occur: V1B is also cut off because of the cathode voltage decrease of V2, which is fed back to the grid of V1B; the falling cathode output voltage of V2 is clamped to the −30V level by diodes CR4, CR5, and CR6. Thus, the output of V2 is pulse restricted to an upper level of +17V and a lower level of −30V.

3.66 POWER OUTPUT AMPLIFIER

3.66.1 Definition and Description

A power output amplifier (POA) is a nonlogic circuit whose output is utilized to energize one of the two phases of the azimuth drive motor. There are two identical POA's in the azimuth motor drive circuitry. The second is used to drive phase 2 of the azimuth motor. The logic block symbol of the POA is shown in figure 3–164.

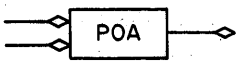


Figure 3–164. Power Output Amplifier, Logic Block Symbol

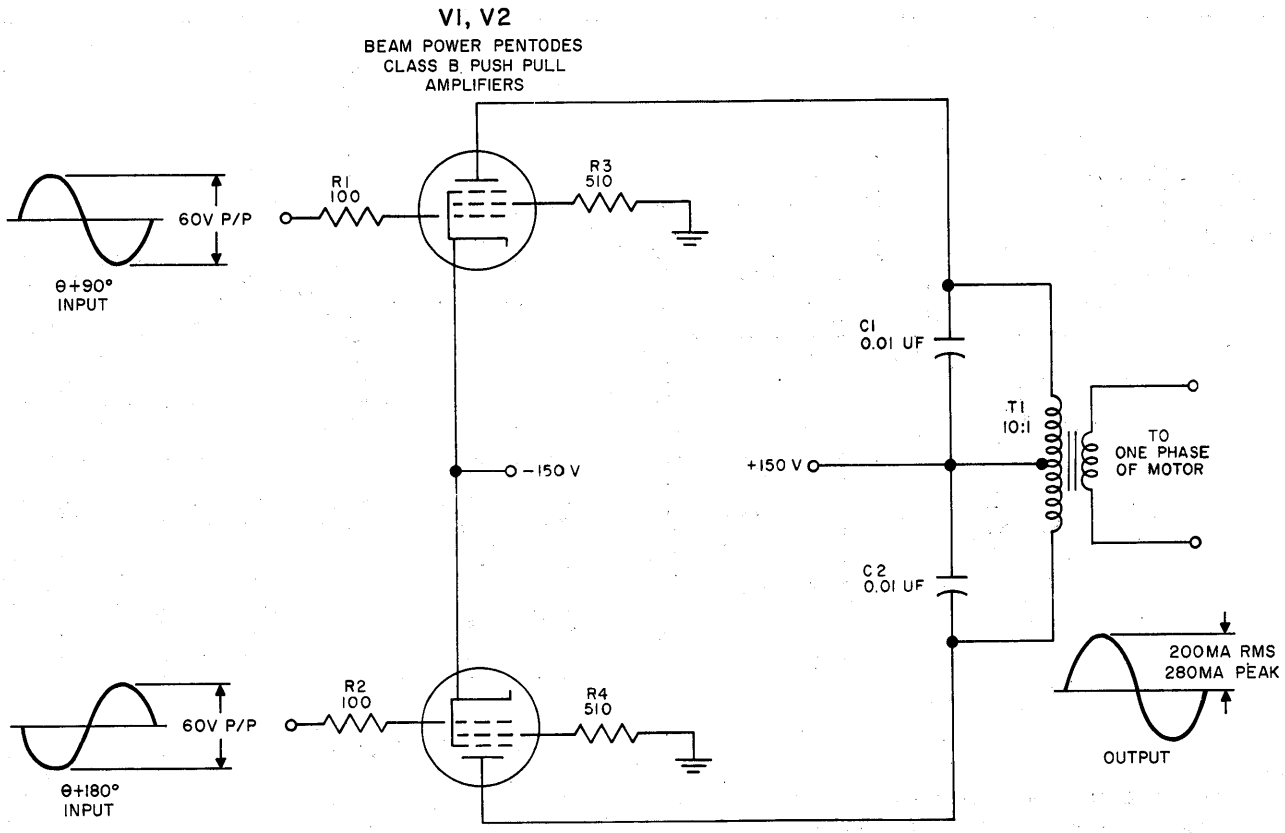


Figure 3–165. Power Output Amplifier, Schematic Diagram

3.66.2 Principles of Operation

Since both POA's mentioned perform in the identical manner, only one of the two is described.

Figure 3–165 is the schematic diagram of the power amplifier. Table 3–79 lists associated detail parts and their function. The circuit utilizes two beam power tubes and associated components.

With no signal applied, the tubes are placed near cutoff from the —30V effective grid bias established by the —180V potential on the grids and the —150V potential of the cathodes. The input signal is a dual 60V peak-to-peak sine wave. The positive half-cycle of one input signal applied to the grid of one of the two tubes overcomes the bias and causes that tube to conduct heavily. At the same time, the other tube is receiving the negative half-cycle of the other input signal, lowering the —30V bias to —60V and driving this tube well beyond cutoff.

TABLE 3–79. POWER OUTPUT AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1, C2	Protects T1 circuit against power surges
R1, R2	Grid input resistors
R3, R4	Screen grid return resistors
T1	Output transformer
V1, V2	Push-pull pentode amplifiers

On the second half-cycle of the input signal the procedure is reversed; the signal applied to the first tube will be negative-going and the signal applied to the second tube will be positive-going. This action results in the first tube being cut off and the second tube being driven into conduction. Thus, the end result is that the two half-cycles of the input signal are each amplified by one of the two tubes in push-pull. Since the primary of the output transformer is in series with the plate circuit of each tube, the total amplified signal voltage is induced in the secondary of the transformer.

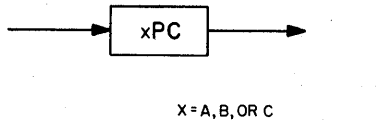
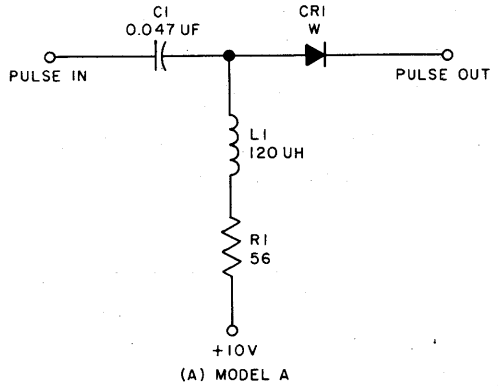
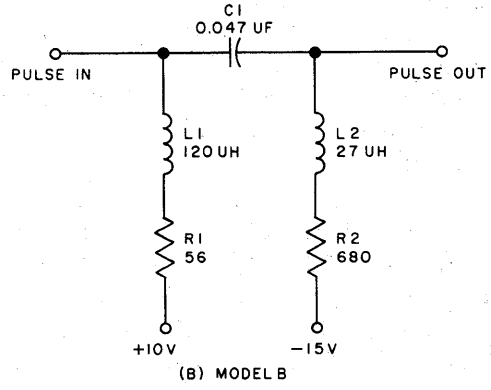


Figure 3–166. Pulse Coupler, Models A, B, and C, Logic Block Symbol





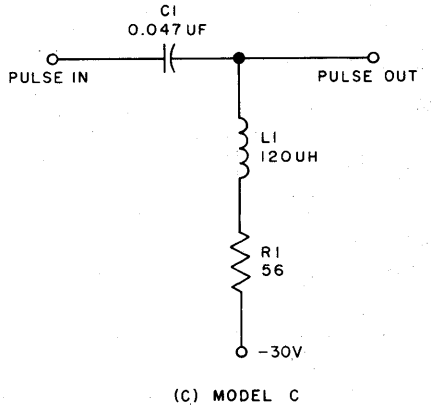


Figure 3–167. Pulse Couplers, Models A, B, and C, Schematic Diagrams

3.67 PULSE COUPLERS, MODELS A, B, AND C

3.67.1 Definition and Description

The pulse couplers (PC) are nonlogic circuits employed as level matching devices between capacitor diode gates (CDG's) and other circuits. Figure 3–166 is the logic block symbol for the PC.

3.67.2 Principles of Operation

Figure 3–167 contains the schematic diagrams for three pulse couplers. Table 3–80 lists associated parts and their functions.

TABLE 3–80. PULSE COUPLER, MODELS A, B, AND C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	USED ON MODEL	FUNCTION
C1	All	Coupling capacitor
CR1	A	Gating diode
L1	All	Peaking coil
L2	B	Peaking coil
R1	All	Damping resistor
R2	B	Damping resistor

The APC couples CDG outputs to any circuit with an input level of less thar +10V. Inductor L1 presents a high impedance to input pulses and a low d-c discharge path for C1 preventing bias buildup. Diode CR1 prevents negative overshoots from appearing in the input of the following circuit.

One leg of the BPC provides the +10V cathode bias for the cathode of the diode in the preceding CDG. The output leg (L2 and R2) establishes the bias for the succeeding circuit. The BPC matches the CDG to a circuit where the input level at not +10V. The CPC is identical to APC except that CR1 is omitted.

3.68 PULSE SHAPERS, MODELS C, D, AND E

3.68.1 Definition and Description

The pulse shaper (SH) is a nonlogic circuit used to amplify the driving power and to reduce the width of input sine wave or pulse signals. Figure 3–168 shows the logic block symbols for the three models of the SH.

In Central Computer logic, two stages of the CSH are used with COSC to produce a train of standard pulses at 0.5-μsec intervals, and three stages of the DSH are used with the DOSC to convert a 1.19-mc sine wave into a train of standard pulses at 0.84-μsec intervals. In the Display System four stages of the ESH are used to shape the 400-kc output of the EOSC into a train of standard pulses at 2.5-μsec intervals.

3.68.2 Principles of Operation

3.68.2.1 Basic Operation

Pulse shapers perform two shaping operations. They amplify a relatively small portion of an input sine wave signal to produce pulses and they reduce the width of input pulse signals. Figure 3–169 illustrates the dual function for sinusoidal (A) and pulse (C) signals. The SH is biased beyond cutoff so that only a portion of the positive excursion (above zero reference) is utilized in turning the shaper on and off. With a sine wave this has the effect of producing a pulse with a width of from one-quarter to three-quarters of the positive half-cycle width. Similarly input pulse width is reduced by utilizing a portion of the pulse rise to overcome the cutoff bias on the shaper. Consequently the SH is turned on and off at a cutoff level on the input pulse which is smaller in width than the base. By this means alone successive stages of shapers would eventually produce pulses of desired width. However, by employing pulse-shaping transformers the process is speeded up so that fewer shaping stages are required to produce the desired reduction in pulse width.

3.68.2.2 Detailed Operation, Model C

The model C pulse shaper is fed by the COSC which produces a 2-mc sine wave output. At this frequency the width of the positive half cycle of the signal is 0.25 μsec.

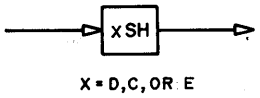


Figure 3–168. Pulse Shaper, Models C, D, and E, Logic Block Symbol

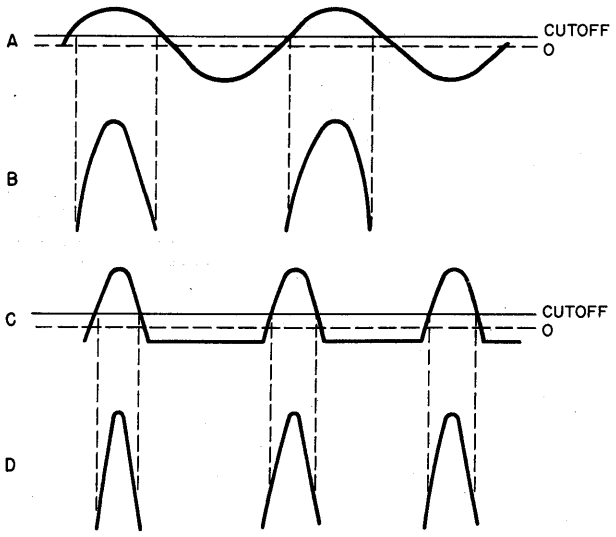


Figure 3–169. Pulse-Shaping Functions of Pulse Shapers on Sine Waves and Pulses

Two stages of pulse shaping by cSH are sufficient to reduce this width to the required standard pulse width of 0.1 ± 0.02 μsec.

Figure 3–170 is a block diagram which depicts the only application of the cSH. The cOSC output is fed to the first pulse-shaping stage where a portion of the positive half cycle of input voltage is amplified to produce a pulse of 120V magnitude and 0.15 μsec width. This pulse is then fed to two output stages in parallel which increase the driving power of the pulse and further reduce the width of the pulse.

Figure 3–171 is the schematic diagram of the cSH. Table 3–81 lists the associated detail parts and their functions. The first and second stages, each a cSH, differ in two respects. The first stage utilizes input 1 and T1. The second stage employs input circuit 2 and a transformer with a turns ratio of 4:1.

The operation of each stage is identical. Consider the first stage to which a 120V peak-to-peak sine wave voltage of 2 mc is applied. The 60V positive half cycle readily overcomes the —15V bias applied through R3, and drives the grid of V1 positive with respect to the cathode. Resultant grid current charges the coupling capacitor (a part of cOSC and not shown). During the negative half cycle, V1 is cut off and the coupling capacitor loses a portion of its acquired charge through R1. With R1 larger than grid-to-cathode resistance, the coupling capacitor gains more charge than it loses. The cumulative effect of a large charge and a small discharge is to build up a negative bias of about 55V on the grid. At this level, the charge accumulated during V1 conduction is equal to the charge lost during nonconduction. As a result, the grid never becomes more than 5V positive with respect to the cathode. Since V1 cutoff voltage is —10V, only the upper 15 volts of the positive half cycle of input voltage is effective in turning V1 on and off. The effective rise in voltage (upper 15 volts) at the input increases current through V1 from 0 to 100 ma, inducing a voltage drop across the primary of V1. The transformer is wired to invert pulses. Therefore the fall of voltage in the primary appears as a rise in the secondary. When input voltage reaches peak value, the current reaches a maximum. The magnetic field collapses, inducing a rise in voltage at the plate of V1. The fall in voltage from a peak value at the input is in step with the collapsing field. Therefore the decrease in current through the primary reaches zero at the same time that the magnetic field becomes zero, and relatively no overshoot appears in the output voltage. Careful selection of damping resistor R1 in input circuit 2 which T1 feeds aids in establishing this synchronism.

TABLE 3–81. PULSE SHAPER, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Damping resistor for T1 secondary
R2, R3	Grid return
T1	Pulse transformer
V1	Tetrode-connected pentode

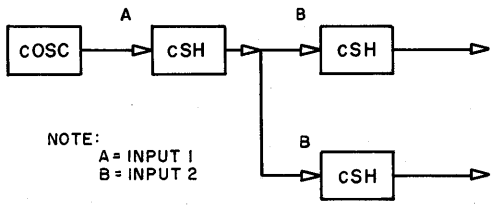


Figure 3–170. Application of Pulse Shaper, Model C, Block Diagram

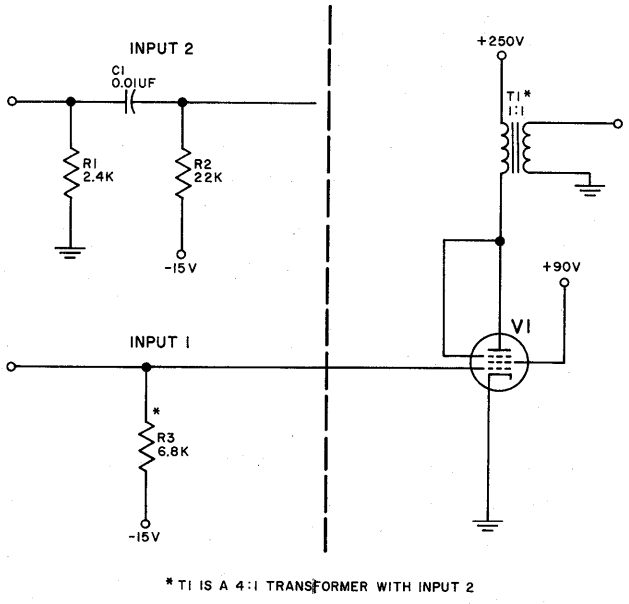


Figure 3–171. Pulse Shaper, Model C, Schematic Diagram

In a similar manner the second SH stage amplifies a portion of the input pulse and decreases the width of the pulse developed across R1 of input 2. Transformer T1 now with a turns ratio of 4:1 amplifies current through V1 by four times to increase the driving power of the output pulse. Unloaded, the SH produces an output pulse with an amplitude of 60V. With proper loading the pulse amplitude is reduced to +30V ±10V.

3.68.2.3 Detailed Operation, Model D

The DSH is fed by the DOSC which produces a 1.19-mc sine wave output. At this frequency the positive half cycle of the signal is 0.42 μsec in width. Two stages of

pulse shaping by DSH are required to reduce this width to the required standard pulse width.

Figure 3–172 is a block diagram which depicts the only application of the DSH. The DOSC output is fed to two identical pulse shapers (DSH) connected in cascade. Each stage successively reduces pulse width as shown. Figure 3–173 is the schematic diagram for the DSH. Table 3–82 lists associated detail parts and their functions. The operation of the DSH is similar to the CSH.

TABLE 3–82. PULSE SHAPER, MODEL D, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input coupling capacitor
R1	Grid return
R2	Damping resistor
T1	Pulse transformer
V1	Tetrode-connected pentode

3.68.2.4 Detailed Operation, Model E

Figure 3–174 is a block diagram which depicts the application of the ESH.

The circuit is fed by the EOSC which produces a 400-kc sine wave output. At this frequency the positive half cycle of the signal is 1.25 μsec wide. Four shaping stages are required to reduce this width to standard pulse width. The four stages are identical except for the input circuit. Figure 3–175 is the schematic diagram for the ESH. Table 3–83 lists associated detail parts and their functions. The two input circuits used to connect four of ESH in cascade are shown.

TABLE 3–83. PULSE SHAPER, MODEL E, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input coupling capacitor
L1	Peaking coil
R1	Grid return
R2	Damping resistor for T1 secondary
R3	Grid return
T1	Pulse transformer
V1	Tetrode-connected pentode

The operation of ESH differs from DSH and CSH in one respect. The width of the positive half cycle of EOSC output is sufficiently large to appear as a square wave to T1 in the first shaping stage. That is, the transformer generates a positive pulse during the voltage rise at the grid and a negative pulse during the voltage fall at the grid. Damping resistor R2 is selected to attenuate negative overshoot and to prevent transformer singing.

3.69 READ-HEAD AMPLIFIER

3.69.1 Definition and Description

A read-head amplifier (RHA) is a nonlogic circuit which amplifies the somewhat sinusoidal signals received from the read head. Table 3–84 lists the two models of the RHA's utilized in AN/FSQ-7 and -8 equipments. Each model is listed by logic symbol, show-

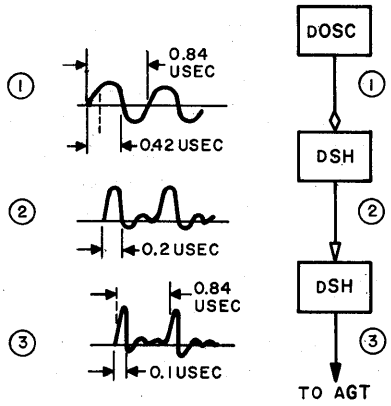


Figure 3–172. Application of Pulse Shaper, Model D, Block Diagram

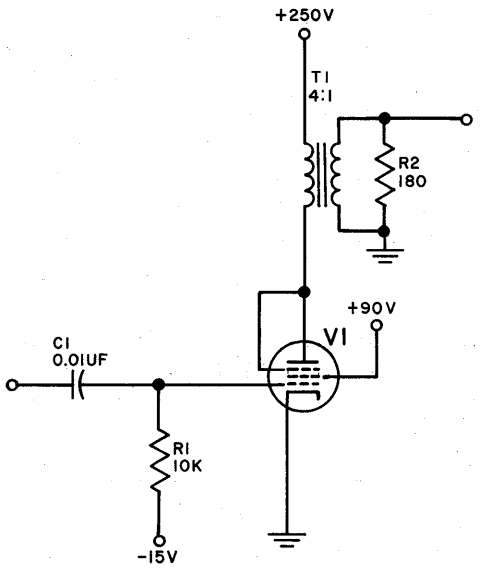


Figure 3–173. Pulse Shaper, Model D, Schematic Diagram

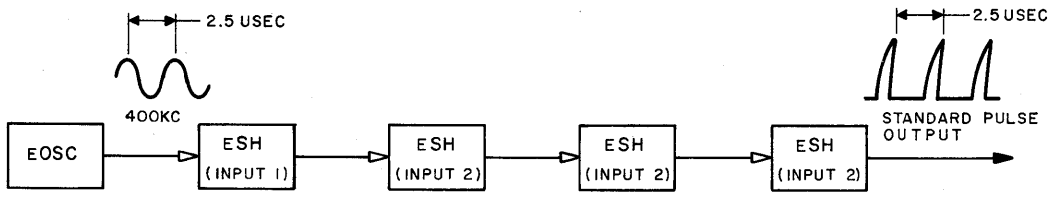


Figure 3–174. Application of Pulse Shaper, Model E, Block Diagram

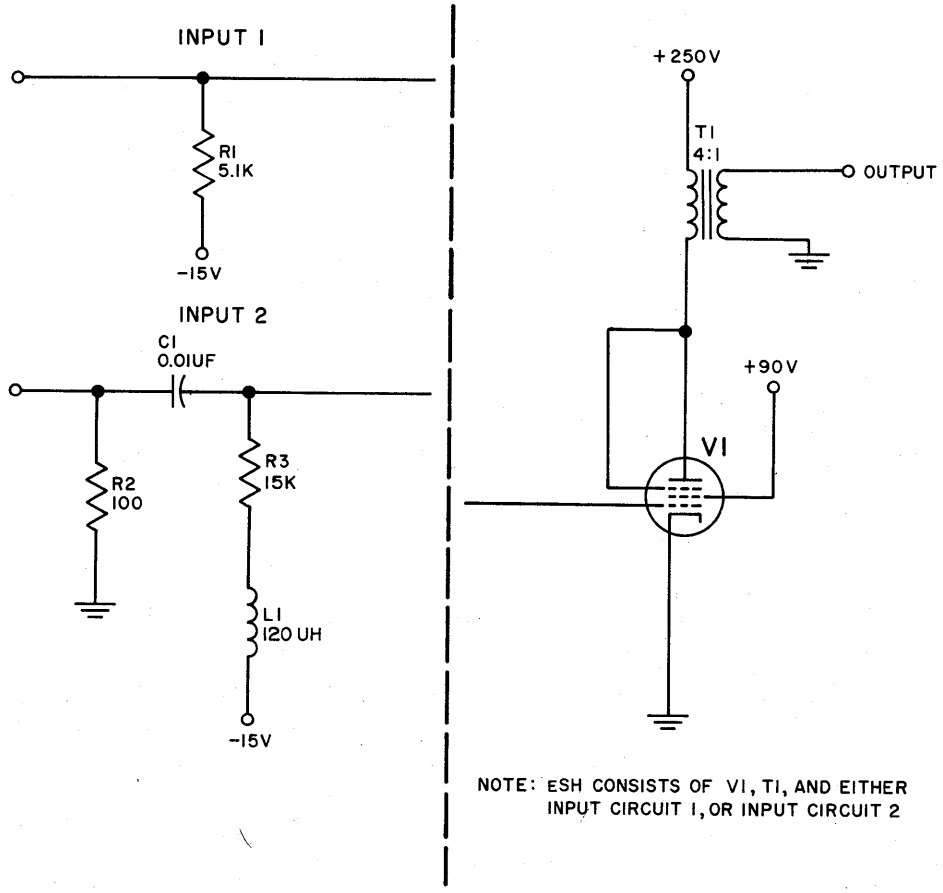


Figure 3–175. Pulse Shaper, Model E, Schematic Diagram

ing the characteristics which distinguish one from the other.

3.69.2 Principles of Operation

Since both models of the RHA perform identically, the model A will be described as a typical RHA circuit in the following discussion.

Figure 3–176 is the schematic diagram of the ARHA. Table 3–85 lists associated detail parts and their functions. The circuit consists of an input transformer, a pentode amplifier, and an output clamp.

In its quiescent condition, the amplifier conducts and causes a voltage drop at its plate. This voltage is clamped to –30V by crystal diode CR2. When a negative input signal is applied to the grid, the output of the

TABLE 3–84. READ-HEAD AMPLIFIERS, MODEL-DISTINGUISHING CHARACTERISTICS

MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A	ARHA	Provides positive pulse output. Drives one input of 2-way AND circuit.
B	BRHA	Provides negative pulse output. Drives one input of 3-way AND circuit and one CFF.

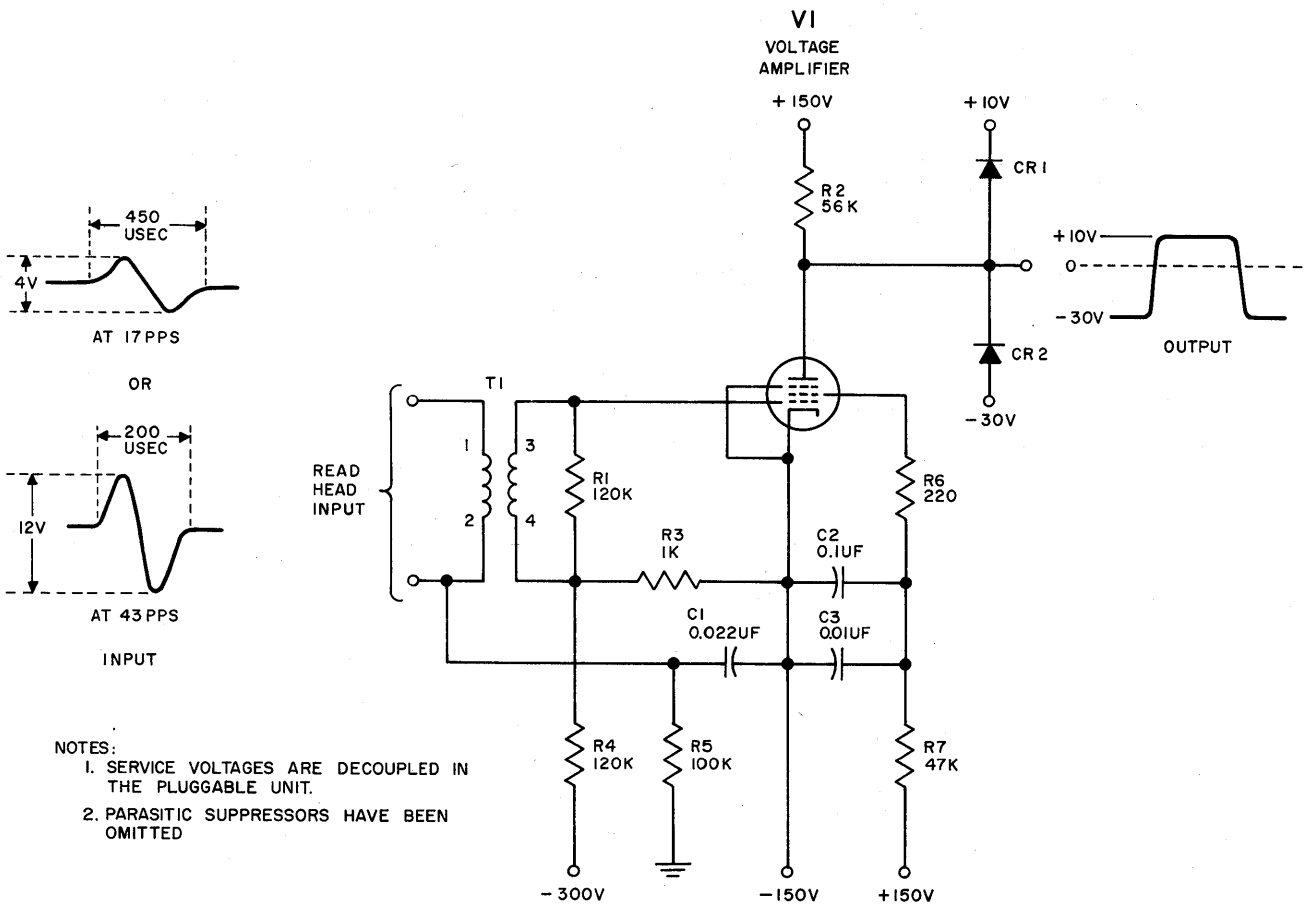


Figure 3–176. Read Head Amplifier, Model A, Schematic Diagram

amplifier is a square-wave pulse referenced at the −30V plate voltage level and extending in the positive direction to the +10V level clamped by crystal diode CR1. Transients on the −150V line are coupled back into the ARHA input line by means of C1. This maintains the grid-to-cathode potential of the circuit constant and, consequently, the operation of the circuit is not upset by transient voltages.

The single-cycle sinusoidal signal from the read head which appears at the primary of transformer T1 is phase-reversed in the secondary of T1 before it reaches the amplifier. Therefore, the first signal to appear at the grid of the amplifier is of negative potential. This first half-cycle of the input signal is then utilized to develop the square-wave output.

Since the first half-cycle of the signal applied to the grid of the amplifier is the negative half, conductivity across the tube decreases. Consequently, the voltage at the plate rises from its quiescent value of −30V to the upper level of +10V clamped by CR1. After the plate voltage reaches the +10V level, the time taken for the input signal to reach its maximum negative value and return to the value causing the +10V plate value constitutes the plateau of the square-wave output. Plate

TABLE 3–85. READ-HEAD AMPLIFIER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Prevents ringing caused by negative excursions
R2	Plate load resistor
R3, R4	Voltage divider
R5	Provides ground reference level for input signal
R6, R7	Screen grid return
C1	Couples transients on −150V line back into input
C2, C3	Screen grid bypass capacitors
CR1	Clamps output at +10V level
CR2	Clamps output at −30V level
T1	Input stepup transformer

voltage then decreases until it return to its —30V quiescent level. The second half of the input cycle will tend to lower the plate voltage even further, but the CR2 clamp will maintain the plate voltage at the stable value of —30V.

3.70 RESET CIRCUIT, MODEL A

3.70.1 Definition and Description

The model A reset circuit (ARS) is a nonlogic circuit which produces a pulse of adequate power and having the characteristics required to return the cores to some predetermined configuration. The logic block symbol for the ARS is shown in figure 3–177.

3.70.2 Principles of Operation

3.70.2.1 Basic Operation

Figure 3–178 is the schematic diagram for the ARS. Table 3–86 lists associated detail parts and their functions. The circuit consists of a cathode follower which incorporates an integrating circuit in its input and clamping circuits in its output. The cathode follower provides the power required by a low-impedance load. The integration circuit rounds off the steep slopes of the input waveform, avoiding the abrupt transitions that might cause shifting action in the register. The clamping circuits hold the output waveform within the voltage limits required for proper clearing action in the register.

3.70.2.2 Detailed Operation

The input signal is integrated by RC network R1 and C1 and applied to the grid of V1. In normal condition, V1 conducts because of the negative voltage on its cathode which is derived from the —150V source. As the input voltage rises, the voltage across the cathode load follows the signal. This voltage change is clamped at its upper and lower limits by two diode-limiting circuits which act in the following manner: Assume that the input voltage, and therefore the voltage at the cathode of V1, is rising. This voltage is applied to the cathode of CR1 and the anode of CR2. Consider the action of CR2 first. The cathode of this diode is at —10V established by the voltage divider between the —15V source and ground. Therefore, CR2 conducts when the rising output voltage reaches —10V, clamping the upper level of the output at this voltage. When the voltage falls below —10V, CR2 ceases to conduct, and the output is unaffected by either diode. However, when the voltage falls below —30V, CR1 conducts and the output is clamped at —30V.

TABLE 3–86. RESET CIRCUIT, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of input integration network (with R1)
R1	Part of input integration network (with C1)
R2	Cathode load resistor
R3	Output current-limiting resistor
R4, R5	Voltage divider network between —15V and ground
CR1, CR2	Crystal diodes which serve to clamp output voltage

Figure 3–177. Reset Circuit, Model A, Logic Block Symbol

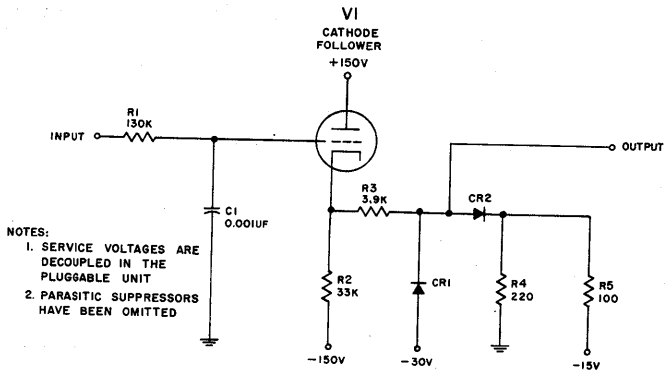


Figure 3–178. Reset Circuit, Model A, Schematic Diagram

3.71 RESET-INHIBIT DRIVER

3.71.1 Definition and Description

The reset-inhibit driver (RID) is a nonlogic circuit which either prevents the read-in of information into an array or furnishes a pulse which produces the read-in of information. The logic block symbol for the RID is shown in figure 3–179.

3.71.2 Principles of Operation

Figure 3–180 is the schematic diagram of the RID. Table 3–87 lists associated detail parts and their functions. The circuit is a 2-stage feedback amplifier. The

Figure 3–179. Reset-Inhibit Driver, Logic Block Symbol

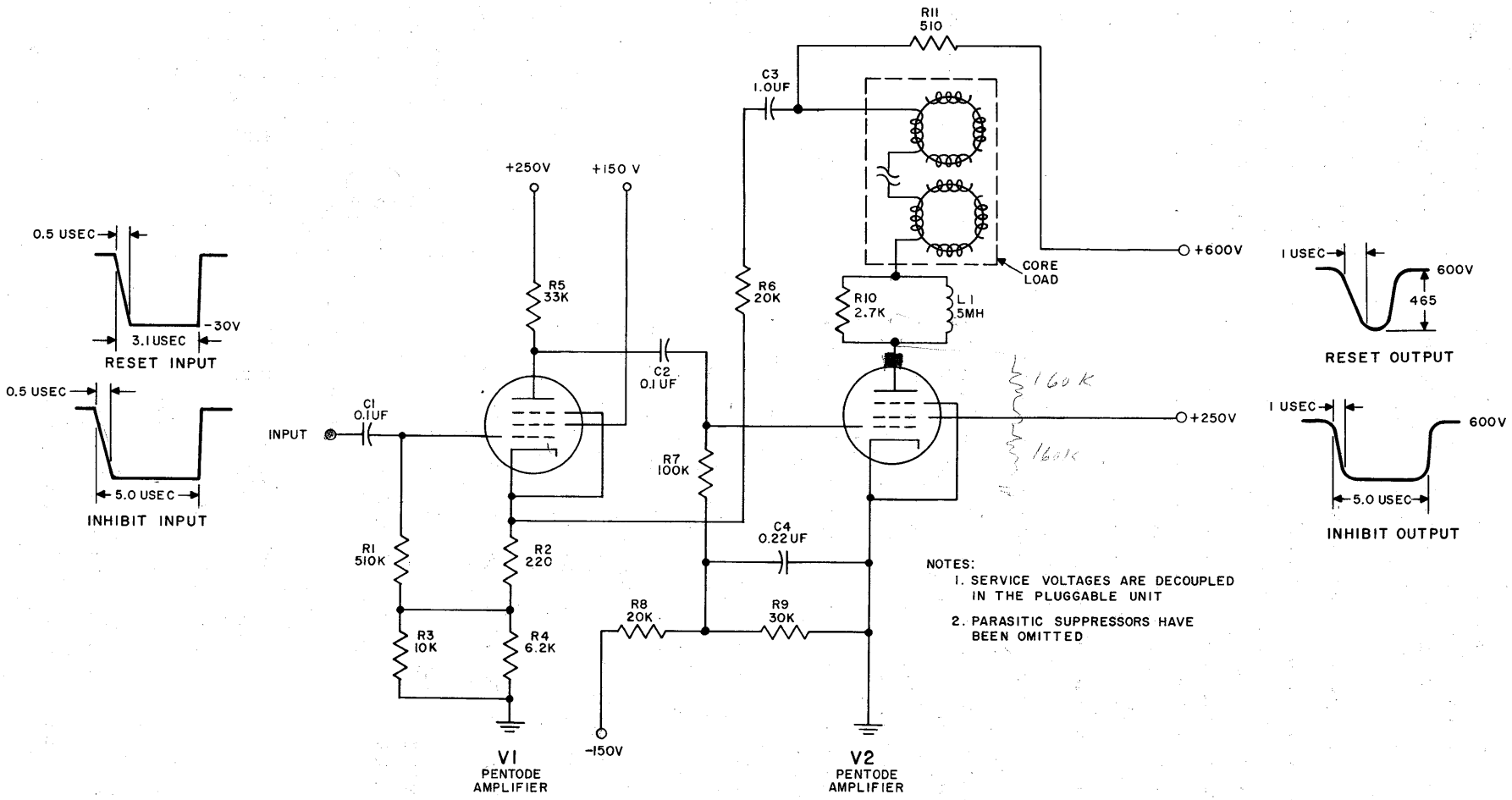


Figure 3–180. Reset-Inhibit Driver, Schematic Diagram

TABLE 3–87. RESET-INHIBIT DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	V1 control grid resistor	R10	Part of plate load for V2 (with L1)
R2, R3, R4	Feedback voltage divider network (with R6)	R11	Load resistance for feedback voltages
R5	V1 plate load resistor	L1	Part of V2 plate load (with R10)
R6	Part of voltage divider feedback network (with R2, R3 and R4)	C1	Input coupling capacitor
R7	V2 control grid resistor	C2	Output coupling capacitor
R8, R9	Voltage divider which provides V2 cathode with —90V bias	C3	Forms part of degenerative feedback circuit which couples plate of V2 to cathode of V1
		C4	Bypass capacitor

second stage supplies a nominal current of 185 ma to reset or inhibit core current drivers.

The first stage input is a negative pulse of 30V amplitude and having a nominal width of 3.1 or 5.0 μsec, depending upon whether the reset or inhibit function is being performed. This pulse is amplified in both stages and delivers current to a load consisting of the reset-inhibit windings of 16 CCD's in series and a load resistance of 510 ohms. The current rise time through the load is approximately 1 μsec, thus providing a proper output current pulse from the CCD's during reset time. C3 and R6 form the degenerative feedback circuit coupling the plate of the second stage to the cathode of the first stage; thus, the amplifier functions as a constant current source. The output voltage is obtained from the plate side of the 510-ohm resistor to ground.

The input pulse to the first stage varies from 0 to —30V. When the input drops to the maximum level, the first tube, which has been conducting, is cut off. The plate voltage, because of no voltage drop across the 33K plate load resistor, rises toward the +250V supply. This rise in plate voltage is coupled through a 0.1-μf capacitor to bring the control grid of the second tube above cutoff, where it has been biased at —90V by the action of the voltage divider across the —150V supply. The positive-going grid voltage results in a flow of plate current through the core load of this stage. The plate voltage drops from the +600V supply output to +135V for a change of 465V.

When the input to the first stage rises to 0V after 3.1 or 5.0 μsec, depending upon whether the reset or inhibit function was complete, plate current flows, producing a drop in plate voltage. The second tube is cut off again by this action and its plate voltage rises to the supply output of +600V.

3.72 SCHMITT TRIGGER, MODEL A

3.72.1 Definition and Description

The model A Schmitt trigger (AST) is a nonlogic circuit which produces a constant amplitude bilevel output and is capable of voltage level discrimination and reasonably fast switching. The logic block symbol for the Schmitt trigger is shown in figure 3–181.

3.72.2 Principles of Operation

The AST is shown schematically in figure 3–182. Table 3–88 lists associated detail parts and their functions. In its quiescent condition, the grid of V1A is considerably negative with respect to its cathode. With the

TABLE 3–88. SCHMITT TRIGGER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Grid bias resistors for V1A
R3	Plate load V1A
R4	Part of V1B plate load (with L1)
R5	Voltage divider (with R7)
R6	Cathode resistor common to V1A and V1B
R7	Voltage divider (with R5)
C1	Part of RC circuit which serves to increase a-c loop gain (with R5)
L1	Choke in plate load of V1B serves to provide peaking action

application of a rising positive level on the grid of V1A, this tube starts conducting. As conduction increases in V1A, the current through R3 causes a decrease in voltage at the plate of this tube and a consequent proportional drop at the grid of V1B because of the action of voltage divider R5 and R7. As the grid voltage of V1B is lowered, this tube heads toward cutoff. Since there is less conduction through the cathode resistors, the cathode goes more negative, increasing the positive-going difference between the grid and cathode of V1A and thereby driving the tube further into conduction. This action continues in the direction of conduction in V1A and cutoff in V1B until V1A saturates. Any further positive movement of the left grid results only in an increase in grid current. As the voltage level on the left grid is now lowered, a point is reached at which the feedback divider moves the right grid to a point where some conduction starts, raising the cathode slightly. Since the left grid is held by the input voltage and the cathode is now moving positive-wise, V1A tends toward cutoff, further raising its plate and the grid of V1B. The circuit has now switched back to the original state.

Figure 3–181. Schmitt Trigger, Model A, Logic Block Symbol

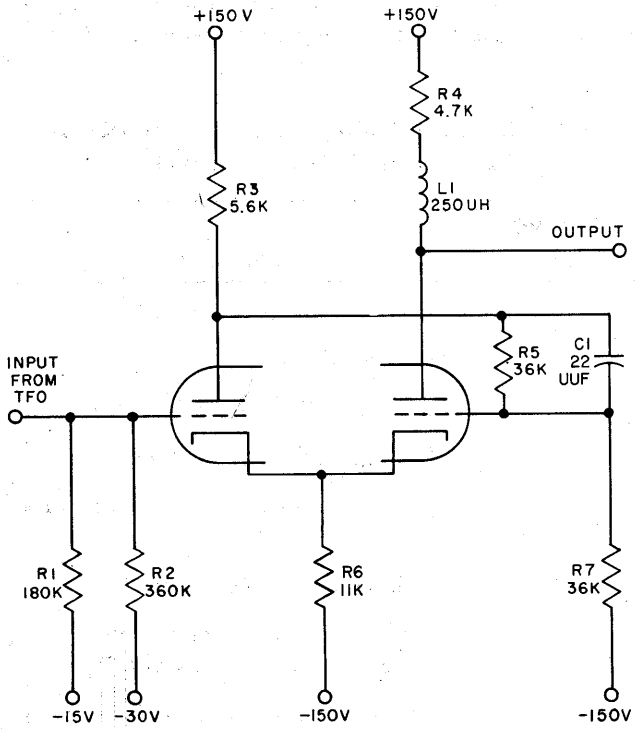


Figure 3–182. Schmitt Trigger, Model A, Schematic Diagram

The input voltage level needed to cause conduction to switch from right to left is somewhat higher than that needed to cause the reverse action. This is due to the difference in the plate load resistors in the two halves of the circuit and produces a hysteresis effect with more inherent stability than that found in a symmetrical circuit.

3.73 SENSE AMPLIFIERS

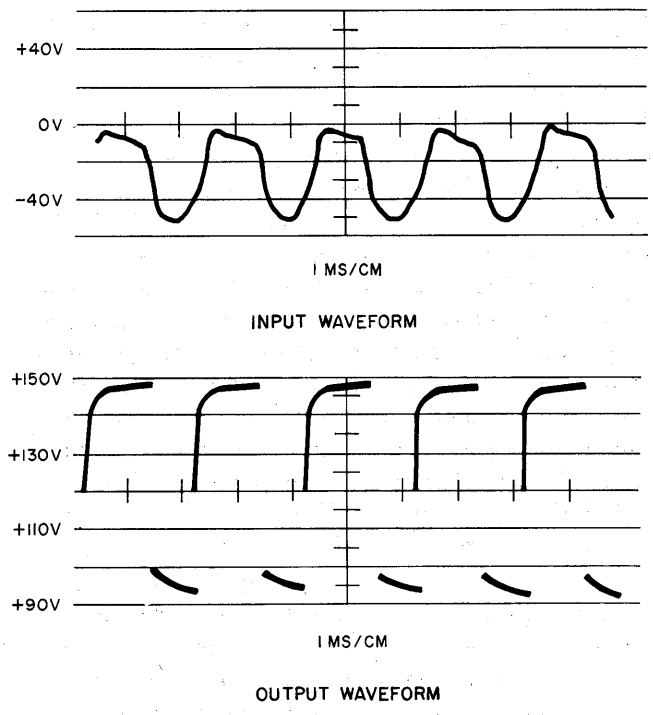
3.73.1 Sense Amplifier, Model B

3.73.1.1 Definition and Description

The model B sense amplifier (BSA) is a logic circuit which develops a positive output signal regardless of the polarity of the input signal. The logic block symbol for the BSA is shown in figure 3–183.

3.73.1.2 Principles of Operation, Basic

Figure 3–184 is a block diagram of the BSA. Two inputs are supplied to the first stage of the amplifier from a sense winding in the array. The difference stages of the amplifier have balanced inputs, and half of the signal induced in the sense winding is applied to each input of the first stage; these input signals are 180 degrees out of phase with each other. The first three stages amplify the difference signal existing between these two inputs and generate difference signals on two output lines. The difference signal on the output lines from the third stage is applied to a detector and is also returned to the first stage to provide negative feedback. Although the two input signals to the detector are of equal amplitude but 180 degrees out of phase, the detector is actuated by the positive input only,



producing a single line output pulse of negative polarity. The negative signal is amplified and inverted by the inverter-amplifier stage to produce a positive pulse output which is fed to a cathode follower. The positive output pulse from the cathode follower is applied to the suppressor grid of a model A gate tube, thereby conditioning the gate tube.

3.73.1.3 Principles of Operation, Detailed

Figure 3–185, foldout, is the schematic diagram and related waveforms of the BSA. Table 3–89 is the associated list of detail parts and their functions.

The first three stages, V1, V2, and V3, form a conventional class A difference amplifier, with negative feedback from the third difference-amplifier plates applied to the grids of the input stage. Tube V1 is a low-noise tube which is used to decrease microphonic noise. With no signal applied to the inputs, the level of both grids is at approximately +1V, with the result that the common cathodes are at approximately +4V. The plates of V1A and V1B are both at approximately +100V. Since both sides of the tube are identical, the plate voltages are equal. If a 100-mv signal is induced in the sense winding, a 50-mv signal to ground is applied to each input. However, the signal on one grid is 180 degrees out of phase with that on the other grid; therefore, one grid rises by 50 mv whereas the other falls by 50 mv. The grid signal causes one plate to fall while the other rises. Since operation is based on the linear portion of the tube characteristics, the changes in plate current are equal but 180 degrees out of phase and the total cathode current will remain the same. The signals from the two plates are resistance-capacitance coupled to the second stage.

The second and third stages further amplify the signal and furnish two equal and opposite output signals to the detector stage. Regardless of the polarity of the input pulse, a positive pulse is generated at one of the two outputs of the third stage. Detector stage V4 is a mixer circuit biased at about 4V, or near cutoff. Both halves of the twin triode which is used as a detector share a common plate load and a common cathode load. Two inputs are supplied by the two outputs of the third difference amplifier, V3, but, since the detector is sensitive to positive signals only, it makes use of only one. A positive signal on either grid produces a negative signal at the plate of V4. This negative signal is coupled to the grid of inverter-amplifier stage V5A. With a 100-mv input to the difference amplifier, the input to the detector is approximately 9V and the resultant output only 6V. The gain of the detector stage is less than unity because of the large cathode resistor employed, and because, owing to the imperfect cutoff of the tube, the negative signal on the second grid has some effect.

Inverter-amplifier stage V5A is a triode amplifier with a gain of approximately 10. The stage is operated at zero bias in order to allow a larger negative input signal to be attained before cutoff. Diode clamp CR1 is used across the grid resistor to prevent base-line shift. Shunt-peaking is used in the plate circuit to decrease the rise and fall time of the signal. Since the amplifier drives a cathode follower (V5B) that has a low input capacity, a relatively small inductance is used. For a 100-mv input to the difference amplifier, the output of the inverter-amplifier is about 52V.

Cathode follower V5B receives a positive pulse from inverter-amplifier V5A, and provides a low impedance source for conditioning the gate tube. The input to the cathode follower is clamped to prevent base-line shift. Two diodes, CR2 and CR3, are used in series because of the high back voltage developed. The grid is biased by means of a voltage divider network connected to a −150V marginal checking line. The grid, and therefore the cathode, is normally at −26V. The gate tube suppressor grid, since it is directly coupled to the output of the cathode follower, is also at −26V in the absence of a signal. If a sufficient signal is supplied to the suppressor grid when the gate tube is sampled, the gate tube conducts and produces a pulse. Conduction of the suppressor grid at this time loads the cathode follower. The loading effect is represented in the form of a notch in the pulse waveform taken at the suppressor grid of the gate tube.

Figure 3–183. Sense Amplifier, Model B, Logic Block Symbol

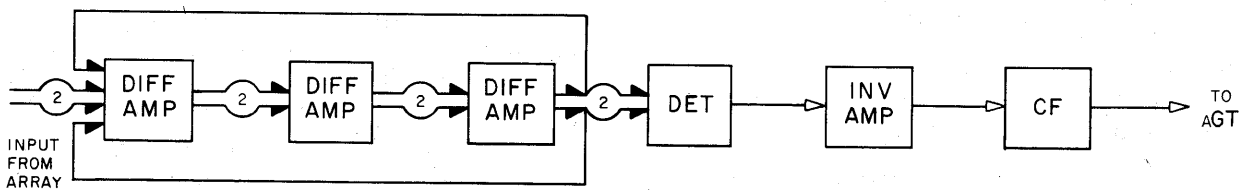


Figure 3–184. Sense Amplifier, Model B, Block Diagram

TABLE 3–89. SENSE AMPLIFIER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1, R2	Input load resistors for V1	R27	Part of voltage divider between −150V and ground (with R30)
R3, R4	Current-limiting resistors	R28, R29	Equalizing resistors for CR2 and CR3
R5, R6	Feedback resistors	R30	Part of voltage divider between −150V and ground (with R27)
R7, R8	Plate load resistors for V1	R31	Cathode resistor for V5B
R9	Cathode resistor for V1	CR1	Part of V5A grid clamping (with R24 and R25)
R10	Part of stabilization network (with C1)	CR2, CR3	V5B grid-clamping diodes
R11, R12	Form part of RC coupling networks between V1 and V2 (with C2 and C3)	C1	Part of stabilization network with (R10)
R13, R14	Plate load resistors for V2	C2, C3	Part of RC coupling network between V1 and V2 (with R11 and R12)
R15	Cathode resistor for V2	C4, C5	Part of RC coupling network between V2 and V3 (with R16 and R17)
R16, R17	Form part of RC coupling network between V2 and V3 (with C4 and C5)	C6, C7	Coupling capacitors between V3 and V4
R18, R19	Plate load resistors for V3	C8	Bypass capacitor in V4 cathode circuit
R20	Cathode resistor for V3	C9	Coupling capacitor between V4 and V5A
R21	Plate load for V4 (with L1)	C10	Coupling capacitor between V5A and V5B
R22	Part of cathode bias network for V4 (with C8)	C11	Bypass capacitor
R23	Grid return for V4B		
R24, R25	Part of grid-clamping circuit for V5A (with CR1)		
R26	Plate load for V5A (with L2)		

3.73.2 Sense Amplifier, Model C, Transistorized

3.73.2.1 Definition and Description

The model C sense amplifier (cSA) is a logic element which functions as a voltage amplifier and a gate circuit. The logic block symbol for this circuit is shown in figure 3–186.

In Central Computer logic, the cSA interprets the output from the sense winding of the 256^2 core memory plane and provides a gated 0.1-μsec pulse to set the memory buffer register if a 1 is read from memory.

3.73.2.2 Principles of Operation, Basic

Figure 3–187 is the block diagram of the cSA. The input to this circuit consists of four identical difference amplifiers, one for each of the four sense sections in a memory plane. Each amplifier is followed by a mixer, and all four mixer outputs are connected to the grounded base amplifier, Q5. All stages shown in figure 3–187 are transistorized with the exception of the vacuum tube pulse amplifier (APA).

For a given memory address, only one of the four sense sections in a plane may provide a 1 signal to an associated difference amplifier. Whenever one of the difference amplifiers receives a signal, its companion mixer provides an output to the grounded base amplifier.

Each of the four difference amplifiers comprises two closely balanced transistor amplifiers which produce an output only when a difference signal (voltages of opposite polarity) is applied at their input. Common mode

disturbances, that is, noise pulses of equal amplitude and of the same polarity appearing at the input of both balanced amplifiers, are rejected. The amplified difference signal is applied to a mixer which, regardless of the polarity of the signal at its input, supplies a negative pulse to the grounded base amplifier. The mixer is biased to function as a clipper to eliminate base line noise.

The output of each mixer is fed through grounded base amplifier Q5 and emitter follower Q6 to a gate circuit consisting of Q7 and Q8. The operation of Q5 and Q6 is analogous to that of a grounded grid amplifier and a cathode follower, respectively. Transistors Q7 and Q8 are connected in series. The application of an amplified 1 signal to Q7 conditions the gate, and the simultaneous application of a 0.1-μsec pulse to Q8 produces an output pulse which is supplied to the pulse amplifier. The pulse amplifier amplifies the signal to standard amplitude and delivers it to a flip-flop in the memory buffer register.

3.73.2.3 Principles of Operation, Detailed

Figure 3–188, foldout, is the schematic diagram of the cSA. Table 3–90 lists associated detail parts and their functions. Transistors Q1 and Q2 in the difference amplifier are biased to operate as Class A amplifiers. Base and collector potentials are obtained at different points along a voltage divider connected between ground and −150V. The emitters are returned to +150V through separate 68K resistors. The large value of these resistors and also of resistors R9 and R10 limits the amplitude of collector current and maintains it fairly constant. Consequently, in the quiescent state, only a small direct current flows through the two halves of the center-tapped primary of T1, resulting in +0.32V at the emitters, +0.3V at the base, and −3.2V at the collectors of transistors Q1 and Q2.

When a 1 is read out of a core in the memory plane, a pulse of voltage about 1-μsec wide and between 60 and 100 mv in amplitude is generated in the sense winding.

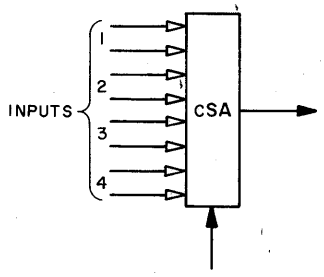


Figure 3–186. Sense Amplifier, Model C, Logic Block Symbol

This voltage is applied to the base of Q1 and Q2 across R3 and R8 which, in combination with R4 and R7, terminate the sense winding with the correct impedance. Since the bases of the difference amplifier are connected to opposite ends of the sense winding, the voltage appearing at the base of Q1 will be 180 degrees out of phase with the voltage at the base of Q2. A negative signal reduces the bias on the transistor to which it is applied and results in an increase in current flow through the associated half of the primary winding of T1. Conversely, positive voltage applied concurrently to the other transistor decreases the current flow through its associated half of the T1 primary winding. These currents in the primary winding complement one another and induce an output voltage in the secondary of T1. It should be noted that common mode disturbances would cause both transistors to operate in phase and that the currents flowing in the primary would then cancel each other. Common mode current amplitude is limited greatly by the 68K resistors.

The output of the difference amplifier is transformer-coupled to mixer transistors Q3 and Q4. The bases of these transistors are connected to opposite sides of the secondary of T1. Both transistors are biased beyond cutoff by a positive potential which is obtained at the arm of R11 in the +90V supply and applied to both bases through the center tap on the secondary winding.

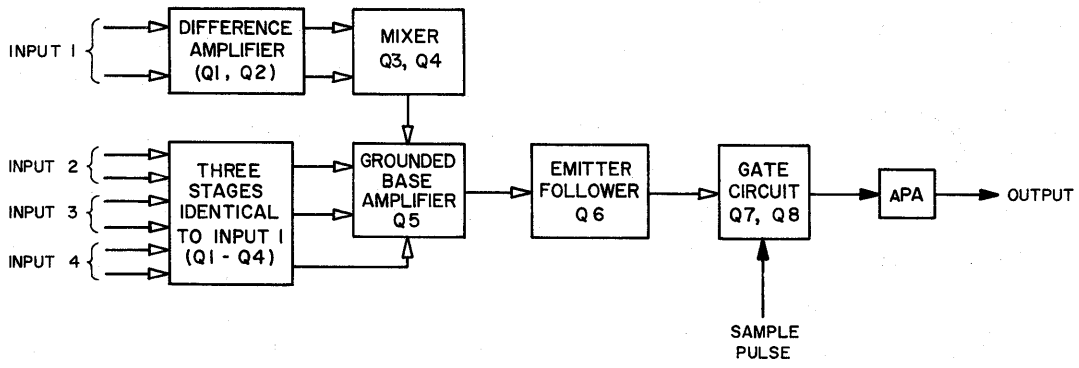


Figure 3–187. Sense Amplifier, Model C, Block Diagram

This bias voltage and the emitter potential establish the clipping level. When a core is switched, the voltage induced in the secondary of T1 is positive at one end of the winding and negative to the other. The transistor whose base is connected to the postive side is driven further into cutoff; the transistor whose base is connected to the negative end is driven into conduction. Thus, for a signal of a given polarity only one of the two transistors in the mixer will conduct. Regardless of which transistor in the mixer conducts, the signal voltage supplied to the emitter of grounded base amplifier Q5 is always negative.

Transistors Q5, Q6, and Q7 are all directly coupled. Consequently, each stage contributes to the quiescent as well as the active state of all.

TABLE 3-90. SENSE AMPLIFIER, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Emitter resistors for Q1 and Q2
R3, R4	Part of voltage divider between −150V and ground (with R7, R8, R9 and R10)
R5, R6	Base resistors for Q3 and Q4
R7, R8, R9, R10	Part of voltage divider between −150V and ground (with R3 and R4)
R11, R12	Part of voltage divider between +90V and ground (with R15, R16, and R17)
R13	Emitter resistor for Q5
R14	Q6 base-biasing resistor
R15, R16, R17	Part of voltage divider between +90V and ground (with R11 and R12)
R18	Q6 emitter resistor
R19	Part of coupling network (with C3)
R20, R21	Voltage divider
R22	Damping resistor
R23, R24	Voltage divider
R25	V1 suppressor grid-dropping resistor
C1, C2	Bypass capacitors
C3, C4	Compensating capacitors
C5	Bypass capacitor
CR1	Clamping diode

In the quiescent condition, Q5 is conducting at saturation because of the large +150V forward bias applied to its emitter. For this condition, its emitter and collector potential is approximately +0.3V. The collector of Q5 is tied directly to the base of Q6. Since the emitter of Q6 is connected to +10V, this stage is also conducting and its emitter voltage is +0.5V. This potential is applied through R19 to the base of Q7 in the sample gate circuit, and is sufficient to hold Q7 at cutoff. Transistor Q8 is also at cutoff, its base being returned to +2.6V at the junction of R20 and R21.

In the operating condition, a negative output from any of the four mixer stages drives transistor Q5 from saturation to cutoff. Its collector potential drops from +0.3V to approximately −2.7V. This negative 3.0V swing is reproduced by Q6, its emitter voltage dropping from +0.5V to −2.5V. The negative voltage drives Q6 further into conduction, thereby lowering the collector impedance of Q7 and conditioning the gate. Application of a pulse (inverted and reduced in amplitude by T3) to the base of Q8 at the time Q7 is saturated, allows Q8 to conduct and to generate a pulse of current in the primary of T2.

The output of the sample gate is a positive pulse having a minimum amplitude of +10V at the primary of T2. The secondary winding increases the pulse ampli-

TABLE 3-91. SENSE AMPLIFIER, BLOCKING OSCILLATOR, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	V1A plate load resistor
R2	V1B grid return
R3	Part of voltage divider between +250V and ground (with R7)
R4, R5, R6	Part of damping circuit which prevents ringing across T2 (with CR1, CR2)
R7	Part of voltage divider between +250V and ground (with R3)
R8	Cathode resistor for V2
CR1, CR2	Part of damping circuit across T2 (with R4, R5, and R6)
C1	Coupling capacitor
C2	Filter capacitor
C3	Output coupling capacitor
T1, T2	Input transformers

tude in a 1:1.5 ratio and delivers it to the grid of pulse amplifier V1. This tube is normally held at cutoff by a —10V bias obtained at the junction of R23 and R24. The positive pulse input allows V1 to conduct and to develop a standard pulse of voltage in the primary winding of output transformer T4. Diode CR1, in the control grid circuit of V1, limits the negative inductive swing of T2 to —10V and prevents ringing.

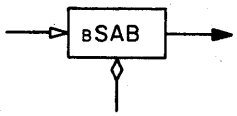


Figure 3–189. Sense Amplifier Blocking Oscillator, Model B, Logic Block Symbol

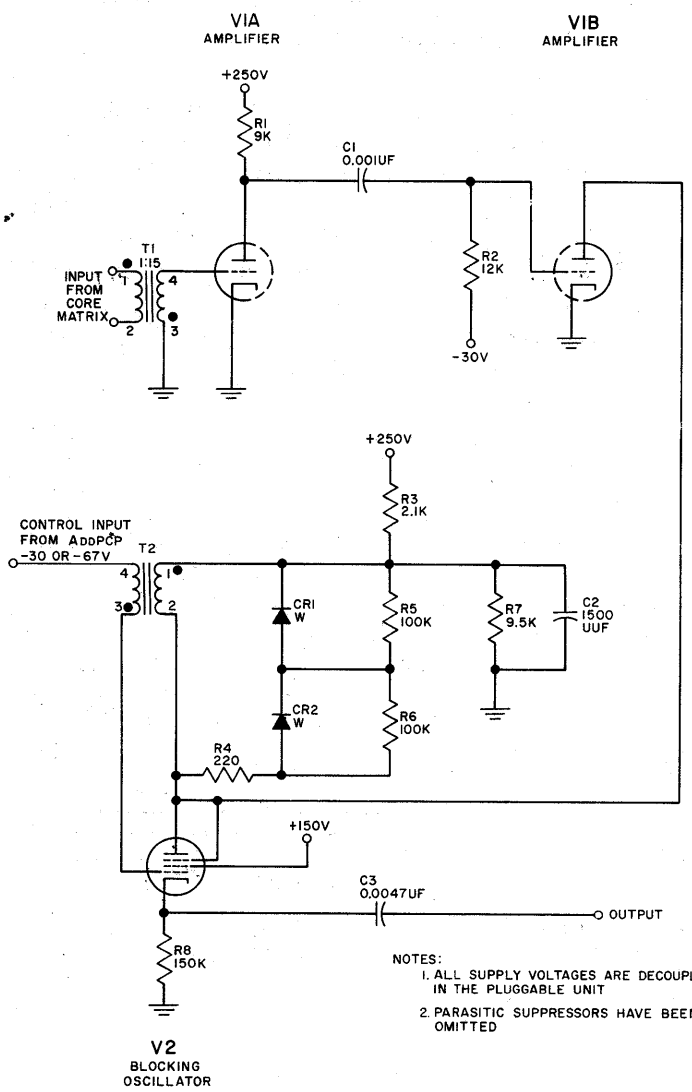
3.74 SENSE-AMPLIFIER BLOCKING OSCILLATOR, MODEL B

3.74.1 Definition and Description

The model B sense-amplifier blocking oscillator (BSAB) is a logic circuit which amplifies the readout pulses developed in the sense windings of the core matrix cores and utilizes these pulses to provide output pulses properly shaped for use in the Central Computer System. The logic block symbol for the BSAB is shown in figure 3–189.

3.74.2 Principles of Operation

Figure 3–190 is the schematic diagram for the BSAB. Table 3–91 lists associated detail parts and their functions. The circuit consists of a 2-stage pulse amplifier (V1A, V1B) followed by a conventional blocking oscillator (V2).



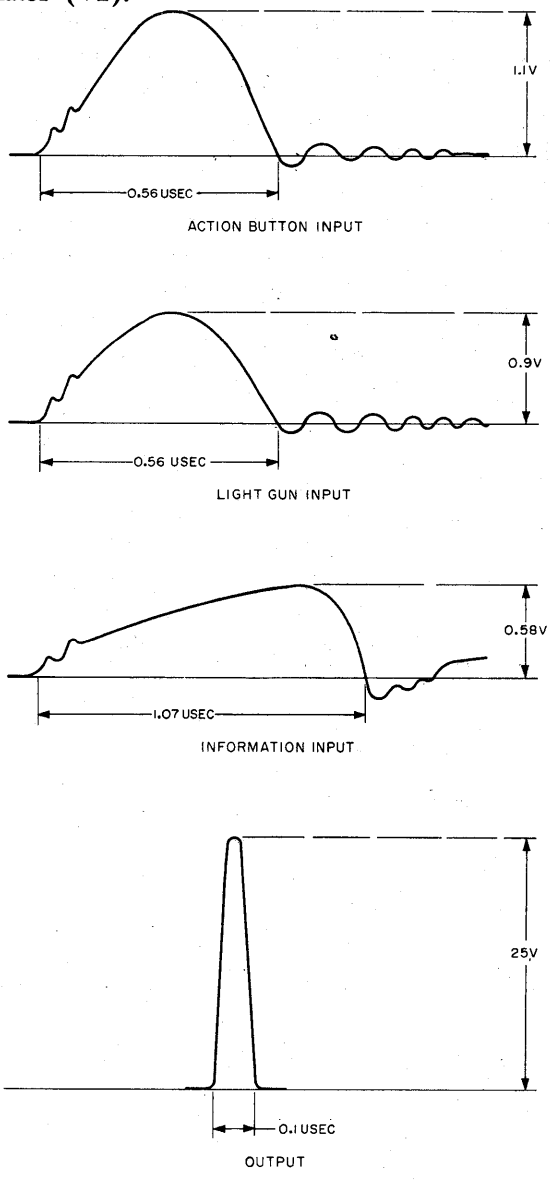


Figure 3–190. Sense Amplifier Blocking Oscillator, Model B, Schematic Diagram

As the contents of the core matrix are driven out register by register, the readout pulse from a particular core is applied to its associated sense amplifier, amplified in two stages, and then used to excite a blocking oscillator.

The BSAB has specified accept and reject levels. An input to the circuit of a 300-mv positive pulse will produce a 0.17-μsec output pulse; an input of 200 mv will yield no output.

Assume that a 300-mv positive pulse is applied to the primary of T1. This pulse is stepped up by a ratio of 1:15 and appears as a negative pulse of 4.5V across the T1 secondary. This negative pulse, in turn, is applied to the grid of V1A. Normally, V1A is conducting. The negative signal produces a positive pulse at the plate of V1A. This pulse is coupled through C1 to the grid of V1B, causing a negative pulse at the plate of this stage and at the plate end of T2 primary (terminal 2). Since the primary of T2 is in the plate circuit of both V1B and V2, the voltage across the primary reflects the action of both these tubes.

A control input voltage stepped at —30V and —67V respectively is applied to the grid of V2 through the secondary of T2. Assume that a negative-going voltage has been applied to terminal 2 of T2. Polarity inversion by the transformer produces a positive-going pulse at terminal 3 which is applied to the grid of V2. This pulse has a peak amplitude of +60V, insufficient to override a bias of —67V; consequently, when the control voltage is down (—67V) the tube remains cut off. However, when the control voltage is up (—30V), the positive 60V pulse causes conduction through the tube. The ensuing current surge through the T2 primary re-enforces the negative-going voltage at terminal 2, which is reflected regeneratively as an increase in the positive voltage applied to the V2 grid. V2 quickly saturates, and current flow through the T2 primary levels off at maximum. Since a transformer can couple only ac, the magnetic field around the secondary of T2 is unsupported. Consequently this magnetic field collapses, producing a voltage approximately equal but opposite in direction to the voltage previously applied to V2 grid. The regenerative action of the blocking oscillator is now in the negative direction, rapidly cutting off V2. This completes the cycle, which is repeated when another negative pulse is supplied by V1B. Meanwhile, the current pulse through V2 has appeared as a corresponding positive voltage pulse across the cathode load of this tube. This pulse, 0.2 μsec wide as determined by the circuit constants, is utilized as the output of the circuit.

3.75 SET DRIVER

3.75.1 Definition and Description

The set driver (STD) is a nonlogic circuit which is used to produce a current pulse to switch tape cores. The logic block symbol for the STD is shown in figure 3–191.

3.75.2 Principles of Operation

The STD shown schematically in figure 3–192 consists of a single pentode tube. Input signals are applied to the suppressor and control grids. Inputs to the suppressor grid are from two sources: (1) The suppressor grid of an STD used for the address axis receives its input from the register address decoder, to determine in which row in the core array the information will be written. (2) The suppressor grid of an STD used for the message axis receives its input from the right drum

Figure 3–191. Set Driver, Logic Block Symbol

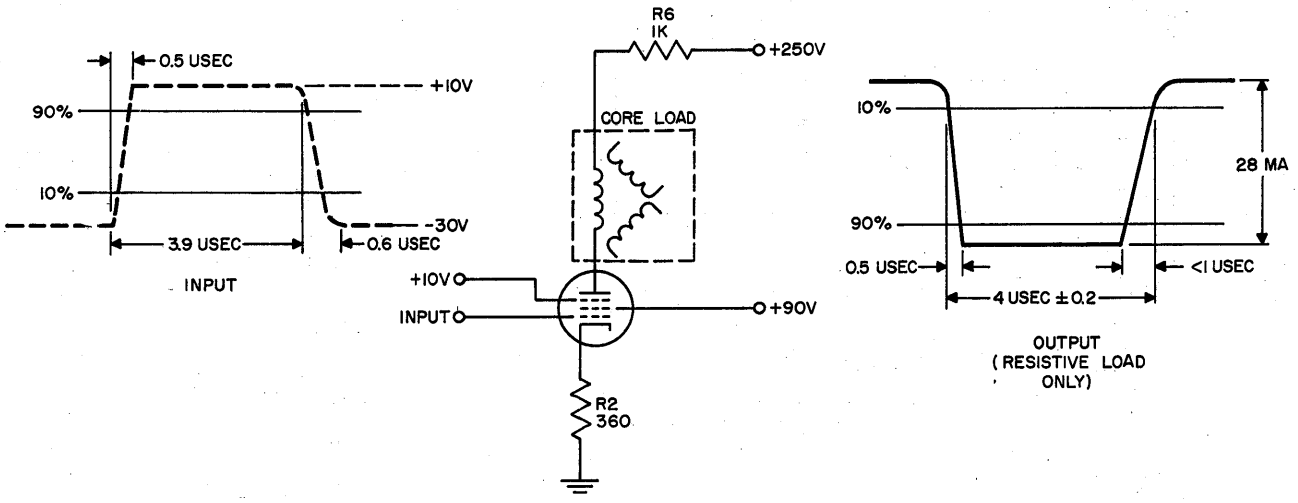


Figure 3–192. Set Driver, Schematic Diagram

word register which contains the intelligence (message column) to be written in the particular row of the core array. Input to the control grid is from the read-in control circuit.

The plate voltage of the STD pentode is obtained from the +250V service voltage supply, and the screen grid voltage from the +90V marginal checking voltage supply. A nominal current of 28 ma flows through the CCD set windings connected in the plate circuit. The tube is maintained at cutoff by the −30V level of a flip-flop circuit that supplies the control grid and by the absence of a positive level on the suppressor grid. The register address decoder or the right drum word register selects a specific row or column and its associated circuitry places a +10V level on the suppressor grid of the selected STD. This signal level (conditioning) is maintained throughout the complete read-in operation (approximately 6 μsec). If the address and parity information is correct and the word is correctly timed, the read-in control circuit, through a flip-flop circuit, places a +10V pulse on the control grid of the selected STD.

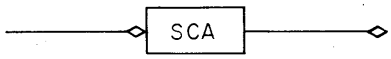


Figure 3–193. Sine-Cosine Approximator, Logic Block Symbol

When the control grid is pulsed, the output of the STD, a nominal output pulse of 28 ma, flows through the set windings of the CCD's connected in the plate circuit.

3.76 SINE-COSINE APPROXIMATOR

3.76.1 Definition and Description

The sine-cosine approximator (SCA) is a nonlogic circuit which converts time-related voltages representing straight line approximations of azimuth sine and cosine functions to a more refined approximation of these functions. The logic block symbol for this circuit is shown in figure 3–193.

In Input System logic, two SCA's are used in the analog section of the LRI monitor. One processes the output of the sine binary decoder after it is fed through the sine buffer amplifier. The other processes the output of the cosine binary decoder after it is fed through the cosine buffer amplifier.

3.76.2 Principles of Operation

3.76.2.1 Basic Operation

Figure 3–194 is the schematic diagram of the SCA. Table 3–92 lists associated detail parts and their functions. The circuit employs six twin triodes, each connected as a diode.

Azimuth information from the buffers occurs as a series of d-c voltage levels corresponding to varying

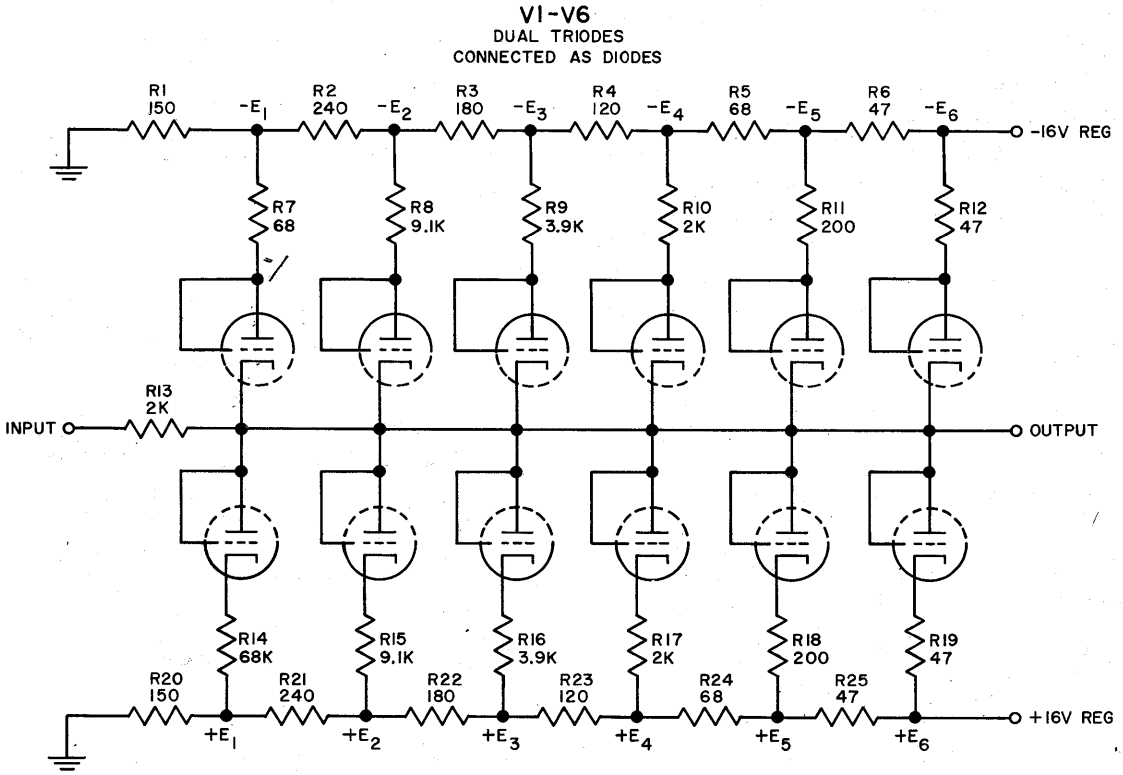


Figure 3–194. Sine-Cosine Approximator, Schematic Diagram

values of θ. The relationship of input to output is shown in figure 3–195. The first approximators of azimuth angle θ functions appear as straight lines (linear inputs), and the second approximations appear as properly formed sine and cosine curves (sinusoidal outputs). Since the voltage range and the manner of treatment are the same for both functions, the two networks are identical and interchangeable.

3.76.2.2 Detailed Operation

As stated above, the SCA employs six twin triodes, each triode section functioning as a diode. Six of the diodes conduct for positive input voltage, and the other six conduct for negative input voltage. The 12 diodes are paired so that one positive and one negative conducting diode in one envelope are affected by a like change in voltage.

Positive bias is obtained from the +16V input and the voltage divider network consisting of R20 through R25; negative bias is obtained from the −16V input and the voltage divider network consisting of R1 through R6. The voltage divider networks are such that V1 responds to changes in the smallest voltage range (corresponding to the bias range between $+E1$ and $+E2$, or $-E1$ and $-E2$), and V6 responds to the largest voltage range.

There is no output for the 0 voltage input because of the cutoff point at V1. Input voltage greater than the bias level at $\pm E2$ causes V2 to conduct; this progression continues until all six stages are conducting when the input voltage is ±25V.

The output of each stage is proportional to the input at that stage, but attenuation is inversely proportional to the input amplitude, and is affected by resistors R14 through R19 for positive input values, and by resistors R7 through R12 for negative input values. The attenuation factor for either positive or negative input voltages is the same for voltages of the same amplitude; it may be computed as illustrated by the following progressive formula:

$$\frac{R13}{R13 + X1} \text{ when input is between } +E1 \text{ and } +E2$$

$$\frac{R13}{R13 + X2} \text{ when input is between } +E2 \text{ and } +E3$$

$$\frac{R13}{R13 + X3} \text{ when input is between } +E3 \text{ and } +E4$$

where $X1 = R14$

$$X2 = \frac{X1R15}{X1 + R15}$$

and $$X3 = \frac{X2R16}{X2 + R16}$$

This nonlinear attenuation in the sine-cosine approximator is calculated to produce a sinusoidal representation of the straight-line approximation input voltage.

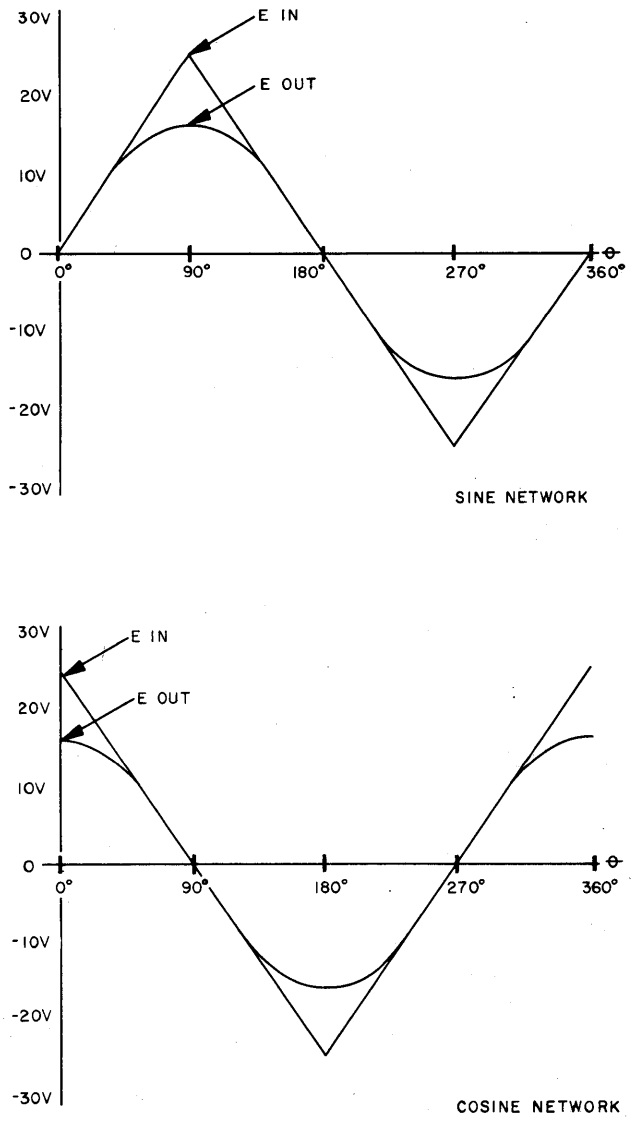


Figure 3–195. Sine-Cosine Approximator Waveforms

TABLE 3–92. SINE-COSINE SHAPING APPROXIMATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1-R6	Voltage divider
R7-R12	Plate load resistors
R13	Input resistor
R14-R19	Cathode resistors
R20-R25	Voltage divider

3.77 SWITCH DRIVER, MODEL A

3.77.1 Definition and Description

The model A switch driver (ASWD) is a logic circuit which provides a nonstandard current pulse. The logic block symbol for the ASWD is shown in figure 3–196.

In Central Computer logic, the ASWD is used to isolate the current regulator pulse source from the back voltage produced by the 16 x 16 tape core matrix of the expanded memory. The ASWD also affords a means of switching the current pulse to difference lines of the tape core matrix, thereby eliminating the need for separate pulse inputs for each line.

3.77.2 Principles of Operation

Figure 3–197 is the schematic diagram of the ASWD. The circuit requires two coincident inputs to produce an output. The input amplifier (par. 3.39) supplies the ASWD with nonstandard levels of −150V and −240V; the other input is a nonstandard current pulse from the current regulator (par. 3.22). An output is produced only if a ASWD is conditioned by the upper −150V level from its associated input amplifier and, at the same time, is supplied with a driving current from the current regulator.

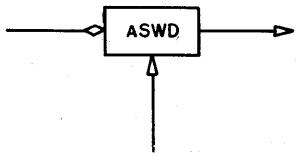


Figure 3–196. Switch Driver, Model A, Logic Block Symbol

3.78 TAPE FLIP-FLOP, MODEL A

3.78.1 Definition and Description

The model A tape flip-flop (ATFF), a logic circuit, is a bistable multivibrator. The logic block symbol for the ATFF is shown in figure 3–198.

In Central Computer logic, the ATFF is used in the character register of the tape element and is set by pulses read from the tapes. One setting of the flip-flop corresponds to a 0 and the other setting to a 1. The contents of the TFF's are transferred to the word register.

3.78.2 Principles of Operation

3.78.2.1 Basic Operation

Figure 3–199 is the schematic diagram of the ATFF. Table 3–93 lists associated detail parts and their functions.

Tubes V1A and V1B have two stable operating conditions. When one is in a state of full conduction, the other is cut off. The plate voltage of each tube has two possible levels: +125V when the tube is cut off, and +50V when the tube is conducting. The circuit is a plate-coupled multivibrator. Positive feedback is taken from the plate of V1B to the grid of V1A by means of net-

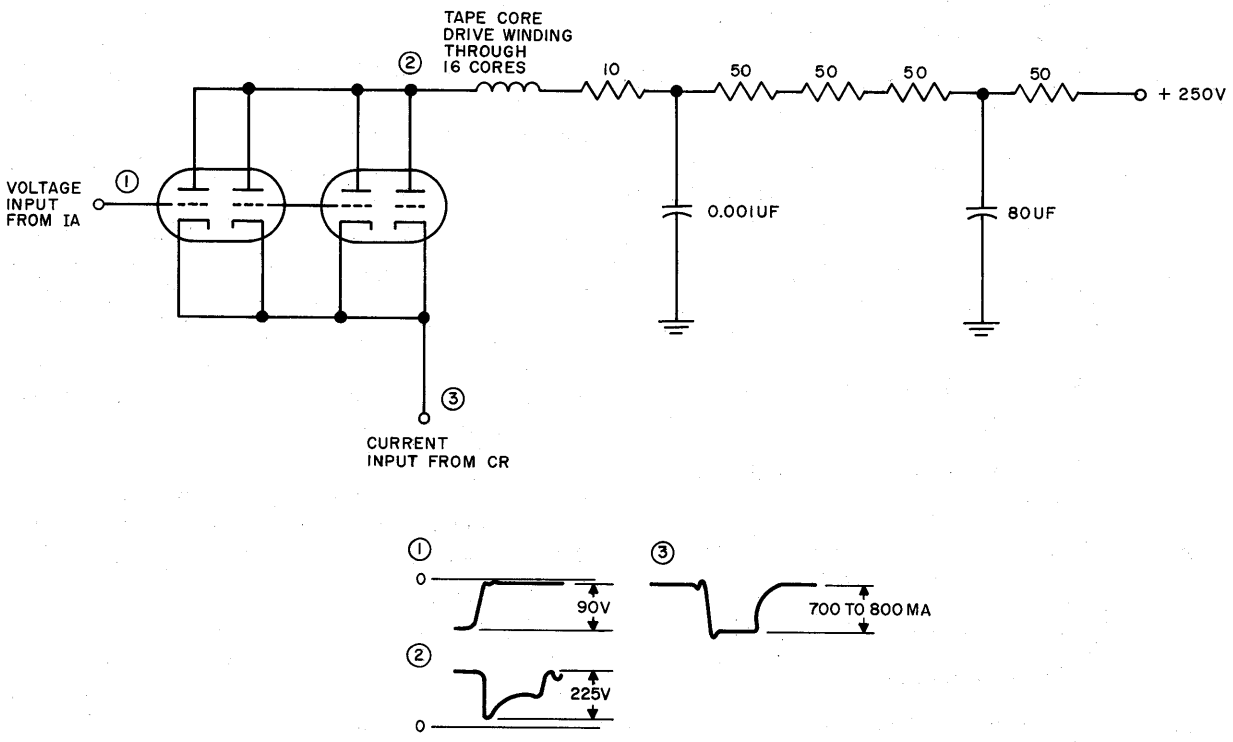


Figure 3–197. Switch Driver, Model A, Schematic Diagram

work R5, and R9. Positive feedback is taken from the plate of V1A to the grid of V1B by means of network R4 and R10. Capacitors C2 and C4 compensate for the input capacitances of the two tubes, and operate to speed up the transition times.

3.78.2.2 Detailed Operation

The flip-flop is normally in the cleared condition. In this state, tube V1A is conducting, and the tube V1B is cut off. The plate voltage of V1A is at +50V. This voltage is applied to the grid of V1B through voltage divider R4 and R10, and causes a voltage of about −12V at the grid. This keeps V1B cut off. There are identical voltage divider networks in the plate circuits of both tubes. When the plate of V1A is at +50V, this voltage, applied to voltage divider R2 and R3, results in a voltage of about −30V at the junction of R2 and R3. This is the output of tube V1A, and it indicates that the flip-flop is in the cleared state. Since V1B is cut off, its plate voltage is approximately +125V. This voltage, applied to voltage divider R7 and R8, results in a level of about +10V at the junction of the voltage divider. This is the output of V1B when the flip-flop is in the cleared condition.

TABLE 3–93. TAPE FLIP-FLOP, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2, R3	Voltage divider between +140V and −130V in V1A plate circuit
R4	Part of voltage divider feedback network between −130V supply, V1B grid, and V1A plate (with R10)
R5	Part of voltage divider feedback network between −130V supply, V1A grid, and V1B plate (with R9)
R6, R7, R8	Voltage divider between +140V and −130V in V1B plate circuit
R9	Part of voltage divider feedback network between −130V supply, V1A grid, and V1B plate (with R5)
R10	Voltage divider feedback network between −130V supply, V1B grid, and V1A plate circuit (with R4)
R11	Part of V1B input coupling network (with C5)
CR1, CR3	Clip positive excursion of input voltage
CR2, CR4	Clip negative part of input pulses beyond −12V
C1, C3	Compensating capacitors
C2, C4	Commutating capacitors
C5	V1B input coupling capacitor
L1, L2	Peaking coils

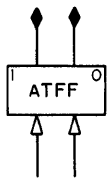


Figure 3–198. Tape Flip-Flop, Model A, Logic Block Symbol

The input to the circuit, as applied to the grid of V1A, consists of negative pulses of about 12V in amplitude. These pulses set the flip-flop. The negative pulses applied to the grid of V1B through C5 and CR3 clear the flip-flop. Diodes CR1 and CR3 in the input circuit of V1A and V1B function to clip off any part of the input pulses that are positive. Diodes CR2 and CR4 clip off any part of these pulses that is more negative than −12V. Thus, the setting and clearing pulses are cut down to proper amplitudes.

When the setting pulse appears at the grid of V1A, its amplitude of −12V is sufficient to cut off V1A. The plate voltage then increases to its cutoff value of +125V and the output of V1A, taken at the junction of R2 and R3, increases to about +10V. The plate of V1A is coupled to the grid of V1B through voltage divider R4 and R10. When the plate voltage rises to its upper level of +125V, it causes the grid of V1B to rise to about 0 volts. This causes tube V1B, which was previously not conducting, to come into a state of full conduction. When this happens, the plate of V1B goes from its cutoff value of +125V to its lower level of +50V. This plate is coupled to the grid of V1A through divider network R5 and R9 and results in a voltage of −12V on the grid of V1A. The circuit condition caused by the setting pulse is thereby maintained because the voltage level on the grid of V1A which was initiated by the pulse is now maintained by the circuit in its stable condition. The output of V1B, taken at the junction of R7 and R8, is now at the −30V level.

The flip-flop is now in its set condition. It may be cleared (or reset) by a negative pulse applied to the grid of V1B. The action which takes place when a clearing pulse is applied to the flip-flop is the exact reverse of what happens when the flop-flop is set. In this case V1B is cut off, and V1A conducts.

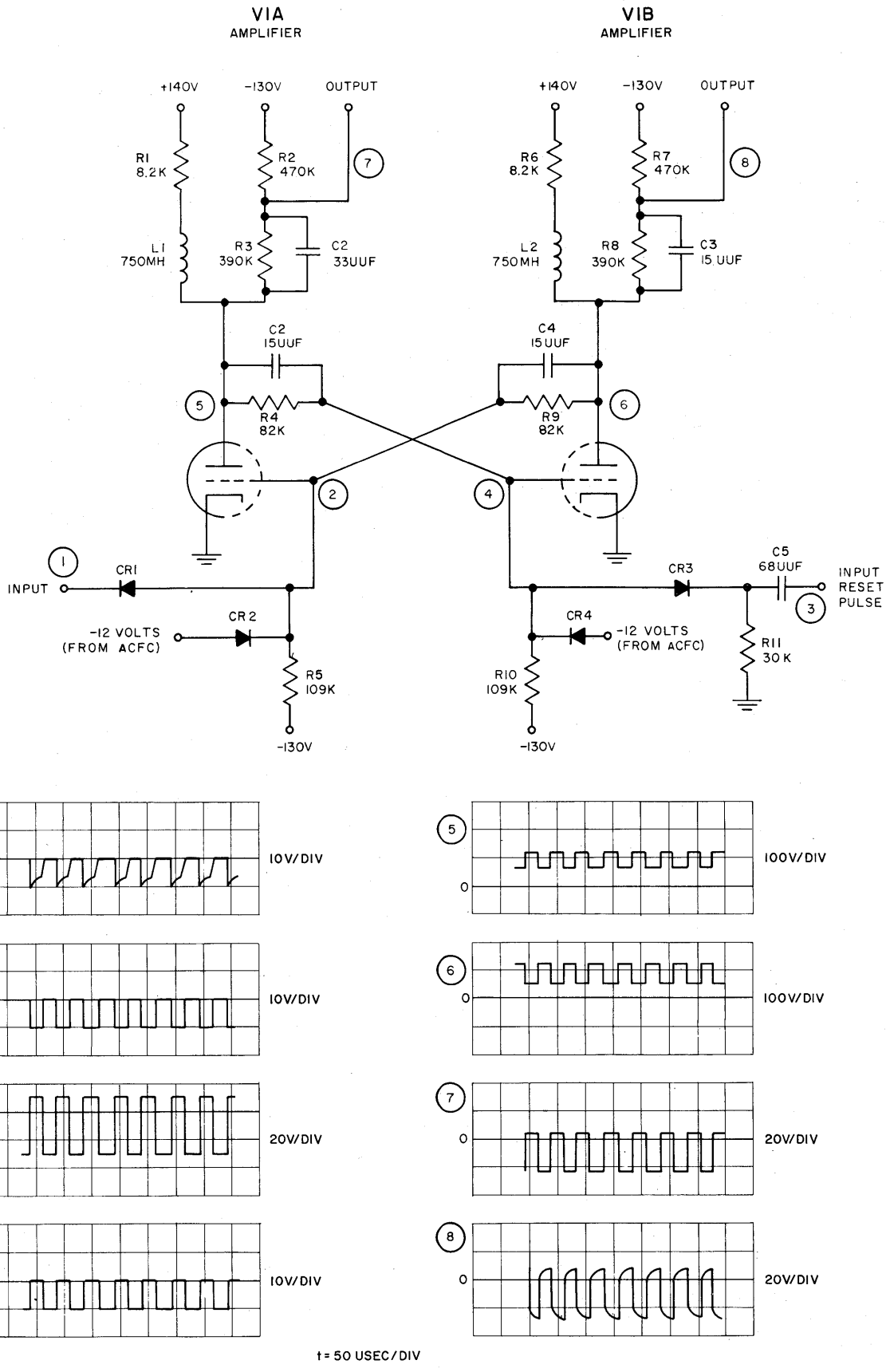


Figure 3-199. Tape Flip-Flop, Model A, Schematic Diagram

3.79 TAPE INVERTER, MODEL M

3.79.1 Definition and Description

The model M tape inverter (MTI) is a nonlogic circuit which amplifies and inverts the write echo pulses from the tape and feeds them to a negative OR circuit (paragraph 3–57). The logic block symbol for the MTI is shown in figure 3–200.

3.79.2 Principles of Operation

Figure 3–201 is the schematic diagram of the MTI. The circuit consists of a 1-stage pulse amplifier.

The MTI is maintained in a nonconducting state by an externally supplied negative d-c level applied to the grid of V1 through resistor R1. The voltage at the plate of V1 is +140V in this condition. When a write echo pulse (about 30V in amplitude) is applied to the input, V1 goes into conduction and the plate voltage decreases to about +75V. The output of V1, taken from the plate is then fed to part of the negative OR circuit. The short time constant of network C2 and R3 results in peaking of the waveform. C1 and L1 improve the transition time of the circuit.

Figure 3–200. Tape Inverter, Model M, Logic Block Symbol

3.80 THYRATRON CORE DRIVERS

3.80.1 Definition and Description

A thyratron core driver (TCD) is a logic circuit which produces a peaked current waveform utilized to drive out the contents of a core register. There are three models of the TCD utilized in AN/FSQ-7 and -8 equipments. The basic difference between models A and B is in the number of cores driven by each. Model C is essentially the same as A and B, except that it is gated.

Model C is used when two ferrite core arrays are required. The gated TCD permits one array to be read

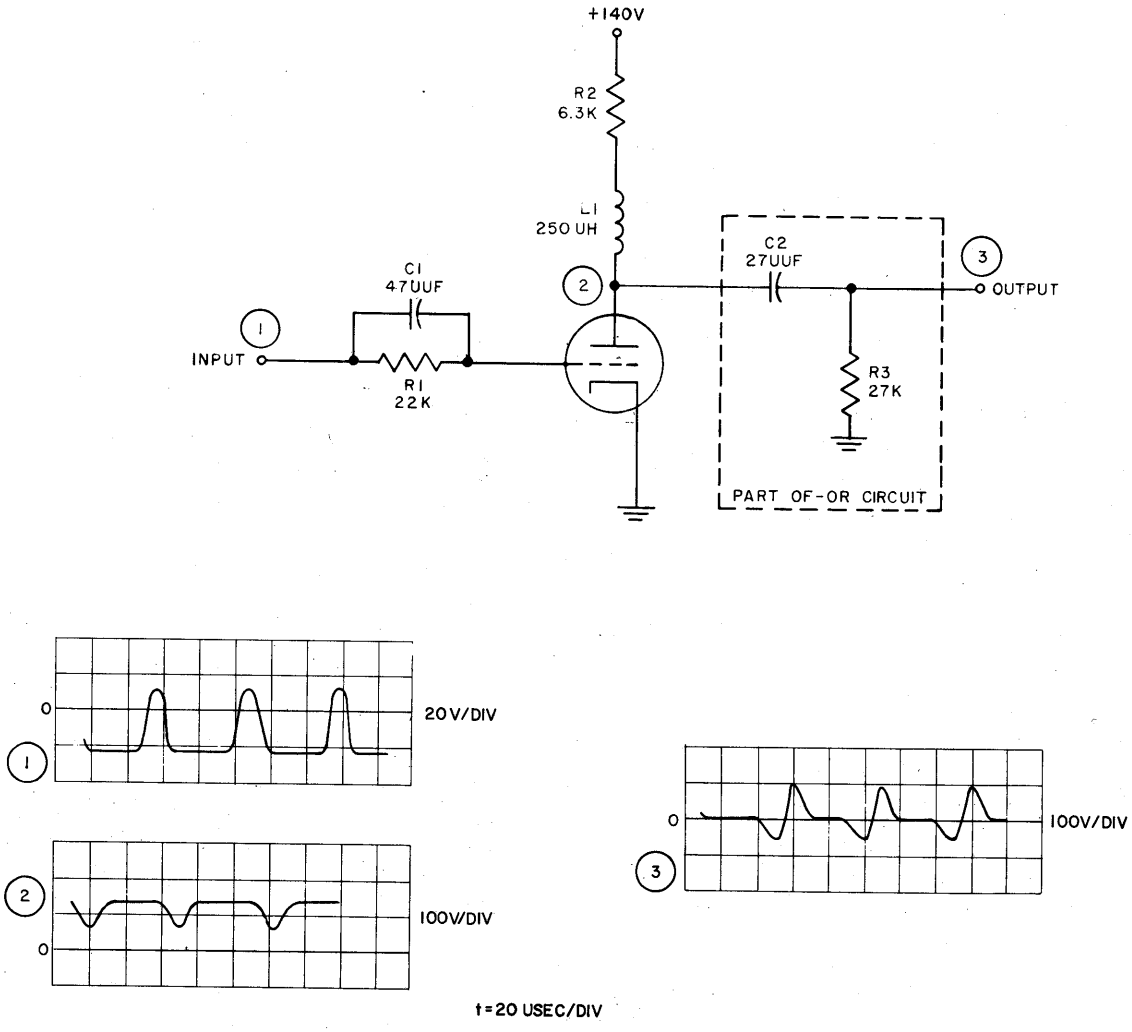


Figure 3–201. Tape Inverter, Model M, Schematic Diagram

out while the other array is prevented from delivering information in cases where the input voltage controlling both readouts comes from a single source.

Since all models of the TCD operate basically the same, only the ATCD is discussed in detail. Figure 3–202 contains the logic block symbols of the three TCD's.

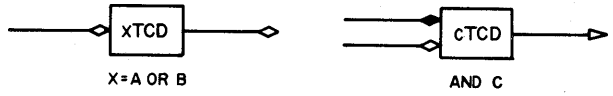


Figure 3–202. Thyratron Core Drivers, Models A, B, and C, Logic Block Symbols

3.80.2 Principles of Operation

Figure 3–203 is the schematic diagram for the ATCD. Table 3–94 lists associated detail parts and their functions. The circuit consists of a tetrode thyratron and its associated circuits.

The grid of the thyratron is biased at approximately −12V established by voltage divider R2 and R4 between −15V and ground. This bias is sufficient to cut off the tube. The input signal, which is 40V to 60V positive, overcomes this bias, triggering the tube. Since the internal resistance of an ionized thyratron is negligible, plate voltage drops from +250V to almost zero. Capacitor C3, originally charged to the +250V supply, now discharges through the driver load consisting of 33 core windings, setting all cores to the 0 state and producing a sense output from those cores that were in the 1 state. The low plate voltage now present at the thyratron is insufficient to maintain current flow through the tube and, as a result, the thyratron deionizes and returns to cutoff. Capacitor C3 again begins to charge through R5 toward the +250V supply, terminating the current flow through the core drive windings.

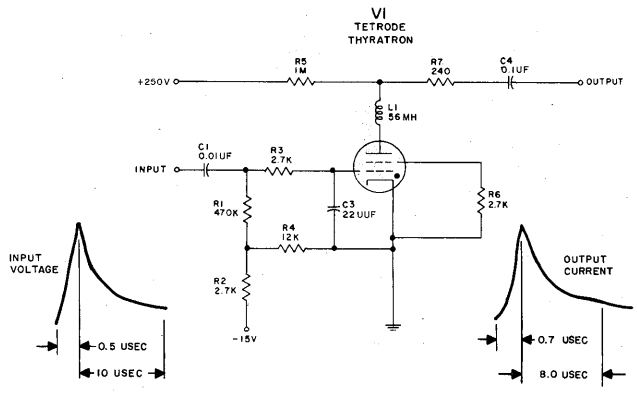


Figure 3–203. Thyratron Core Driver, Model A, Schematic Diagram

TABLE 3–94. THYRATRON CORE DRIVER, MODEL A, FUNCTION OF DETAILED PARTS

REFERENCE SYMBOL	FUNCTION
R1	Forms part of input pulse-shaping network (with C2).
R2	Forms part of voltage divider network (with R4)
R3	Grid current-limiting resistor
R4	Part of voltage divider (with R2)
R5	Serves as high resistance source which produces voltage drop necessary to cut off V1.
R6	Screen grid return
C1	Input coupling capacitor
C2	Forms part of input pulse-shaping network (with R1)
C3	Provides output current when discharged
L1	Limits surge voltages when V1 fires or deionizes.

3.81 THYRATRON RELAY DRIVER, MODEL D

3.81.1 Definition and Description

The model D thyratron relay driver (DRYD) is a nonlogic circuit designed to energize three relays which control the operation of the north-synchonizing circuit. The logic block symbol for the DRYD is shown in figure 3–204.

3.81.2 Principles of Operation

3.81.2.1 Basic Operation

The DRYD, shown in schematic form in figure 3–205 consists of two thyratrons, three relay coils, a north cam reset switch and associated components. Table 3–95 lists associated detail parts and their functions.

The circuit is energized only while the 15-degree sector cam of the north cam synchronizer switch completes the plate return circuit. There are two thyratron channels available in this circuit, one is triggered by the yoke-north pulse, and the other by the north-radar pulse. The presence of either or both of these pulses determines, through external circuitry, the application of the normal-speed, double-speed, or stop brakes which control the rotation speed of the yoke.

3.81.2.2 Detailed Operation

The following description is made on the assumption that the 15-degree sector cam of the north cam synchronizer is making the circuit operative through application of plate voltage. The yoke-north pulse fires thyratron V1, causing current flow through the K1 relay coil located in the plate circuit of this tube. Relay K1 is

Figure 3–204. Thyratron Relay Driver, Model D, Logic Block Symbol

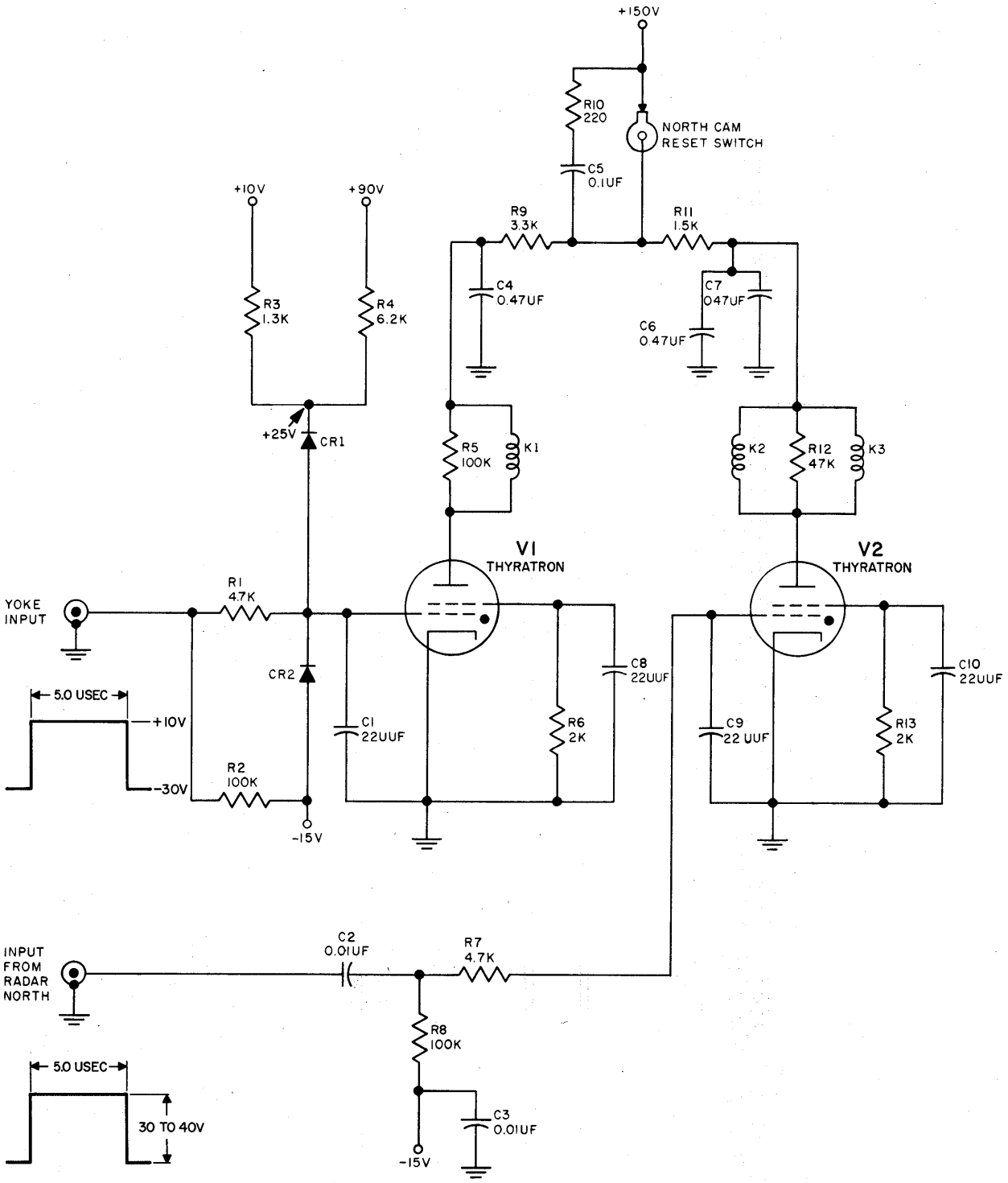


Figure 3–205. Thyratron Relay Driver, Model D, Schematic Diagram

thereby energized. The radar-north pulse causes similar action in thyratron V2, energizing relays K2 and K3.

When the yoke-north and radar-north pulses are coincident, relays K1, K2, and K3 are energized. In this condition, the —150V power supply to K4 is switched from opening contacts 4-5 of K1 to closing contacts 1-2 of K3. Relay K4 is thereby maintained energized, closing its contacts 3-1 and removing the +48V power supply to the stop brake. The model B Miller integrator (BMI) is maintained quiescent as contacts 1-2 of K1 are closed and contacts 4-5 of K3 are opened, removing the ground from the BMI output; however, no output will be obtained from a quiescent BMI. With no output from the BMI, the model E vacuum tube relay driver (EVRD) will maintain K5 energized and, through its contacts 2-3, the normal-speed brake is energized. (Relay K4 is also energized as previously established.) The yoke then rotates at its normal speed as a result of yoke-north and radar-north pulse coincidence.

When the yoke-north pulse leads the radar-north pulse, K1 is energized and K2 and K3 remain de-energized. In this condition, opening contacts 4-5 of K1 remove the —150V power supply to K4, through whose contacts 3-5 the +48V power supply is connected to the stop brake. Yoke rotation is thereby stopped until the radar-north pulse appears and coincidence is established.

When the radar-north pulse leads the yoke-north pulse, K1 is maintained de-energized and K2 and K3 are energized. Ground is removed from the BMI output by opening contacts 4-5 of K2. With open contacts 1-2 of K1 and 4-5 of K3, the BMI starts producing a negative-going triangular output. Relay driver EVRD is cut off and K5 is thereby de-energized. Since K4 is maintained energized through contacts 4-5 of K1, the —48V power supply is applied to the double-speed brake through contacts 1-3 of K4 and contacts 3-5 of K5.

TABLE 3–95. THYRATRON RELAY DRIVER, MODEL D, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	V1 grid current limiter
R2	Grid return to —15V source
R3, R4	Form voltage divider network which maintains cathode of CR1 at +25V
R5	Load resistor for coil of K1
R6	Screen grid return
R7	V2 grid current limiter
R8	V2 grid return to —15V source
R9	Part of V1 plate decoupling network (with C4)
R10	Part of network which suppresses transients on +150V line (with C5)
R11	Part of V2 plate decoupling network (with C6, C7)
R12	Serves as load to coils of K2 and K3
R13	V2 screen grid return
C1	Filter capacitor
C2	Coupling capacitor
C3	Filter capacitor
C4	Part of V1 plate decoupling network (with R9)
C5	Part of network which suppresses transients on +150V line (with R10)
C6, C7	Part of V2 plate decoupling network (with R11)
C8, C9, C10	Noise transient filters
CR1	Clamps upper limit of yoke-north pulse at +25V
CR2	Clamps lower limit of yoke-north pulse at —15V
K1, K2, K3	Relay coils

3.82 TIMING PULSE GENERATOR

3.82.1 Definition and Description

The timing pulse generator (TPG) is a logic circuit that produces two standard pulses 5 μsec apart as a function of a 100-kc sine wave input. Figure 3–206 is the logic block symbol of the TPG.

In Drum System logic, timing pulses are obtained from a timing channel on each drum. This timing channel consists of 2,048 or 2,060 magnetized areas (bits) evenly spaced around the drum. Associated with each drum, one TPG is used to write bits into this channel, another is used to generate timing pulses from voltages developed by reading bits out of this channel.

3.82.2 Principles of Operation

3.82.2.1 Basic Operation

Figure 3–207 is the block diagram for the TPG. Timing signals (100-kc sine wave) from the optical

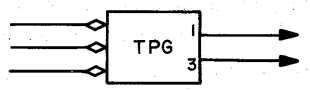


Figure 3–206. Timing Pulse Generator, Logic Block Symbol

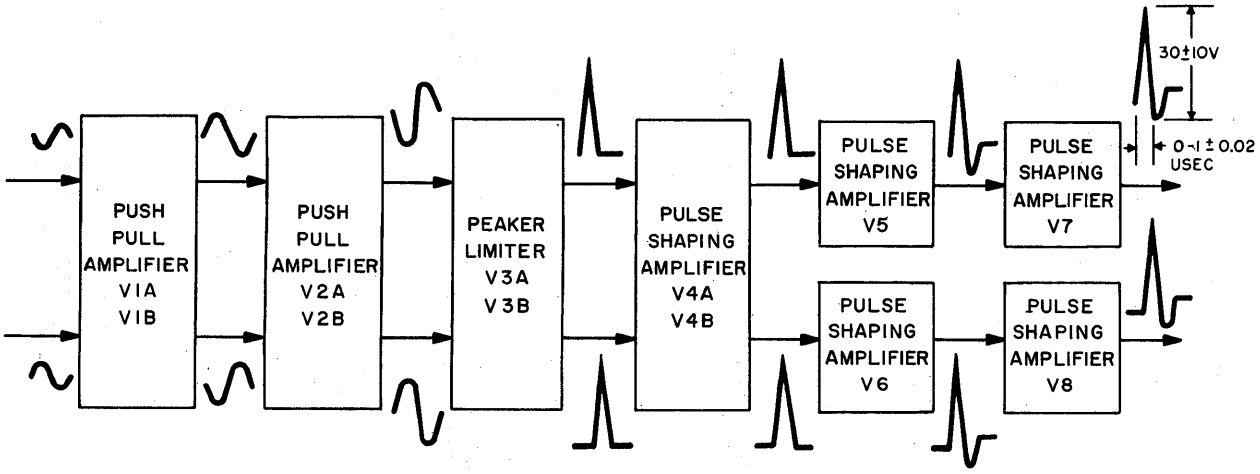


Figure 3–207. Timing Pulse Generator, Block Diagram

frequency generator or a drum-timing channel read head are amplified by two stages of push-pull amplifiers. The amplified signals are applied to peaker limiters V3A and V3B which convert the 100-kc input signal into two 0.5-μsec positive pulses 5.0 μsec apart. The pulses are generated at the negative-going crossover of each V3 input signal. Since these inputs are 180 degrees out of phase, the negative-going crossovers are one-half cycle apart. In a 100-kc sine wave this interval is equal to 5.0 μsec. Three successive stages of pulse-shaping amplifiers convert each pulse into a standard pulse. The earlier output pulse (V6A output) is labeled drum-timing pulse 1; the later output pulse (V6B output) is labeled drum-timing pulse 3.

3.82.2.2 Detailed Operation

Figure 3–208 is the schematic diagram of the TPG. Table 3–96 lists detail parts and their functions. Only one of the two identical channels producing standard pulses is shown completely. However, waveforms at all stages in each channel are shown. The input to T1 is a sine wave (100 kc) from either the optical frequency generator or a timing channel read head. When the TPG is being used for writing, the signal is applied to terminal A and terminal B is grounded. When the TPG is being used in reading, the signal from the read head is applied to terminals A and B and the center tap is grounded. In either instance, when a signal is impressed across the input winding, two signals 180 degrees out of phase are developed at the secondary terminals of T1 and applied to the grids of V1A and V1B. With no input signals, the grids of V1 are at ground potential, the cathodes are at +2V, and the plates are at +210V. Point A, to which V1A and V1B are connected, is maintained at +240V by decoupling network R2 and C1.

TABLE 3–96. TIMING PULSE GENERATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Decoupling network (with R2)
C2	Coupling capacitor
C3	Cathode bypass capacitor for V1
C4	Coupling capacitor
C5	Cathode bypass capacitor for V2
C6	Coupling capacitor
C7	Cathode bypass capacitor for V3
CR1, CR2	Damping diodes
R1	V1A grid return
R2	Decoupling network (with C1)
R3	V1A plate load resistor
R4	V1B cathode resistor
R5	V2A grid return
R6	V2A plate load resistor
R7	V2A cathode resistor
R8	V3A grid return
R9	V3A cathode resistor
R10	Current-limiting resistor for CR1
R11, R12	Bias-setting voltage divider
R13	Damping resistor
T1	Input stepup transformer
T2, T3, and T4	Pulse-shaping transformers

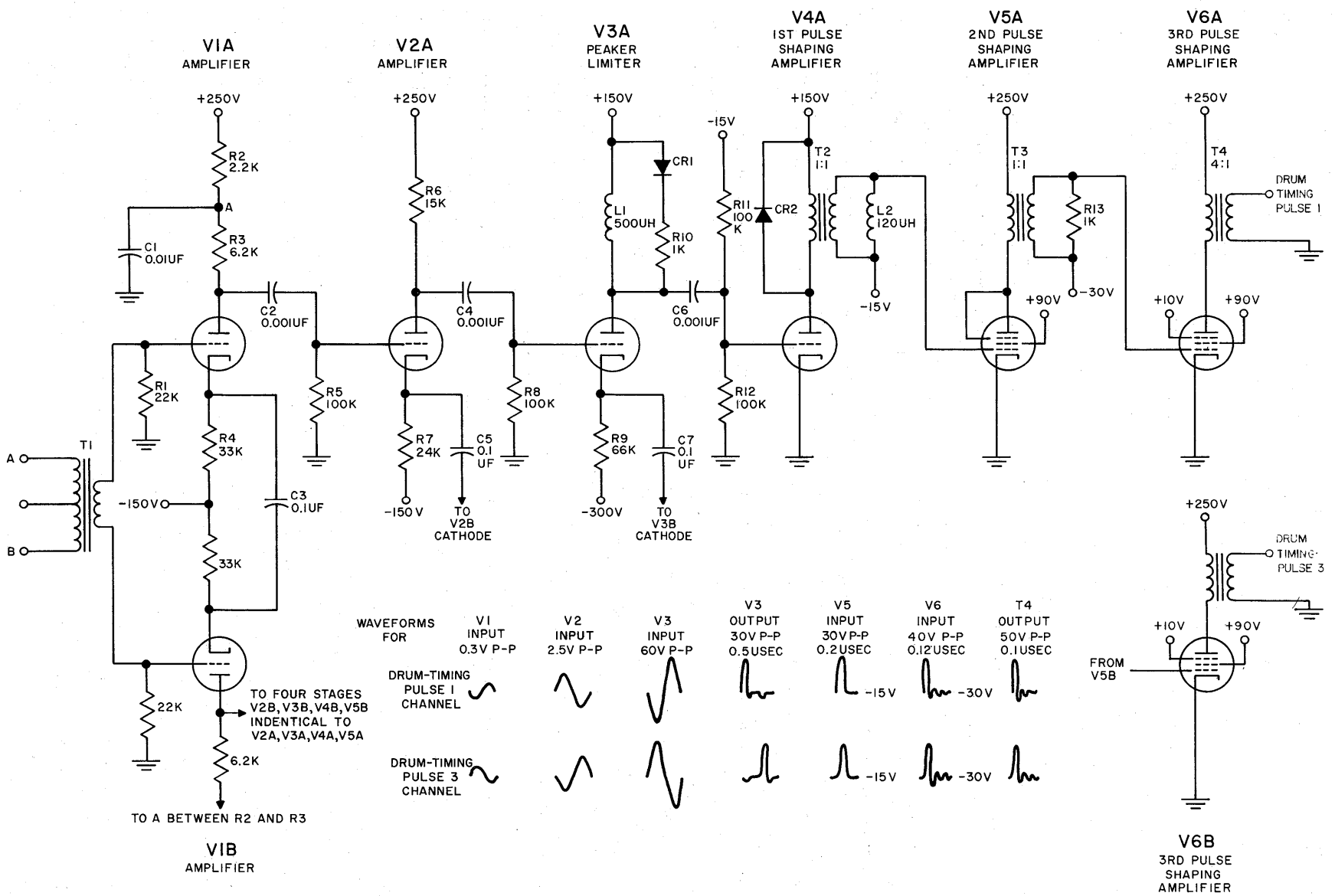


Figure 3–208. Timing Pulse Generator, Schematic Diagram

Amplifier V1 is a conventional class A push-pull amplifier except for the cathode circuit. Capacitor C3 and resistor R4 form a biasing network that permits individual tube sections to establish separate operating points when made necessary by tube variations created in fabrication or aging. In addition, C3 ensures circuit operation even if the input signal to either channel is missing. Assume the input signal to V1B is absent. The signal on the grid of V1A appears at the cathode of V1A and is coupled to the cathode of V1B by C3. Tube V1B then operates as a grounded grid amplifier and the effect is the same as if the missing signal were present. Tubes V1 and V2 amplify the input signal (0.3V peak to peak) by 8 and 25, respectively. The outputs of V2A and V2B are RC-coupled to peaker limit stage V3A and V3B.

The third stage derives its functional name from the plate circuit configuration. Induction L1 performs the peaking function and diode CR1 and resistor R10 perform the limiting function. The magnitude of voltage developed across L1 is a function of the rate of change of current through L1. The rate of change of current through L1 is a function of the rate of change of voltage on the grid of V3A. The maximum rate of change of V3A grid voltage occurs at the zero crossovers of the input signal. Diode CR1 permits only positive pulses to be generated at the plate of V3A. Since this occurs whenever the tube is driven to cutoff, the negative-going crossover of input voltage to V3A produces a corresponding output pulse. The positive-going crossover of input voltage causes CR1 to conduct, and the amplitude of negative pulses in the plate circuit is limited to the voltage drop across R10.

The 60V input signal to V3 appears as a square wave to the tube. The waveform in figure 3–208 shows the 30V positive pulse generated during the fall of V3 input voltage and the small negative pip generated during the rise of V3 input voltage.

The signal output of V3A is coupled to the first pulse-shaping amplifier V4A through C6. Amplifier V4A is normally cut off by the —7.5V bias applied through voltage divider R11 and R12. With the application of a positive pulse to the grid, capacitor C6 is charged by V4A grid current from 157V to 180V. When V4A is cut off, this charge remains on the capacitor biasing V4A by 30V. Thereafter input pulses raise the grid to ground potential only and V4A conducts during a small portion of input voltage; i.e., the peak 4V or 5V. The resultant rapid change of plate current excites L2 into oscillation. However diode CR2 shorts positive plate overshoots to B+ and damps LS oscillation. The output pulse of V4A, 0.2 μsec in duration, is inverted by T2 and applied to V5A. Amplifier V5A operates in a manner similar to V4A except that resistor R13 damps T3 oscillations. The —15V bias on the grid of V5A reduces the effective amplitude of input voltage to approximately 20V. As a result a 70V pulse of 0.12-μsec duration is produced and applied to third pulse-shaping amplifier V6A. The —30V bias on V6A prevents noise and ringing of previous stages from producing an output. In addition, the bias effectively reduces the conduction time of V6A and ensures the production of a standard pulse. Transformer T4 is connected to produce a positive output pulse when the input to V6A is a positive pulse. Stages V1B through V6B operates exactly as do their counterparts V1A through V6A. The output of V6B is a standard pulse occurring 5.0 μsec after the output of V6A.

3.83 TUNING FORK OSCILLATOR

3.83.1 Definition and Description

A tuning fork oscillator (TFO) is a nonlogic circuit which generates continuous sine waves.

Table 3–97 lists the three models of the TFO's utilized in AN/FSQ-7 and -8 equipments. Each circuit is listed by logic symbol showing the characteristics which distinguish one model from the other. Since all three models operate identically, only model B is discussed in detail.

3.83.2 Principles of Operation

The model BTFO, shown in schematic form in figure 3–209, will be discussed as a typical TFO circuit in the following discussion. Table 3–98 lists associated detail parts and their functions.

TABLE 3–97. TUNING FORK OSCILLATORS, MODEL-DISTINGUISHING CHARACTERISTICS

MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A	ATFO	Generates sine wave at a frequency of either 512 or 364 cps, depending on application. Amplitude 45V peak to peak.
B	BTFO	Generates continuous sine wave of 1,300 cps with normal amplitude of 7 to 8V peak to peak.
C	CTFO	Generates sine wave at a frequency of 1,300 cps or 1600 cps, depending on tuning fork used. Amplitude: 11V peak to peak.

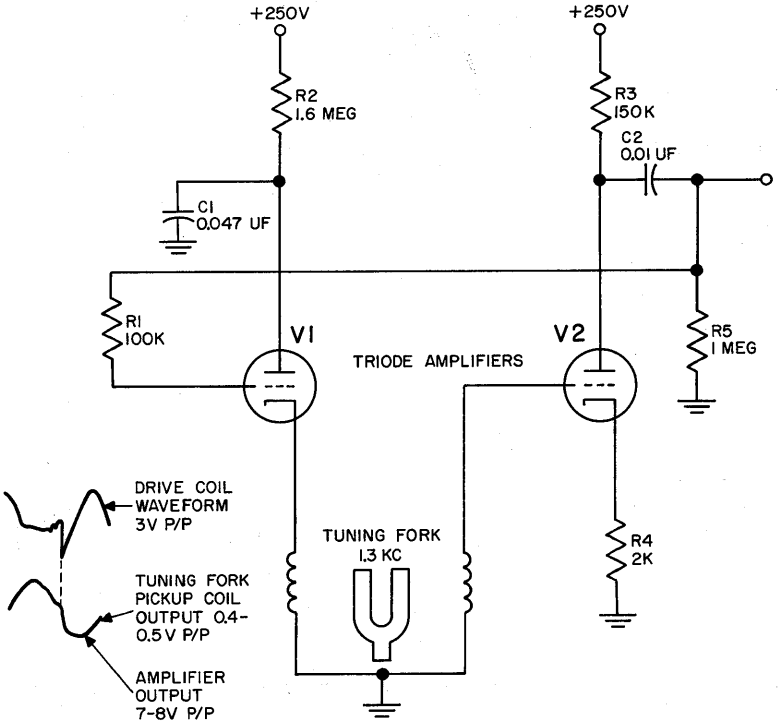


Figure 3–209. Tuning Fork Oscillator, Model B, Schematic Diagram

The BTFO produces a continuous 1300-cps sine wave whose period is extremely stable and accurate. The output from the tuning fork is a 0.5V peak-to-peak sine wave which is applied to the grid of V2. This signal is amplified and fed to V1. The output signal from V1 is a positive 3V feedback of proper phase and magnitude to maintain oscillation of the tuning fork.

TABLE 3–98. TUNING FORK OSCILLATOR, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	V1 grid return
R2	Plate load resistor for V1
R3	V2 plate load resistor
R4	V2 cathode resistor
R5	Part of feedback network (with C2)
C1	Bypass capacitor
C2	Part of feedback network (with R5)

3.84 VARIABLE GATE AMPLIFIERS

3.84.1 Definition and Description

The variable gate amplifiers (VGA's) are nonlogic circuits which provide defocus and intensification gate voltages to the SD and DD CRT's. There are three models of VGA's utilized in the AN/FSQ-7 and -8 equipments. Table 3–99 lists the logic block symbols, functions, and differentiating characteristics of each model.

3.84.2 Principles of Operation

3.84.2.1 Basic Operation

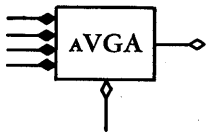
Figure 3–210 is a block diagram containing the basic elements of a variable gate amplifier: a triode, a tetrode-connected pentode, and an output amplitude control. The triode performs a switching function and the pentode is a gate amplifier.

The triode is maintained beyond cutoff by a −30V level applied to the input. To produce an output gate, a positive level is applied to the input, causing the triode to conduct. The output of the switch triode is fed to the tetrode-connected pentode and amplified. The output amplitude of the VGA is adjusted with the amplitude control potentiometer.

3.84.2.2 Detailed Operation, Models B and C

Since VGA models B and C operate basically in the same manner, only model B is discussed in detail. Model C is discussed in terms of its differences as compared to model B. Figure 3–211 is the schematic diagram of the BVGA. Table 3–100 lists associated detail parts and their functions. The cathode of triode V1 is clamped at ground. With a −30V input, triode V1 is cut off. With V1 cut off, its plate voltage is +124V, determined by the

TABLE 3–99. VARIABLE GATE AMPLIFIERS, MODEL-DISTINGUISHING FEATURES

MODEL	LOGIC BLOCK SYMBOL	LOGIC FUNCTION	MODEL-DISTINGUISHING CIRCUIT CHARACTERISTICS
A		SD intensification gate	1. Four switch tubes 2. Input: Four —30V to 0V gates (25 μsec or 75 μsec) One variable amplitude (50 μsec) 3. Output: Variable amplitude gate 0-110V
B		SD defocus gate	1. One switch tube 2. Input: One —30V to +10V gate (37.5 μsec) 3. Output: Variable amplitude gate 0-310V
C		DD intensification gate	1. One switch tube 2. Input: One —30V to 0V gate (90 μsec) 3. Output: Variable amplitude gate 0-110V

voltage divider consisting of resistors R1, R5, and R6. With +124V at the plate of V1, a 424V potential appears across R5 and R6. A 900V potential appears across voltage divider R8, R7, and R6. The resultant voltage at the grid of V2 is —6.5V; the plate voltage of V2 is +92V.

To produce a defocus gate, a positive standard level (+10V) is applied to the control grid of V1, driving V1 into conduction. The resulting plate current develops a voltage drop across cathode resistor R5. This raises the potential on the cathode of V1 and cuts off diode CR1.

Since cathode resistor R2 is large as compared to plate load resistor R1, the triode is a constant current device. Changes in the input level amplitude result in plate current variations which in turn results in voltage changes across R2. The voltage variations developed across R2 oppose input level changes and maintain the plate current at a relatively constant value. Plate current is relatively independent of input level amplitude variations because of the cathode degeneration described above.

Conduction in V1 results in a decrease in the plate potential of V1, reducing the voltage at the grid of V2.

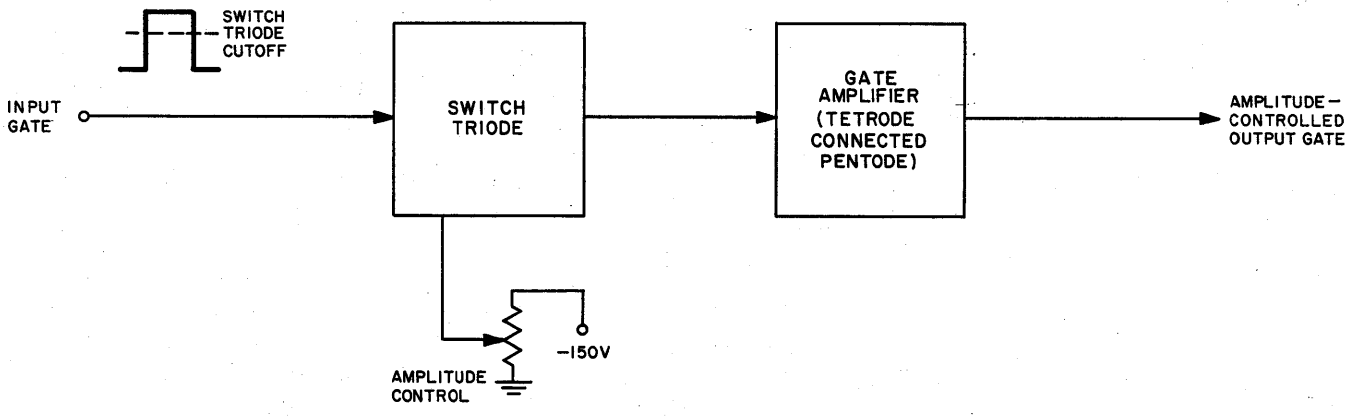


Figure 3–210. Variable Gate Amplifier, Block Diagram

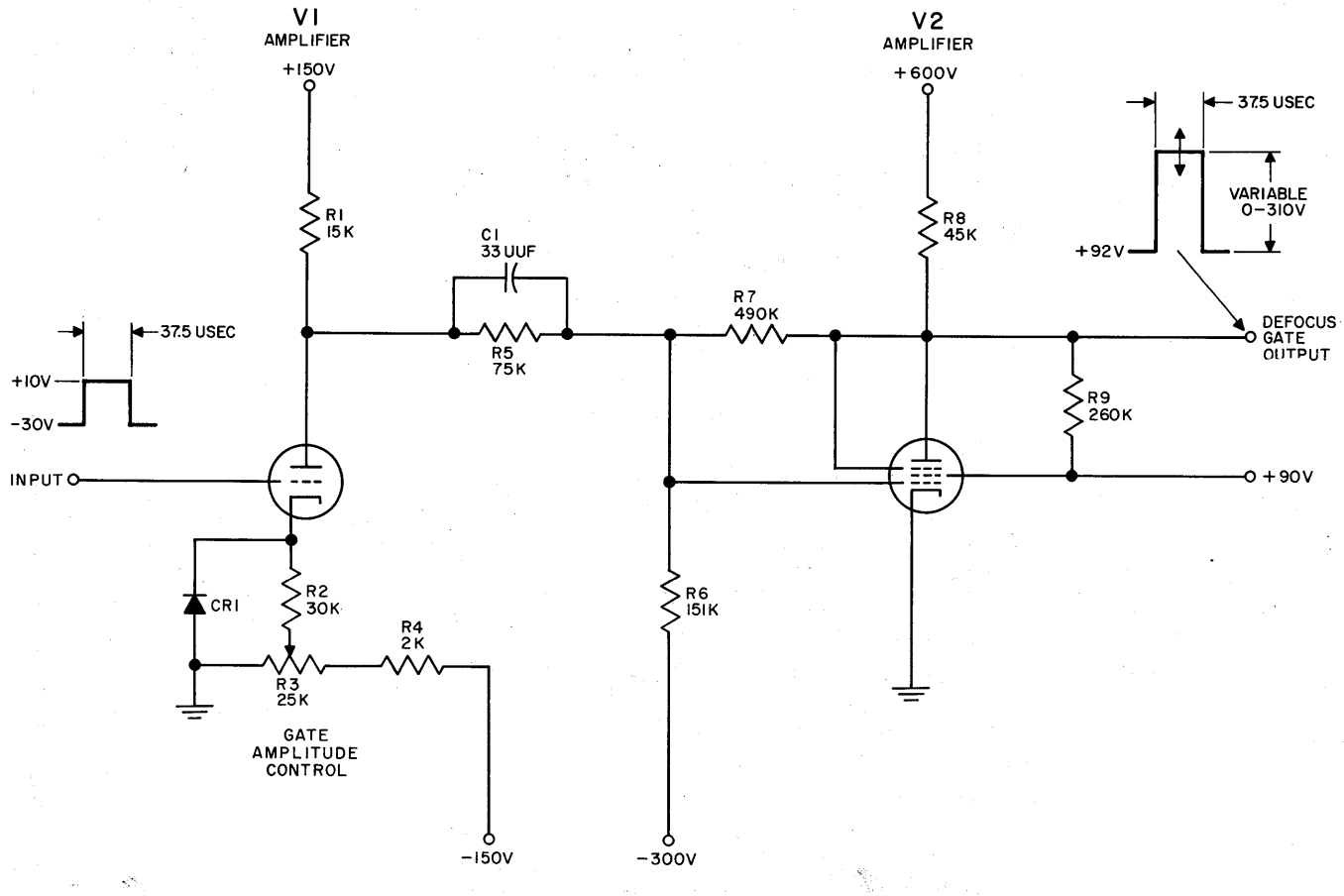


Figure 3–211. Variable Gate Amplifier, Model B, Schematic Diagram

This reduction in grid potential reduces the current through V2 and produces a resultant rise in the plate voltage of V2. D-c coupling from the plate of V2 to the control grid (through R7) introduces degenerative feedback, reducing the effects of voltage variations across R6.

The gate output of the BVGA appears at the plate of V2 and may be varied in amplitude by the setting of potentiometer R3. The setting of R3 determines the magnitude of plate current in V1 (during conduction). This in turn determines the plate voltage of V2 (output level). The output defocus gate is applied to anode 1 of the SD CRT through the SD high-voltage unit.

The circuit operation of the CVGA is similar to that of the model B variable gate amplifier. The CVGA (intensification gate for the DD CRT) generates a smaller output amplitude gate than the BVGA. The essential differences between the two circuits are component values and the plate supply voltage for pentode V2. Another model-distinguishing characteristic (see table 3–99) pertains to the input gate.

3.84.2.3 Detailed Operation, Model A

Figure 3–212 is the schematic diagram of the AVGA. Table 3–101 lists associated detail parts and their functions.

TABLE 3–100. VARIABLE GATE AMPLIFIER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Speedup capacitor, improves rise and fall time
CR1	Crystal diode, clamps V1 cathode at ground
R1	Plate load resistor for V1; also part of voltage divider (with R5 and R6)
R2	Cathode resistor for V1
R3	Defocus gate amplitude control and voltage divider (with R4)
R4	Part of voltage divider (with R3)
R5, R6	Part of voltage divider (with R1)
R7	Feedback resistor from plate to grid of V2
R8	Plate load resistor for V2 and part of voltage divider (with R9)
R9	Part of voltage divider (with R8)

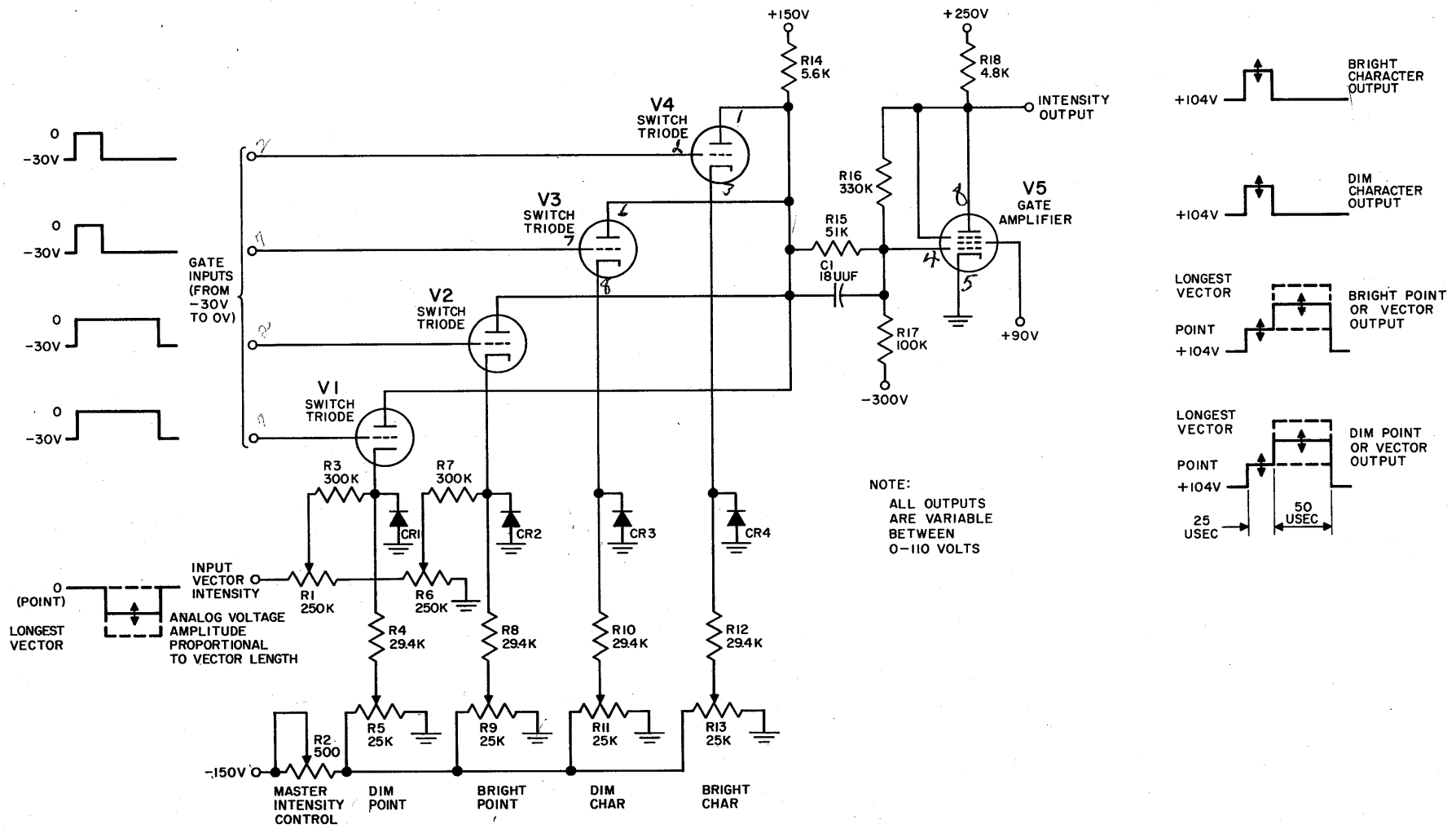


Figure 3–212. Variable Gate Amplifier, Model A, Schematic Diagram

The AVGA provides the SD CRT with an intensification gate. A message may be displayed either bright or dim. Two intensification gate levels are required. However, since a point is chosen with a focused electron beam and characters are selected with the beam defocused, points would be brighter than a character if the same intensification levels were used for both. In order to obtain the same degree of intensity (bright or dim) for both points and characters, the AVGA, with four input channels, is employed. Input selection depends upon whether a bright or dim point or character is displayed. The positive gate applied to an individual input causes the corresponding switch tube to conduct. Except for this selection feature, circuit operation is identical to that of the BVGA. The individual amplitude controls (R5, R9, R11, and R13) permit equalization of all dim and bright displays. Master intensity control R2 permits adjustment of the overall intensity of the display.

Vectors require special compensation because they are generated by a sweeping point over varying distances. If not compensated for, a short vector will appear brighter than a long vector. In order to obtain the same degree of intensification for all vector lengths, a negative gate, the amplitude of which is proportional to vector length, is applied at the cathodes of V1 and V2. A negative voltage applied to a cathode of a tube has the same effect as a positive voltage applied to the control grid. In effect, the grid voltage of V1 or V2, depending on whether a dim or bright vector is required, is increased; this in turn produces an intensity gate output, the amplitude of which is increased. Since the input vector intensity gate amplitude is proportional to vector length, the output is greatest in amplitude for a long vector and least for the shortest vector (a point). Note the associated waveshapes in figure 3–212.

TABLE 3–101. VARIABLE GATE AMPLIFIER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Speedup capacitor, improves rise and fall time
CR1	Crystal diode, clamps V1 cathode at ground
CR2	Crystal diode, clamps V2 cathode at ground
CR3	Crystal diode, clamps V3 cathode at ground
CR4	Crystal diode, clamps V4 cathode at ground
R1	Dim intensity vector amplitude control
R2	Master intensity amplitude control
R3	Isolation and current-limiting resistor for CR1
R4	Cathode load resistor for V1
R5	Dim point amplitude control
R6	Bright intensity vector amplitude control
R7	Isolation and current-limiting resistor for CR2
R8	Cathode load resistor for V2
R9	Bright point amplitude control
R10	Cathode load resistor for V3
R11	Dim character amplitude control
R12	Cathode load resistor for V4
R13	Bright character amplitude control
R14	Plate load resistor for switch tubes
R15	Part of voltage divider (with R17)
R16	Feedback resistor from plate to control grid of V5
R17	Part of voltage divider (with R15)
R18	Plate load resistor for V5

3.85 VECTOR GENERATOR

3.85.1 Definition and Description

The vector generator (VG) is a digital-to-analog conversion circuit employed in the Display System to convert binary levels into analog sweep voltages. These analog voltages are utilized in the generation of vectors on the face of the SD CRT. Figure 3–213 is the logic block symbol for the VG.

The VG contains a sweep generator and two decoders, one decoder for the x-axis co-ordinate and the other for the y-axis co-ordinate of the vector. Each decoder consists of six decoder sections employing a pair of ladder networks. The decoder outputs determine the magnitude and polarity of the vector and are applied through analog line drivers to the corresponding x-axis and y-axis positioning plates of the SD CRT.

The VG output, illustrated in figure 3–214, differs from the decoders discussed in paragraph 3.7. Instead of rapid level shifts as a function of binary inputs, the VG output is a trapezoidal voltage (rapid initial fall followed by a slow linear fall in voltage). The final voltage level is a function of the binary inputs and is directly proportional to the length of the associated vector co-ordinate. The polarity of the decoder output is also a function of binary inputs. The time interval for the generation of the decoder output is fixed at 50 μsec.

3.85.2 Principles of Operation

3.85.2.1 Basic Operation

The operation of the VG is essentially the same as the decoders discussed in paragraph 3.7 with one major difference; the outputs are trapezoidal voltages instead of discrete rapid level shifts. As a result, the current supplied to the ladder sections by the current sources (CUS's) must also be trapezoidal. Therefore, it is necessary to apply a control voltage to the CUS's that produce a trapezoidal current. This control voltage is produced by the sweep generator.

The block diagram in figure 3–215 depicts the relationship between the various elements that comprise the VG. Since the x-axis and y-axis decoder portions of the VG are identical, only the x-axis decoder is shown. Each block is identified by its function in the VG. Tube numbers included in the block diagram are keyed to the schematic diagram of the x-axis decoder.

Upon the application of the start-vector gate, the sweep generator produces a trapezoidal voltage. This voltage is applied to the current source tubes of both the x-axis and y-axis decoders. As a result, the CUS's provide a trapezoidal current. Coincident with the application of the start-vector gate, the vector magnitude and sign binary controls are applied to the decoders. The vector sign (a function of co-ordinate polarity) selects the ladder network to which current is directed; the vector magnitude inputs (a function of co-ordinate length) select the ladder sections within the ladder network. The output of the selected ladder network is a trapezoidal voltage whose amplitude is the result of the summation of the individual ladder section voltage drops.

3.85.2.2 Sweep Generator, Detailed Operation

The schematic diagram of the sweep generator is shown in figure 3–216. Table 3–102 lists associated detail parts and their functions. When no vectors are displayed, a +10V level is applied to the input terminal of the sweep generator, causing triode V1 to conduct. Due to the large plate load resistor R1, the plate voltage of V1 only equals +5V. The output of V1 is directly coupled to V2. Since the cathode of V2 is returned to −30V, V2 conducts and the cathode potential rises to +5V. During this quiescent state (no vector presentation), the four paralleled cathode followers (V3A, V3B, V4A, and V4B) conduct, establishing a −150V level at the output terminals of the sweep generator. Capacitor C1 is charged to the potential difference (155V) that exists between the plate of V1 and the common cathodes of the cathode followers.

The sweep generator develops a trapezoidal voltage output when a negative gate (start-vector) is applied to the grid of V1. This input drives V1 beyond cutoff, causing the plate voltage to rise toward B+ (+250V).

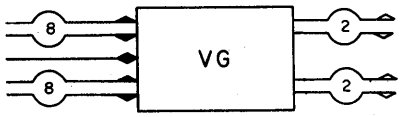


Figure 3–213. Vector Generator, Logic Block Symbol

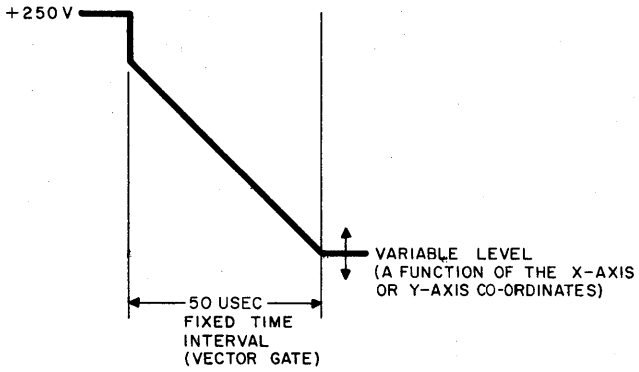


Figure 3–214. Vector Generator, Output Waveform

However, due to RC network C1, R2, and R6, the plate voltage rise is not instantaneous, but, instead, rises trapezoidally with a time constant of 7.05 seconds. As a result of this long time constant, compared to the 50-μsec input gate, the slope of the trapezoid is made very linear because only a small portion of the C1 charge cycle is used. The magnitude of the jump voltage is a function of the R6-R2 ratio. This trapezoidal voltage is then amplified and inverted by V2. The output of V2 is fed through coupling network C2, R5, and C3 to the grids of the four cathode followers. The outputs are fed to the parallel-connected cathodes of the CUS's in each decoder. In addition, a fraction of this output voltage is fed back (degenerative feedback) to the grid of V2 to further improve the linearity of the output voltage.

As a result of cathode degeneration caused by the large cathode resistor R4, the gain of V2 during the time jump voltage is first applied is approximately 3. However, due to the degenerative feedback through C1 and R6, the gain of V2 is reduced to unity. When the start of the slope voltage is applied to V2, the cathode of V2 is at a potential slightly greater than +10V and therefore diode CR1 conducts, reducing the cathode resistance of V2 from 51K to the forward resistance of CR1 (100 ohms). The gain of V2 is now raised to approx-

imately 30. The grid is now positive with respect to the clamped cathode and, as a consequence, grid current flows. This condition exists for the period (50 μsec) that the linear rise appears at the grid of V2. The effective resistance between grid and cathode during this time is 1K, and, in conjunction with R6, determines the magnitude of inverse feedback appearing at the grid of V2. This feedback voltage linearizes the slope voltage applied to the grid of V2 and, hence, the resultant output voltage.

For the function of detail parts not discussed, refer to table 3–102.

3.85.2.3 X-Axis Decoder, Detailed Operation

Figure 3–217 (foldout) is the schematic diagram of the x-axis decoder section of the VG. Table 3–103 lists associated detail parts and their functions. The X-axis decoder is a 6-section decoder consisting of a pair of ladder networks. The output of the decoder is a trapezoidal voltage. The magnitude of this voltage is a function of the binary controls applied to the magnitude gate tubes (V1 through V3); the polarity is determined by the ladder network selected to develop the output. Selection of the ladder network is a function of the binary controls applied to the sign gate tubes (V7 through V12).

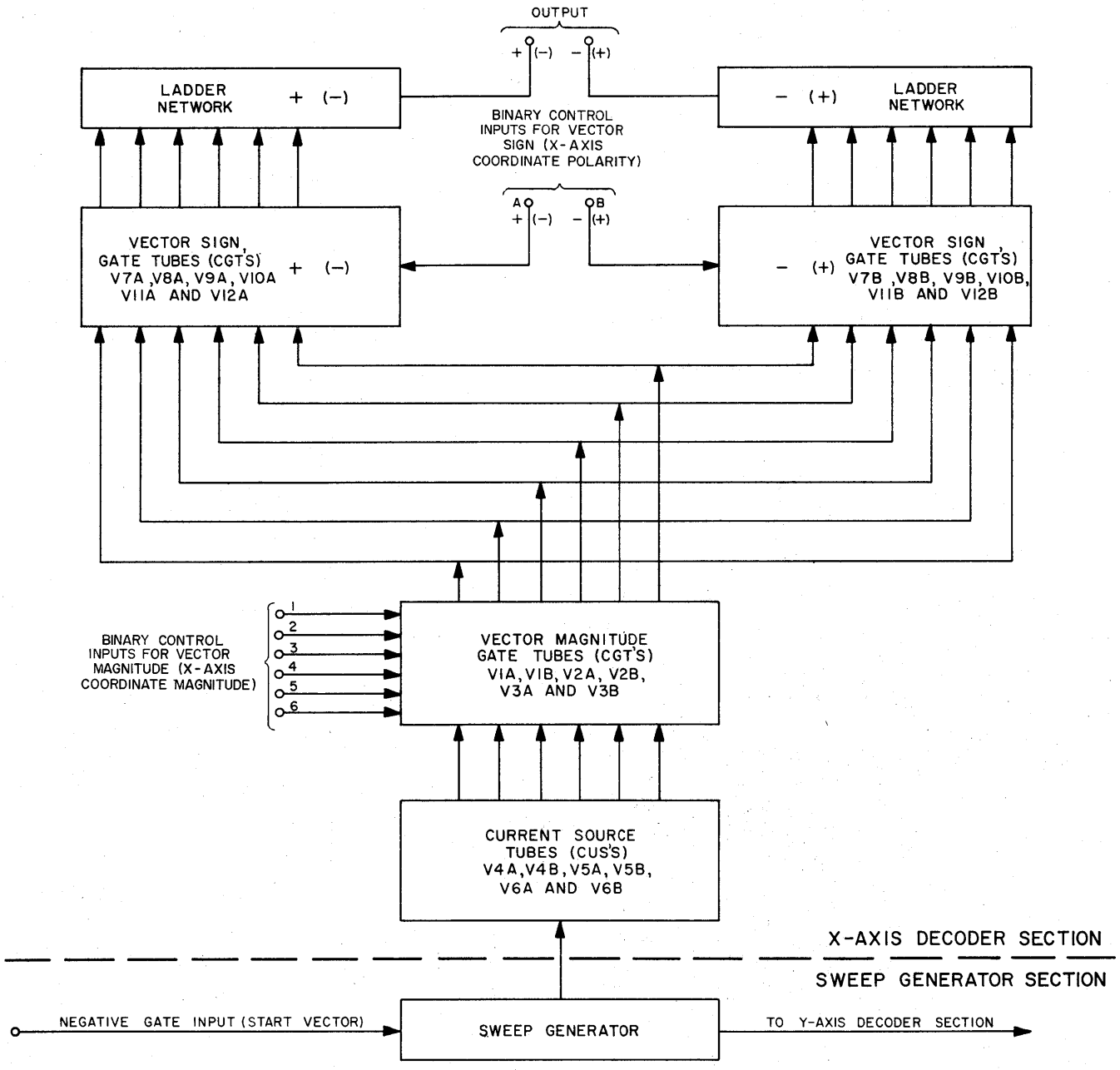


Figure 3–215. Vector Generator, Block Diagram

The grids of the sign gate tubes associated with each ladder network are connected to the complementary outputs of a flip-flop (input terminals A and B). One output of the flip-flop is +10V, the other is −30V. With a +10V input, the sign gate tubes (V7A – V12B, or V7B – V12B) conduct; the grids of these tubes are clamped at ground by the action of diode CR2 or CR4. The input to the other group of gate tubes will be −30V and therefore are cut off.

The current source tubes (V4 through V6) employed in the decoder supply the associated ladder sections with a trapezoidal current instead of a constant current. This is a result of the sweep generator output fed to the cathodes of these tubes. The ladder sections

TABLE 3–102. VECTOR GENERATOR, SWEEP GENERATOR SECTION, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1	Part of trapezoid developing network (with R2 and R6) and part of feedback network (with R6)	R3	Plate load for V2
		R4	Cathode resistor for V2 until CR1 conducts
C2, C3	Part of coupling network (with R5)	R5	Part of coupling network (with C2 and C3)
CR1	Crystal diode, clamps V2 cathode at +10V	R6	Part of trapezoid-developing network (with C1 and R2) and part of feedback network (with C1)
CR2, CR3	Crystal diodes, clamps V3 and V4 grids at −150V	R7, R8	Voltage equalizing resistors for CR2 and CR3
R1	Grid current-limiting resistor for V1	R9	Common cathode load for V3 and V4
R2	Plate load for V1 and part of trapezoid developing network (with C1 and R6)		

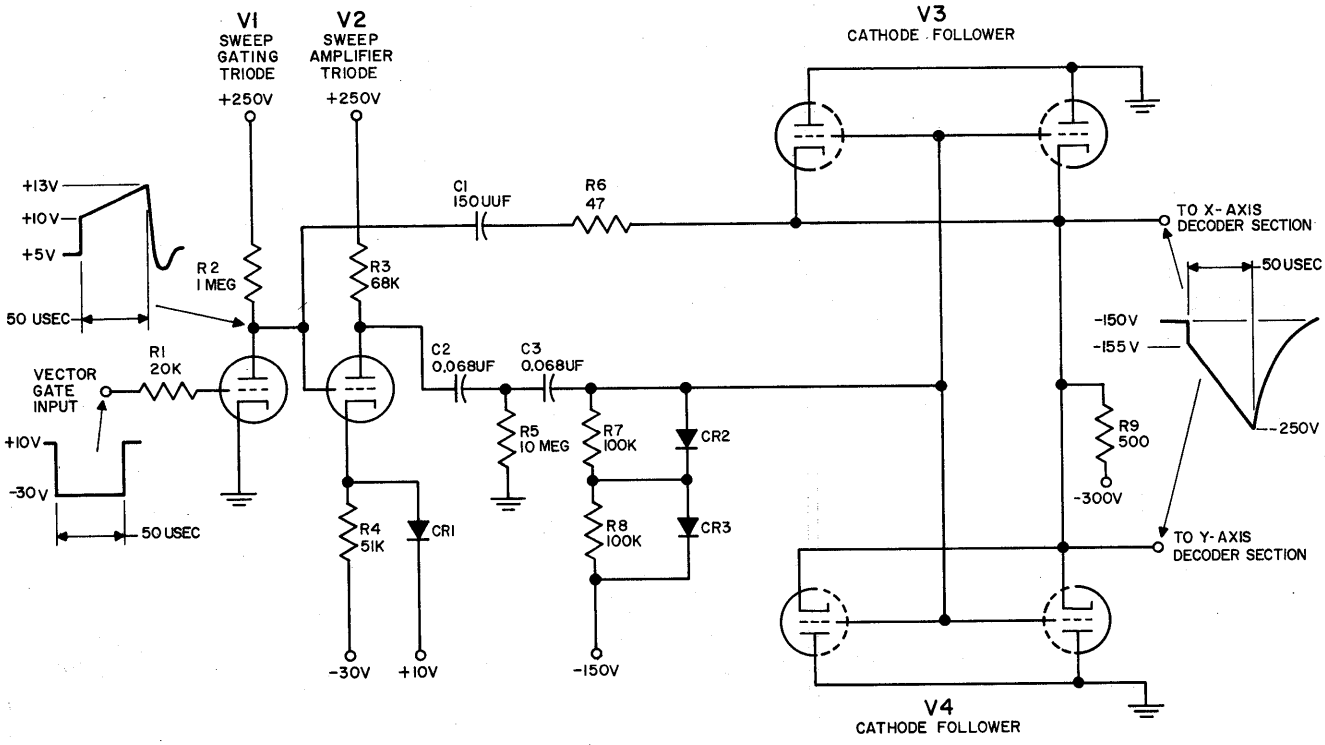


Figure 3–216. Vector Generator, Sweep Generator Section, Schematic Diagram

within the selected ladder network to which current is directed is determined by the inputs (input terminals 1 through 6) to the magnitude gate tubes. With a −30V input, the magnitude gate tube is cut off and its cathode is at ground potential. Since the cathodes of these tubes are connected to the cathodes of the vector sign gate tubes, the cathode of the associated vector gate tube is also at ground potential. This condition enables the current of the associated current source tube to be directed through the vector gate tube, whose grid is clamped at ground, to the associated ladder section of the selected ladder network. When a +10V level is applied, the magnitude gate tube conducts, causing its cathode to rise to +10V which in turn applies a +10V level to the cathode of the associated sign gate tube. Since the grid of the sign gate tube is at ground potential, this cathode potential is sufficient to cut off the tube. The current of the associated current source tube is now diverted through the conducting magnitude gate tube instead of the ladder network. The amplitude of the trapezoidal output is the summation of the individual ladder section voltage drops. Since the decoder comprises six sections, the amplitude will be any one of 64 discrete values.

Consult table 3–103 for the function of detail parts not discussed.

TABLE 3–103. VECTOR GENERATOR, X-AXIS DECODER SECTION, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
CR1, CR2	Vector sign input isolating crystal diodes	R29	Load resistor, part of ladder section (with R30)
CR3, CR4	Clamps grids of vector-sign gate tubes to ground	R30	Branch resistor, part of ladder section (with R29)
R1-R6	Cathode returns for vector-magnitude gate tubes (V1 through V3, respectively)	R31	Load resistor, part of ladder section (with R32)
R7	Bias control for current-source tubes and part of voltage divider (with R8)	R32	Branch resistor, part of ladder section (with R31)
R8	Part of voltage divider (with R7)	R33	Terminating resistor for upper ladder network
R9-R14	Current adjust for current source tubes (V4 through V6, respectively)	R34	Load resistor, part of ladder section (with R35)
R15-R20	Cathode load for current source tubes (V4 through V6, respectively)	R35	Branch resistor, part of ladder section (with R34)
R21	Current-limiting resistor for CR3	R36	Load resistor, part of ladder section (with R37)
R22	Current-limiting resistor for CR4	R37	Branch resistor, part of ladder section (with R36)
R23	Load resistor, part of ladder section (with R24)	R38	Load resistor, part of ladder section (with R39)
R24	Branch resistor, part of ladder section (with R23)	R39	Branch resistor, part of ladder section (with R38)
R25	Load resistor, part of ladder section (with R26)	R40	Load resistor, part of ladder section (with R41)
R26	Branch resistor, part of ladder section (with R25)	R41	Branch resistor, part of ladder section (with R40)
R27	Load resistor, part of ladder section (with R28)	R42	Load resistor, part of ladder section (with R43)
R28	Branch resistor, part of ladder section (with R27)	R43	Branch resistor, part of ladder section (with R42)
		R44	Terminating resistor for lower ladder network

3.86. VECTOR INTENSITY GENERATOR

3.86.1 Definition and Description

The vector intensity generator (VIG) is a nonlogic circuit employed in the Display System. The VIG produces an analog voltage that is applied to the AVGA. This voltage is used to obtain the same degree of intensification (brightness) for all vectors, regardless of length, that are displayed on the face of the SD CRT. The logic block symbol for the VIG is shown in figure 3–218.

Vectors displayed on the face of the SD CRT require special compensation because they are generated by a sweeping point over varying distances in a fixed time interval of 50 μsec. If not compesated for, the degree of intensification of vectors would be inversely proportional to vector length. The VIG produces a voltage whose amplitude is proportional to vector length and is used to compensate for this inconsistency in vector intensification.

3.86.2 Principles of Operation

The schematic diagram for the VIG is shown in figure 3–219, foldout. The list of detail parts and their functions is presented in table 3–104.

There are a total of seven inputs applied to the VIG: a vector on-off gate from the SD timer and six magnitude signals ($X2^{-3}$ to $X2^{-1}$, $Y2^{-3}$ to $Y2^{-1}$) from the vector storage register. The vector-on gate is a 50-μsec negative pulse that is applied to the input cathode follower (V1) each time a vector is generated. The six signals obtained from the vector register represent the three most significant magnitude bits for both the X and Y co-ordinates of the vector to be displayed. These signals are applied to the input adder matrix comprising diode CR2 through CR7 and resistors R3 through R8.

When no vectors are generated, a +10V level is applied to the grids of input cathode follower V1. With a +10V input, V1 conducts and the cathode potential equals +11.5V. Clamping diode CR1 is cut off and as a result +11.5V appear at the anodes of diodes CR2, CR4, and CR6. These diodes conduct through diodes CR3, CR5, and CR7, respectively, placing the output of the adder-matrix at ground potential; consequently the grid of V2A is also at ground potential. With this no-signal condition on the grid of V2A, the VIG does not produce an analog output voltage at this time.

When the vector-on negative gate is applied to the VIG, triode V1 is cut off. The cathode potential of V1 falls toward −150V; however it is clamped at −15V by the action of diode CR1. As a result, diodes CR2, CR4, and CR6 are cut off and the ground potential is removed from the grid of V2A. The digital signals that now appear at the input adder-matrix add together and the sum is applied to the control grid of V2A. Each of the

Figure 3–218. Vector Intensity Generator, Logic Block Symbol

TABLE 3–104. VECTOR INTENSITY GENERATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1-C4	Speedup capacitors
CR1	Crystal diode, clamp V1 cathode at −15V
CR2-CR7	Crystal diodes, part of input adder-matrix (with R3-R8)
CR8-CR10	Crystal diodes, clamps upper output level at 0V
R1	Cathode resistor for V1
R2	Current-limiting resistor for CR1
R3-R8	Part of input adder-matrix (with CR2-CR7)
R9	Grid return for V2A
R10	Plate load resistor for V2A
R11	Common cathode resistor for V2A and V2B
R12, R13, R14	Voltage divider
R15	Cathode resistor for V3
R16	Common plate load resistor for V4, V5 and V6
R17, R18	Voltage divider
R19, R20, R21	Equalizing resistors for CR8, CR9, CR10, respectively
R22	Part of feedback voltage divider (with R23 and R24)
R23	Gain control and part of feedback voltage divider (with R22 and R24)
R24	Part of feedback voltage divider (with R22 and R23)

six inputs to the adder matrix are connected to the 0 side of a flip-flop in the vector register. Therefore, if a binary 1 is stored in the flip-flop, a −30V level appears at the associated input resistor in the adder matrix. When a 0 is stored, the input to the matrix becomes a +10V level. A +10V level causes the associated input diode (CR3, CR5, or CR7) to conduct, placing that segment of the matrix at ground. Therefore, the sum voltage appearing at the grid of V2A is the contribution of only those inputs that represent a binary 1. This voltage varies from 0 volts for the shortest vector (a point) to −15V for the longest vector. The amplified output of V2A is directly coupled to cathode follower V3. The output of V3 is used to drive six parallel-connected amplifiers that comprise the output stage. The amplified analog output, proportional to vector length, varies from 0 to −150V. This output is applied to the AVGA in each of the SD consoles in the Display System. The upper level of the output is clamped at 0 volts by diodes CR8, CR9, and CR10.

A degenerative feedback loop, consisting of voltage divider R22, R23, and R24, is employed between the output stage and the grid of V2B. In addition to stabilizing the output, the feedback is also used to establish the operating point of V2A and hence the gain of V2A. The amount of feedback is controlled by potentiometer R23. Should the output increase (more negative) for a given vector length, the voltage fed back to the grid of V2B becomes more negative. As a result, the plate current of V2B decreases, causing the potential of the common cathode for V2A and V2B to decrease. This decrease in cathode potential produces an increase in the plate current of V2A, which in turn causes the plate voltage of V2A to drop. This fall in plate voltage, amplified by V3, causes the output voltage to become more positive, thus returning the output to its proper level. Conversely, regulation takes place if the output were to decrease for a given vector length.

For the function of detail parts not discussed, refer to table 3–104.

3.87 VOLTAGE REGULATORS, MODELS A, B, AND C

3.87.1 Introduction

The voltage regulators (VR's) are nonlogic circuits that derive regulated voltage outputs from standard service voltage inputs.

There are three models of the VR utilized in Input System logic. Each model is described separately in the following paragraphs.

3.87.2 Voltage Regulator, Model A

3.87.2.1 Definition and Description

The logic block symbol for the AVR is shown in figure 3–220. This circuit is used in the LRI monitor to provide the sine-cosine approximator (SCA) with two closely regulated bias voltage of +16V and −16V potentials. These voltages ensure accurate and stable operation of the SCA.

The AVR is actually composed of two separate circuits: one for the +16V output, and one for the −16V output. The theory of operation of both circuits are identical, and for this reason, only the +16V section will be discussed in detail.

3.87.2.2 Principles of Operation

The schematic diagrams of both sections of the AVR are shown in figures 3–221 and 3–222. Table 3–105 lists associated detail parts and their functions. The essential differences between both circuits as can be noted in the schematics are in connections of VR1 and in the cathode supply for V3. Each section consists of a differential amplifier, a high gain d-c amplifier, a triode-series current tube, a gas-tube voltage regulator, and a feedback circuit.

TABLE 3–105. VOLTAGE REGULATOR, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1-R4	Voltage divider
R5	V1A plate load resistor
R6	V1A, V1B common cathode resistor
R7, R8	Voltage divider which forms d-c coupling network (with C2)
R9	Feedback resistor
R10	Part of phase-compensating network (with C3)
R11	V2 plate load resistor
R12, R13	Voltage divider which forms d-c coupling network (with C4)
R14	V3 cathode resistor
C1	Compensating capacitor for feedback network
C2	Compensating capacitor in d-c couling network (with R7 and R8)
C3	Part of phase-compensating network (with R10)
C4	Compensating capacitor in d-c coupling network (with R12 and R13)
C5	Bypass capacitor

The regulating action of the +16V regulator is obtained by comparing a fixed fraction of the output potential from the cathode of V3 with the output potential of VR1. Any difference between the two is presented to the d-c amplifier and is applied from the output of V3 to the grid of V1B. In this manner, any variation in the output load is compensated for, with the result that the +16V is maintained constant.

The regulated +150V plate supply of V1A is returned to ground through voltage divider R1-R4. A portion of this voltage, kept constant by the voltage-regulating action of VR1, is applied to the grid of V1A. The output voltage to be compared feeds through R9 to the grid of V1B.

Duo-triode V1 initially conducts with the application of power. The cathode side of R6 will be positive with respect to ground, causing the plate of V1A to become more positive. This voltage is fed through R7 to the grid of V2. The amplifier output of V2 is fed to the grid of V3 through R12 and C4. The resulting variation in current through the V3 cathode resistor produces a voltage change which is fed back to the grid of V1B. This will change the plate current in V1B and, due to the common cathode connection, the plate current in V1A will also change. In this manner, any change in output is reflected back to the grid of V1B and compared to the standard voltage on the grid of V1A. The ensuing compensation makes the output constant at +16V.

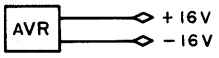


Figure 3–220. Voltage Regulator, Model A, Logic Block Symbol

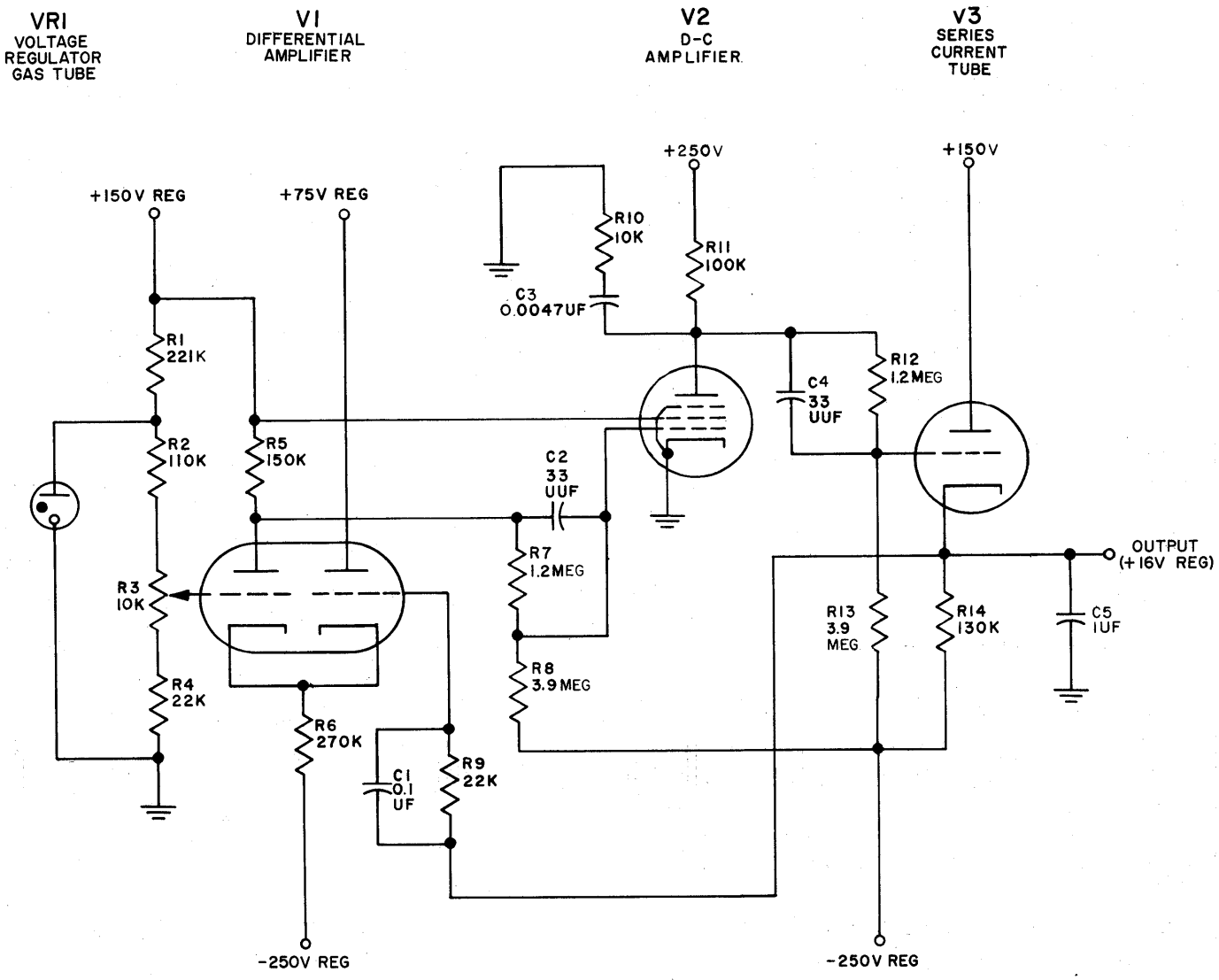


Figure 3–221. Voltage Regulator, Model A, +16V Section, Schematic Diagram

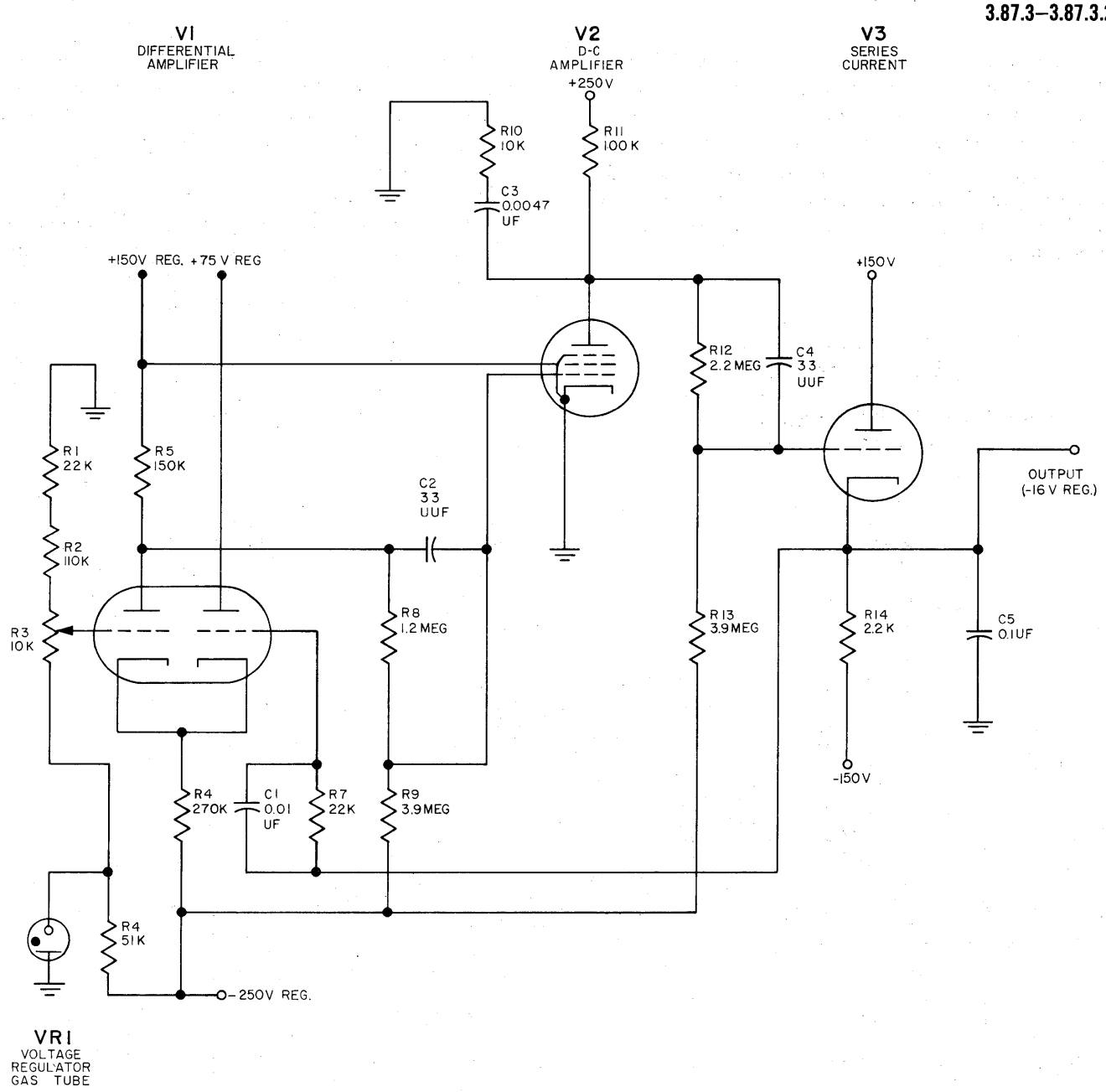


Figure 3–222. Voltage Regulator, Model A, –16V Section, Schematic Diagram

3.87.3 Voltage Regulator, Model B

3.87.3.1 Definition and Description

The logic block symbol for the BVR is shown in figure 3–223. This circuit is used in the Input System to provide the distribution power amplifiers with regulated —150V and —250V supplies to minimize power supply voltage fluctuations. The —250V supply is also used by the AVR.

The BVR, like the AVR, is also composed of two separate circuits. These circuits supply —150V and —250V outputs respectively. Since both circuits operate identically, only the —150V section will be described in detail.

3.87.3.2 Principles of Operation

Figures 3–224 and 3–225 are the schematic diagrams for both the —150V and the —250V sections of the BVR. Table 3–106 lists associated detail parts and their functions. The description of the —150V section follows.

With the application of power, differential amplifier V1 conducts. The portion of the output voltage to be compared with the standard voltage is established at the grid of V1A. This voltage, which is the bias voltage that determines the operating point of the tube, is obtained from voltage divider R1, R2, R3, R17, and R18. The voltage to be compared with the output is applied

to the grid of V1B through resistor feedback network R11, R10, and R9. The difference in compared voltages is coupled from the plate of V1B to the grid of V2 through a d-c coupling network consisting of C2 and R8.

The plate of V2, is directly coupled to the grid of V3. The cathode of V3 is maintained at a positive potential by voltage regulator tubes VR1, VR2, and VR3 connected to the —300V supply.

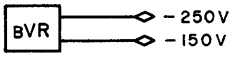


Figure 3—223. Voltage Regulator, Model B, Logic Block Symbol

The series current control tube V4A has its plate returned to ground through R14. The stabilizing regulator action of tube V1A removes a-c compounds superimposed on the d-c voltage. Capacitor C3 prevents any slow changes in voltage from passing through. However, ripple voltages reduce the current flow in V4 and R14, thereby stabilizing the output voltage. The cathode of V4 is returned to the regulated —150V output. Thus, any variation in output is fed back to the grid of V1A and the compensation in the differential tube current holds the output constant.

The —250V regulator section, with the exception of an additional gas VR tube and the connection of V4 to —150V, operates the same as the —150V section of the BVR.

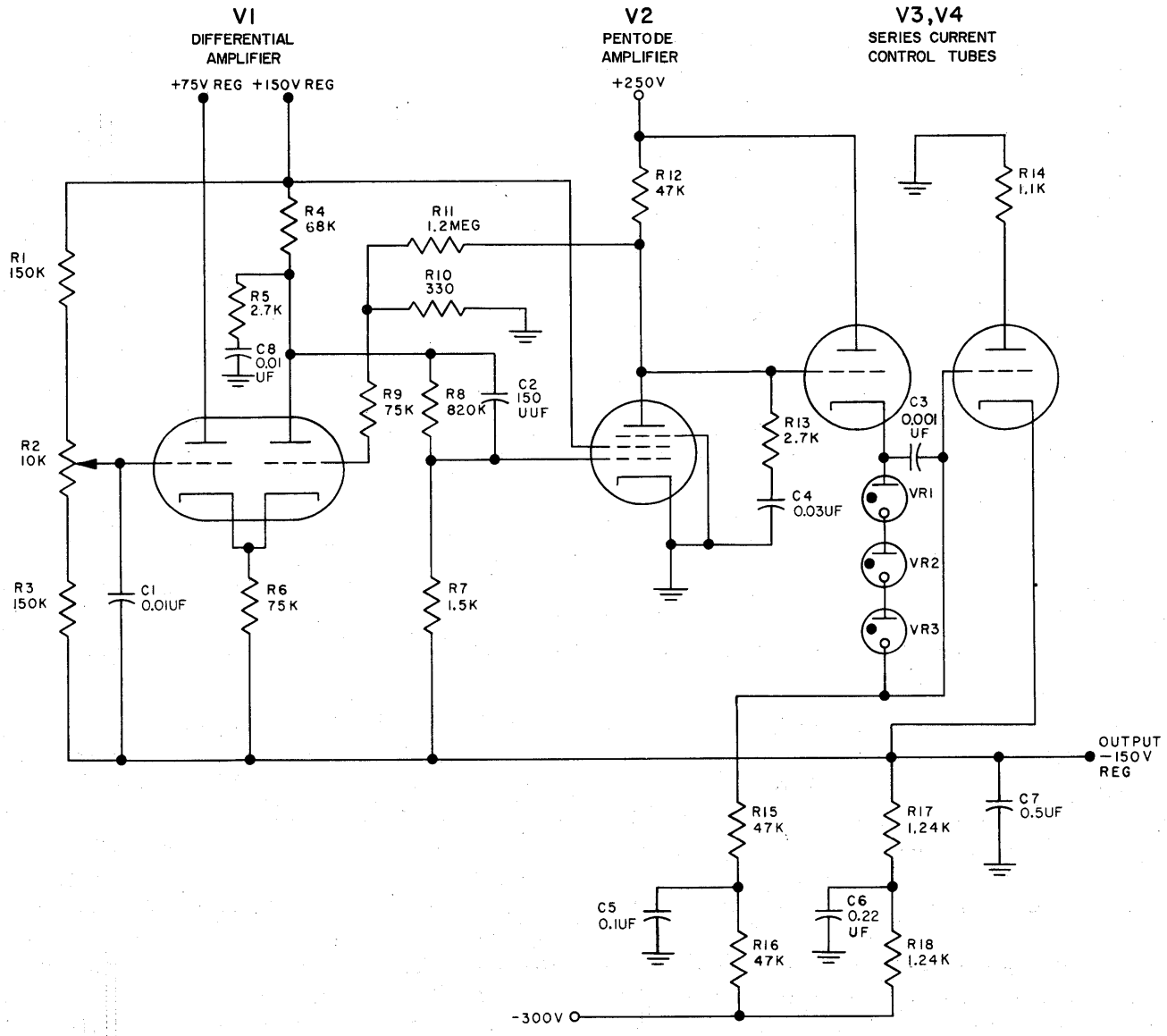


Figure 3—224. Voltage Regulator, Model B, —150V Section, Schematic Diagram

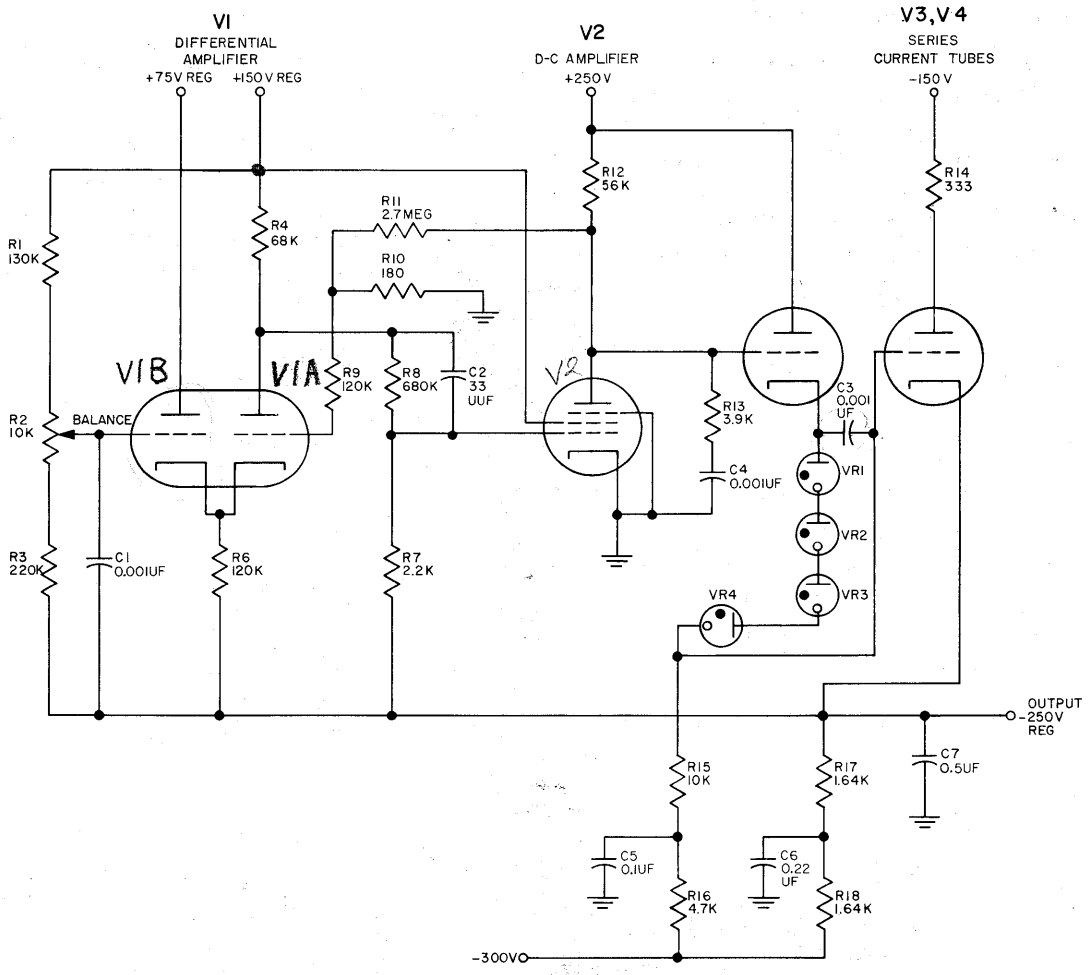


Figure 3–225. Voltage Regulator, Model B, –250V Section, Schematic Diagram

TABLE 3–106. VOLTAGE REGULATOR, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1, R2, R3	Form voltage divider (with R17 and R18)	R17, R18	Form voltage divider (with R1, R2, and R3)
R4	V1B plate load resistor	C1	Compensating capacitor
R5	Part of transient damping network (with C8)	C2	Compensating capacitor in voltage divider d-c coupling network (with R7, R8)
R6	V1 cathode resistor		
R7, R8	Voltage divider which forms d-c coupling network (with C2)	C3	Stabilizing capacitor
R9, R10, R11	Feedback network	C4	Part of transient damping network (with R13)
R12	V2 plate load resistor	C5	Bypass capacitor
R13	Part of transient damping network (with C4)	C6	Bypass capacitor
R14	V4 plate resistor	C7	Stabilizing capacitor
R15, R16	Current-limiting resistors for VR1-VR3	C8	Part of transient damping network (with R5)

3.87.4 Voltage Regulator, Model C

3.87.4.1 Definition and Description

The logic block symbol for the cVR is shown in figure 3–226. In Input System logic, the cVR supplies a constant +150V reference potential to the binary decoder in order to ensure an accurate output from the decoder. The cVR also supplies the buffer amplifier and the AVR with +100V and +75V regulated supplies, respectively.

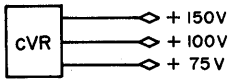


Figure 3–226. Voltage Regulator, Model C, Logic Block Symbol

3.87.4.2 Principles of Operation

Figure 3–227 is the schematic diagram of the cVR. Table 3–107 lists associated detailed parts and their functions. The circuit consists of a differential amplifier with negative feedback and a duo-triode series current tube controlled by a pentode d-c amplifier.

The grid input network of tube V1A, consisting of resistors R1, R2, and R3, determines the grid bias volt-

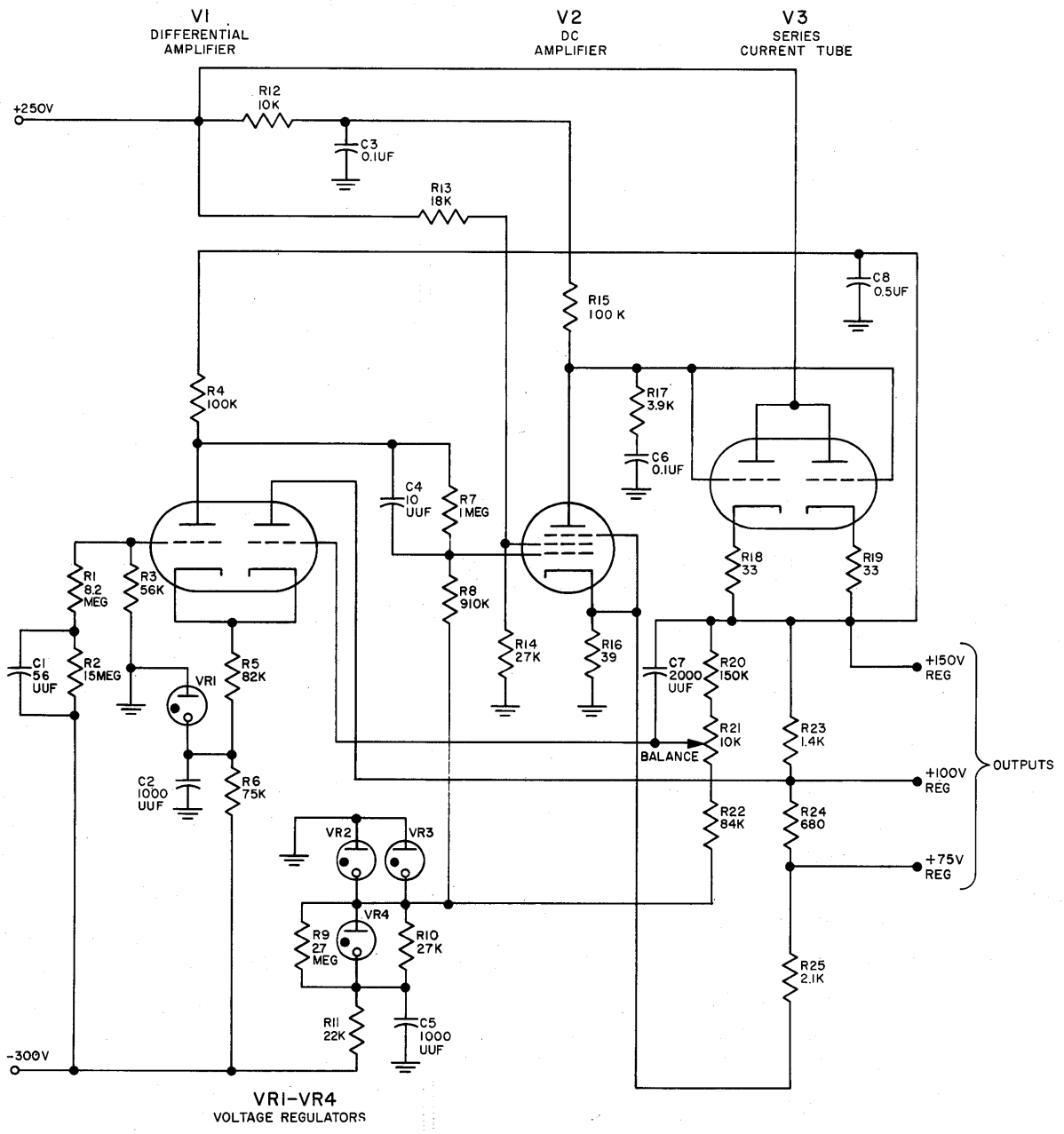


Figure 3–227. Voltage Regulator, Model C, Schematic Diagram

age against which the difference voltage is compared. The portion of the output voltage to be compared is fed from potentiometer R21 to the grid of V1B. Thus the difference in the two voltages is amplified by the differential tube and coupled to the grid of V2.

TABLE 3–107. VOLTAGE REGULATOR, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2, R3	Voltage divider in V1A grid circuit
R4	V1A plate load resistor
R5, R6	V1 cathode resistors
R7, R8	Form d-c coupling network (with C4)
R9, R10, R11	Voltage distribution resistors
R12	Part of decoupling network (with C3)
R13, R14	Voltage divider in V2 screen grid circuit
R15	V2 plate load resistor
R16	Part of voltage divider, which functions as a bleeder and feedback network for V2 (with R23, R24, and R25)
R17	Part of transient damping network (with C6)
R18, R19	Current-equalizing resistors
R20, R21, R22	Voltage divider and feedback network to V1B
R23, R24, R25	Part of voltage divider network which functions as a bleeder and feedback network for V2 (with R16)
C1	Bypass capacitor
C2	Bypass capacitor
C3	Part of decoupling network (with R12)
C4	Compensating capacitor which is part of d-c coupling network (with R7, R8)
C5	Bypass capacitor
C6	Part of transient damping network (with R17)
C7	Compensating capacitor
C8	Bypass capacitor

The voltage-dropping network between the plate of V1A and the control grid of V2 is returned to a reference voltage, regulated by gas tubes VR1, VR2, and VR3. The amplified output of V2 is directly coupled to the grids of the paralleled series control tube (V3A and V3B). The output from V3 cathodes is returned to the +150V output and to a voltage divider network. The +100V and +75V are taken from appropriate sections of the voltage divider network.

3.88 WARNING LIGHT RELAY DRIVER, MODEL A

3.88.1 Definition and Description

The model A warning light relay driver (AWLD) is a nonlogic circuit that supplies a d-c output when triggered by a pulse input. The logic block symbol for this circuit is shown in figure 3–228.

The AWLD is located in the warning light storage and indicator element and is used to drive a relay which in turn actuates an audible alarm. This alarm warns operators at different operating and maintenance positions of various malfunctions and unusual types of programming operations.

3.88.2 Principles of Operation

Figure 3–229 is the schematic diagram of the AWLD. Table 3–108 lists associated detail parts and their functions. The circuit consists of a thyratron and its associated components.

TABLE 3–108. WARNING LIGHT RELAY DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Isolating resistor
R2, R3	Voltage divider between —150V and —300V
R4	Grid-limiting resistor
R5	V1 cathode resistor
R6	V1 plate resistor
R7	V1 screen-limiting resistor
R8, R9	Current-limiting resistors
R10	Prevents sparking upon depression of RESET button (with C4)
C1	Coupling capacitor
C2	Bypass capacitor
C3	Bypass capacitor
C4	Prevents sparking upon depression of RESET button (with R10)

The input to the circuit is supplied by a flip-flop in the warning light storage element. When the flip-flop is set in the 1 state, a positive level shift is applied to coupling capacitor C1. The shift in level is differentiated by C1 and R1, and the positive pulse developed across R1 is integrated by R4 and C2. When the voltage across C2 raises the grid of V1 sufficiently to cause V1 to conduct, relay K4 in V1 plate circuit becomes energized and power is applied to an audible alarm.

In order to de-energize the audible alarm, the RESET pushbutton is depressed. This opens the plate circuit of the thyratron, resulting in the tube becoming nonconductive and K4 becoming de-energized.

3.89 WRITE HEAD DRIVER

3.89.1 Definition and Description

The write head driver (WHD) is a nonlogic circuit which provides the power pulse required for the write heads to record azimuth and substitute azimuth pulses magnetically. The logic block symbol for the WHD is shown in figure 3–230.

3.89.2 Principles of Operation

Figure 3–231 is a schematic diagram of the WHD. Table 3–109 lists associated detail parts and their functions. The circuit consists of a single-stage thyratron used as the driver tube. With no signal applied to the grid, the fixed bias of —15V maintains the thyratron at cutoff and stops current flow in the write head coil

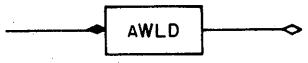


Figure 3–228. Warning Light Relay Driver, Model A, Logic Block Symbol

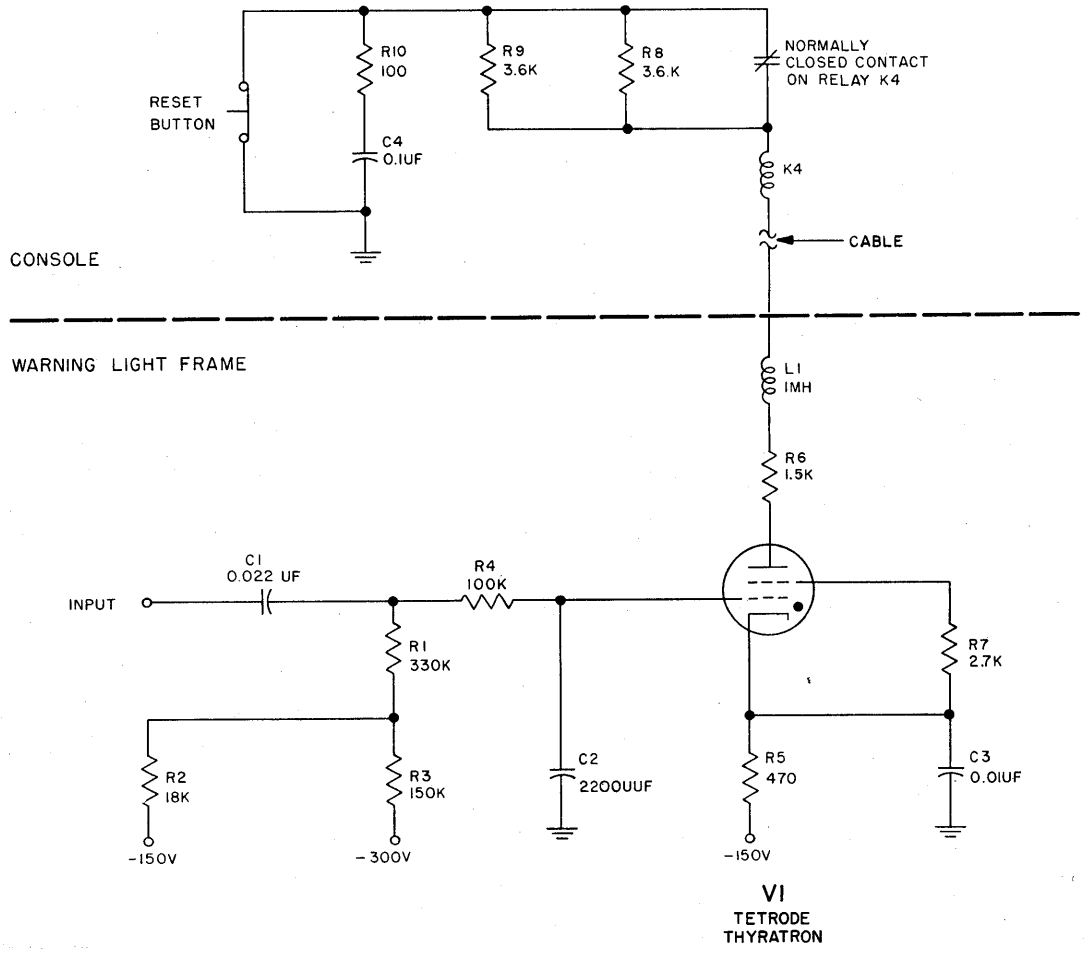


Figure 3–229. Warning Light Relay Driver, Model A, Schematic Diagram

which is in series with the plate supply line. Capacitors C2 and C3 are then charged to +150V.

As a positive trigger pulse with an amplitude of 40V (lower level —30V, upper level +10V) is applied to the grid, the bias on the tube is overcome and causes ionization of the thyratron with resultant plate current flow. At the same instant current flow commences, C2 and C3 begin to discharge through the write head coil (L1), resistor R4, and the tube. The following factors govern the amplitude of the write head current: the value of C2 and C3, the impedance of the write head coil, the value of R4, and the internal resistance of the tube. The current builds up to a maximum of 0.35 ampere and drops back to zero as the capacitors discharge. When the voltage across the thyratron falls below the deionization point, the tube cuts off and restores control to the control grid. With the tube cut off, C2 and C3 begin to recharge to +150V through R3.

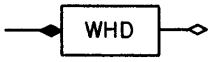


Figure 3–230. Write Head Driver, Logic Block Symbol

TABLE 3–109. WRITE HEAD DRIVER, FUNCTION OF DETAILED PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Grid bias network
R3	Plate load resistor
R4	Current-limiting resistor
R5	Shield grid return
C1	Coupling capacitor
C2, C3	Charging network
L1	Write head coil

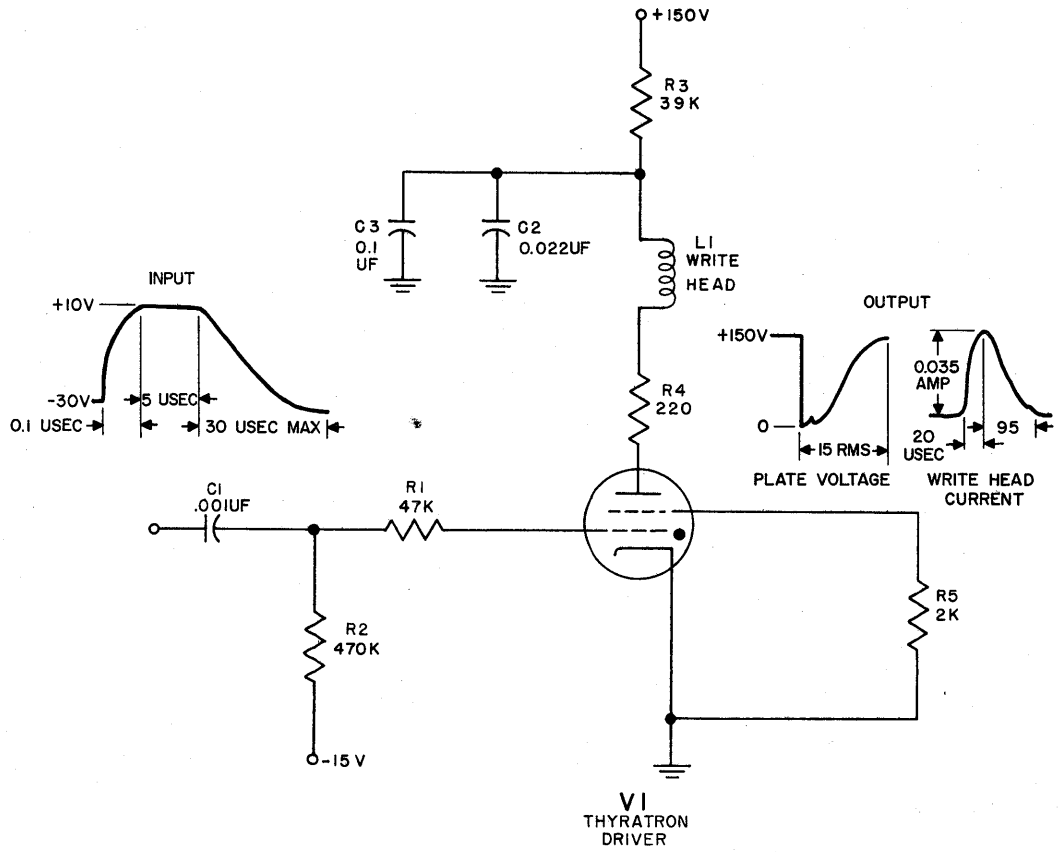


Figure 3–231. Write Head Driver, Schematic Diagram

CHAPTER 4
OTHER CIRCUITS, THEORY OF OPERATION

4.1 ACTIVATE CIRCUIT

4.1.1 Definition and Description

The activate circuit is a logic circuit which applies a +10V pulse to an associated core upon depression of the ACTIVATE pushbutton. In Input System logic, the ACTIVATE pushbutton is used by the console operator to signal the Central Computer that there is a keyboard message in the core matrix ready to be read into the Central Computer. This is done after a message has been set up at a console keyboard.

4.1.2 Principles of Operation

Figure 4–1 is the schematic diagram of the activate circuitry. Table 4–1 lists the associated detail parts and their functions.

The ACTIVATE pushbutton is normally open, allowing C1 to charge to +10V through R1. When the pushbutton is depressed, mercury contact relay K1 is momentarily energized, providing a discharge path for the capacitor through R2 and the associated core in the core matrix. This action results in a pulse being applied to the core, setting the core to the 1 state. During the readout operation of the core matrix, the "A" bit contained in the core associated with a specific ACTIVATE pushbutton is destroyed and is not restored until the pushbutton is again depressed.

4.2 HIGH-VOLTAGE POWER SUPPLIES

4.2.1 Definition and Description

The high-voltage power supplies are nonlogic circuits that provide the accelerating potentials for the CRT's in the Display and Input Systems. Several high-voltage power supplies are utilized in AN/FSQ-7 and -8

TABLE 4–1. ACTIVATE CIRCUIT, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Current-limiting resistor
R2	Parasitic suppressor
R3	Part of network which prevents arcing across S1 (with C2)
R4	Current-limiting resistor
R5	Damping resistor
R6	Current-limiting resistor
C1	Prevents surge voltages from overloading set winding (with L1)
C2	Prevents arcing across S1 (with R3)
L1	Prevents overloading of set winding (with C1)

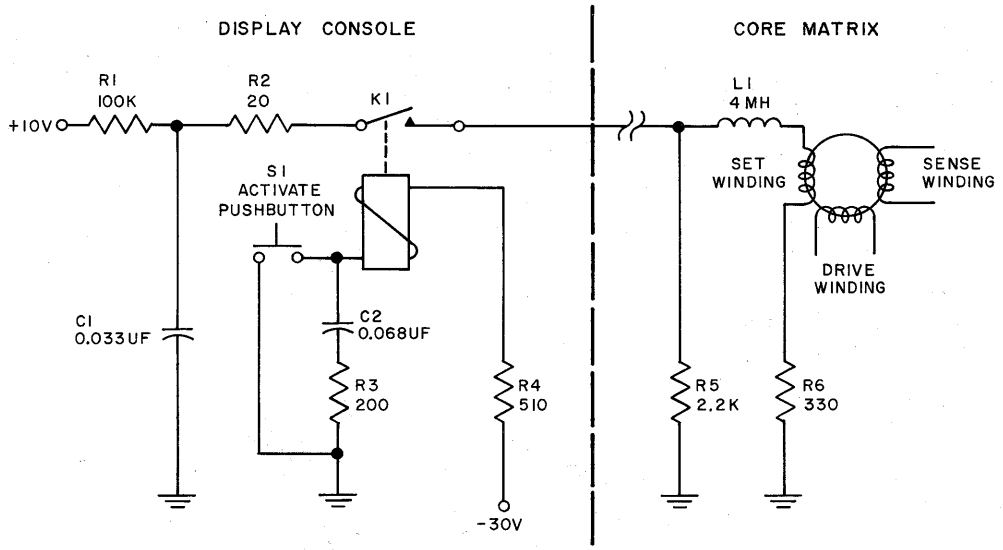


Figure 4–1. Activate Circuit, Schematic Diagram

equipments. Each power supply is described separately below.

4.2.2 Principles of Operation

4.2.2.1 High-Voltage Power Supply, 3,000V

The 3,000V display high-voltage power supply supplies accelerating potentials for the Command Post DD CRT's. There is a power supply of this type for the DD CRT's in each desk of the Command Post console. Each staff desk has two and the command desk has three.

Figure 4–2 is the schematic diagram for the 3-kv power supply. Table 4–2 lists the associated detail parts and their functions. The circuit employs a standard full-wave bridge rectifier. The power transformer has a tapped primary winding permitting a selection of any one of five input voltages to the rectifier. The output of the rectifier, a pulsating dc, is smoothed by a filter network consisting of resistor R1 and capacitors C1 and C2. A voltmeter connected across bleeder resistor R3 gives a visual indication of the output voltage potential.

4.2.2.2 High-Voltage Power Supply, –3,450V

The –3,450V display high-voltage power supply furnishes anode 2 with accelerating potentials for the SD and DD CRT's.

Figure 4–3 is the schematic diagram for the –3,450V power supply. Table 4–3 lists the associated detail parts and their functions. The circuit consists of two standard full-wave bridge rectifiers of –3,300 and –150V and a saturable core reactor regulator. Both rectifiers employ filter networks to minimize the ripple voltage in the outputs. The –3,300Vdc output is obtained in the –3,300V rectifier, with the positive output terminal at ground. A voltmeter, in series with R11 across the output terminals of this rectifier, provides a visual indication of output voltage for adjustment purposes. The

TABLE 4–2. HIGH-VOLTAGE POWER SUPPLY, 3,000V, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Part of filter network (with C1 and C2)
R2, R3	Bleeder network
R4	Current-limiting resistor
CR1-CR4	Selenium rectifiers
C1, C2	Part of filter network (with R1)
T1	Power transformer
M1	Output voltmeter

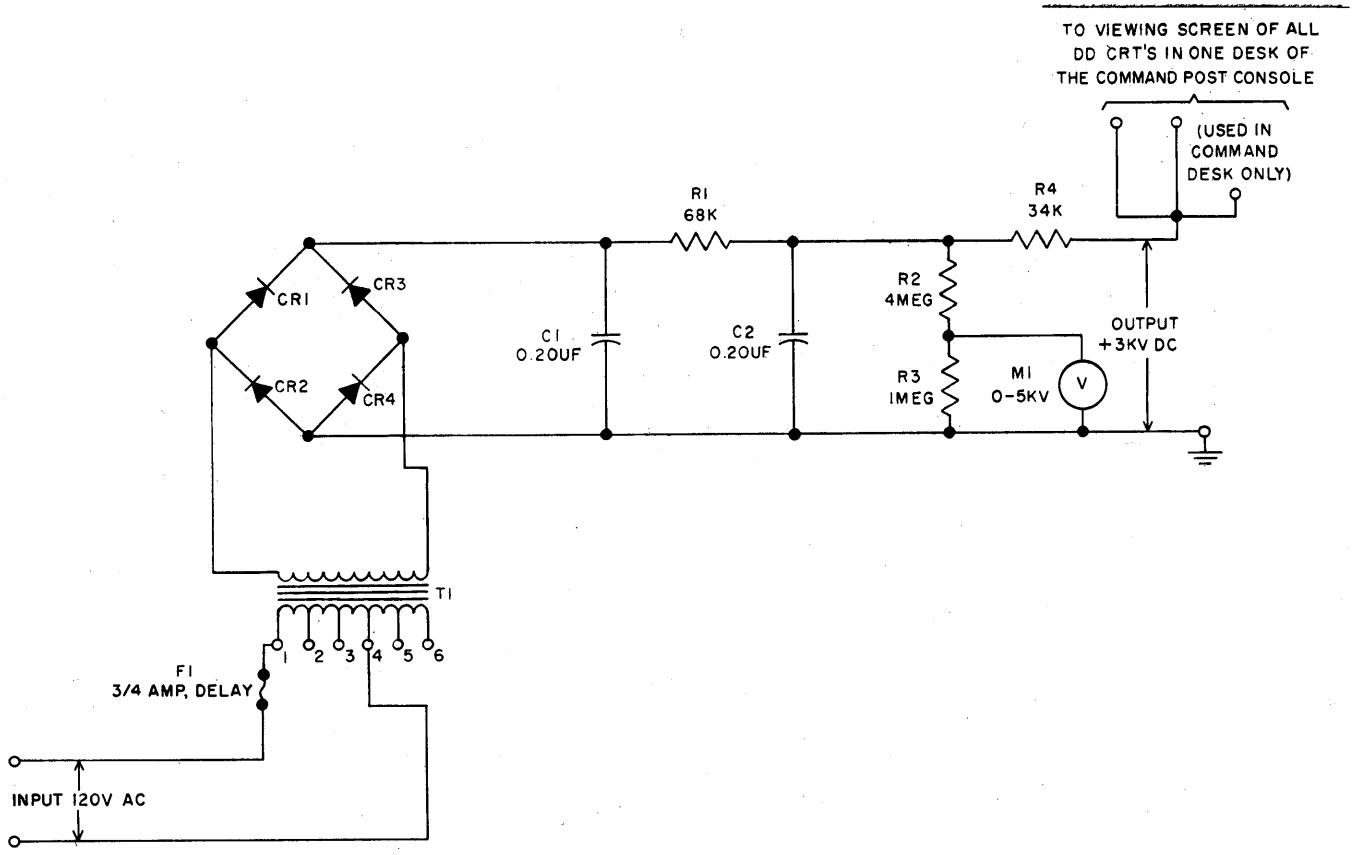


Figure 4–2. High-Voltage Power Supply, 3,000V, Schematic Diagram

TABLE 4–3. HIGH-VOLTAGE POWER SUPPLY, –3,450V, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	Current adjustment for L1	C1	Part of pi filter (with C4 + R8)
R2	Current-limiting resistor	C2	Part of pi filter (with C5 + R9)
R3	Output voltage control for high-voltage rectifier	C3	Speedup capacitor
		C4	Part of pi filter (with C1 + R8)
R4	Current adjustment for L7	C5	Part of pi filter (with C2 + R9)
R5	Current-limiting resistor	C6	Smoothing capacitor
R6	Part of voltage divider (with R3)	F1, F2	Fuses
R7	Voltage-dropping resistor	K1	2-second delay relay
R8	Part of pi filter (with C1 + C4)	L1-L3	Saturable core reactor regulator A
R9	Part of pi filter (with C2 + C5)	L4-L7	Saturable core reactor regulator B
R10	Voltage-dropping resistor	T1	Regulator transformer
R11	Current-limiting resistor for voltmeter	T2	Low-voltage rectifier input transformer
CR1-CR8	Selenium cartridges connected in full-wave rectifier bridge circuit	T3	High-voltage rectifier input transformer

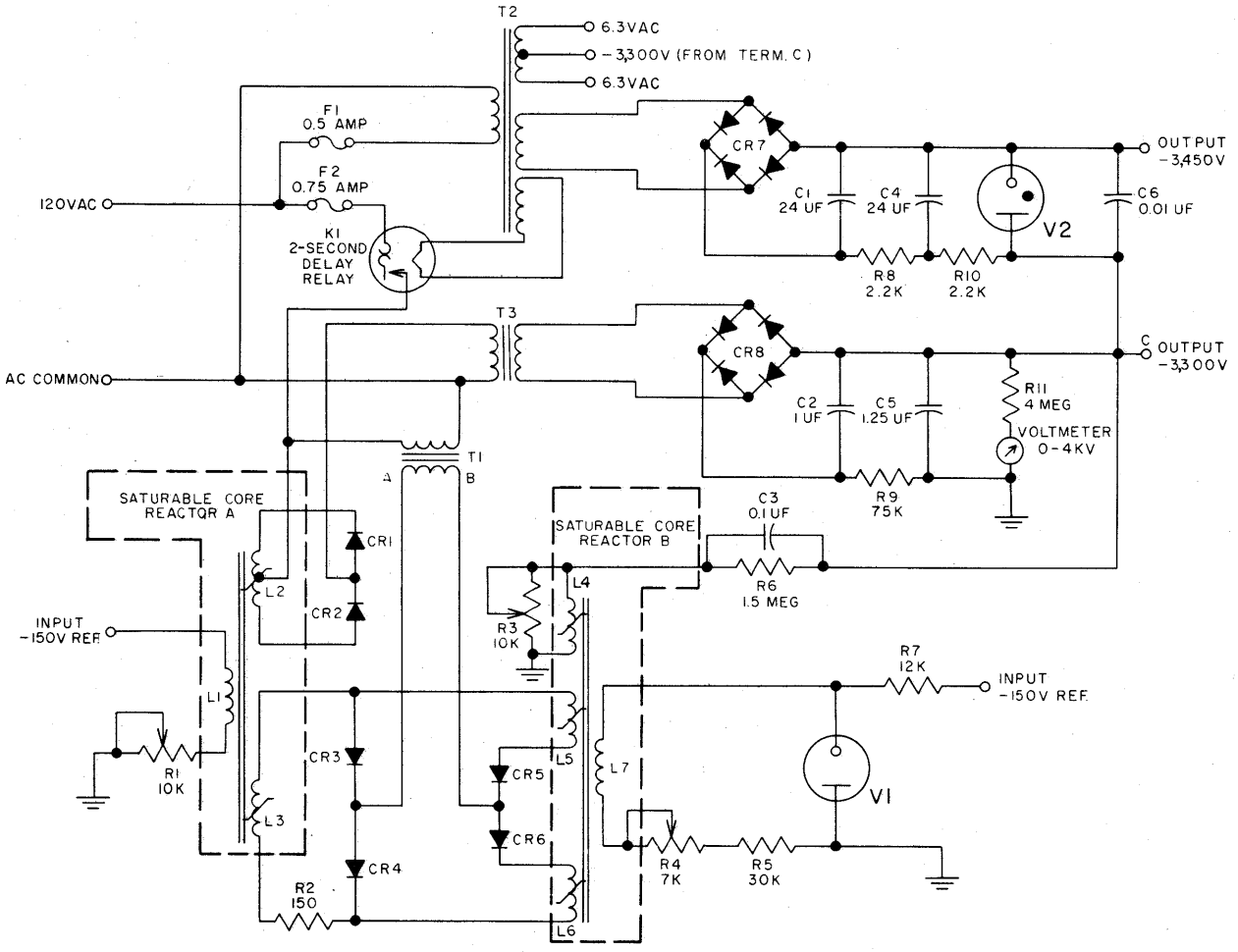


Figure 4–3. High-Voltage Power Supply, –3,450V, Schematic Diagram

output voltage of the —150V rectifier is developed across voltage regulator V2. The positive output terminal of the —150V rectifier is connected to the negative output terminal of the —3,300V rectifier. This produces —3,450V at the negative output terminal of the —150V rectifier.

The operation of the saturable core reactor regulator is divisible into two parts: the input regulator and the output regulator. Input regulation is accomplished by windings L1, L2, L3, L5, L6, L7, transformer T1, and the input circuits of windings L1 and L7. The primary winding of T1 is connected to a 120Vac supply through time delay relay K1. The secondary winding is connected in a full-wave bridge rectifier. With point A (T1 secondary) negative, electrons flow from point A through CR3, L3, L6, R2, and CR6 to point B. With point B negative, electrons flow from point B through CR5, L5, L3, R2, and CR4 to point A. Reference voltages applied to windings L1 and L7 supply the currents for magnetic biasing of saturable reactors A and B. The degree of flux saturation is adjustable by means of resistors R1 and R4.

An increase in input voltage to the primary of T1 increases the current in the secondary of T1. Increased current through L3 increases the impedance of L2. L2 is in series with the primary of high-voltage transformer T3. The increased impedance results in a greater voltage drop across L2, neutralizing the rise of the input voltage across the T3 primary. A fall of input voltage is similarly compensated for by a decrease in inductance and a resultant decrease in voltage drop across L2.

Output regulation is accomplished by the reaction of cores A and B to fluctuations in the sample applied across winding L4 and resistor R3. This voltage is proportional to the output of the —3,300V supply. Variations of output voltage produce proportional voltage variations across L4 and R3. An increase in output voltage produces a corresponding voltage increase across L4 and R3.

The resultant increased voltage drops across L5 and L6 increase current through L3. Increased current through L3 increases the impedance of L2, thereby decreasing the magnitude of voltage applied to the primary of T3. Reduction of voltage across the primary of T3 results in a fall of output voltage, restoring the desired level. A fall of output voltage is similarly compensated for by an increase in voltage applied across the primary of T3.

4.2.2.3 High-Voltage Power Supply, 6-12KV

The 6-12kv display high-voltage power supply provides viewing screen accelerating potentials for the DD and SD CRT's. It is used in both the SD and auxiliary consoles. Figure 4–4 is the schematic diagram for the 6-12kv power supply. Table 4–4 lists the associated detail parts and their functions.

The circuit utilizes a standard full-wave bridge rectifier. The primary of the rectifier transformer is multitapped, permitting a selection of five d-c potentials from 6.0 kv to 12 kv in increments of approximately 2 kv. For its application in the Display System, the 9-kv input tap is used. Ripple is minimized by a pi filter consisting of C1, C2, and R1. A voltage divider across the output terminals provides three output voltages of which two are used. The 9.0-kv output is used for the SD CRT, and a 3.3-kv output is used for the DD CRT. The auxiliary console utilizes only the 3.3-kv output. The voltmeter across R6 gives a visual presentation of the maximum voltage output of the rectifier.

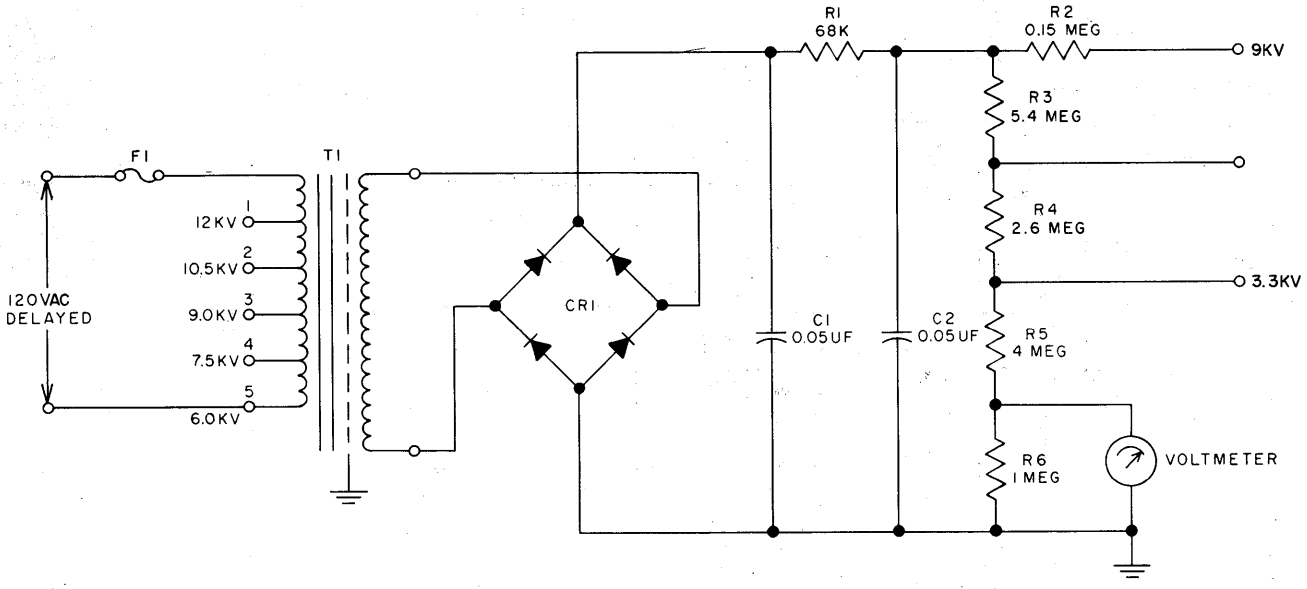


Figure 4–4. High-Voltage Power Supply, 6-12KV, Schematic Diagram

4.3 HIGH-VOLTAGE UNITS

4.3.1 Definition and Description

The high-voltage units are nonlogic circuits used to combine and to apply the d-c and variable control voltages necessary for the operation of Display and Input System CRT's. Each high-voltage unit consists of two sections: an electronic section and a control network section. Since the control networks have the same circuit configuration and differ only in the value of detail parts, they are discussed in general on the basis of a typical network. However, the electronic sections of each high-voltage unit differ one from another and are discussed by model designation.

TABLE 4–4. HIGH-VOLTAGE POWER SUPPLY, 6-12KV, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Part of pi filter (with C1 + C2)
R2	Current-limiting resistor
R3-R6	Voltage divider
T1	Stepup transformer
Voltmeter	Output voltage indicator
C1, C2	Part of pi filter (with R1)

4.3.2 Principles of Operation

4.3.2.1 Typical Control Network

Each high-voltage unit contains from four to six control networks. Each control network is physically connected to a pair of deflection plates. Figure 4–5 is the schematic diagram of a typical control network. Table 4–5 lists the associated detail parts and their functions. Analog-deflecting voltage is applied across resistors R1 and R2. R1 is a dual section (A and B) potentiometer with a single control shaft. Rotation of the shaft in one direction causes the variable arms to move toward R2, reducing the amplitude of the voltage applied to the deflection plates. Rotation of the shaft in the other direction causes the variable arms to move toward the input terminals and increases the amplitude of analog voltage applied to the deflection plates. R1 permits the adjust-

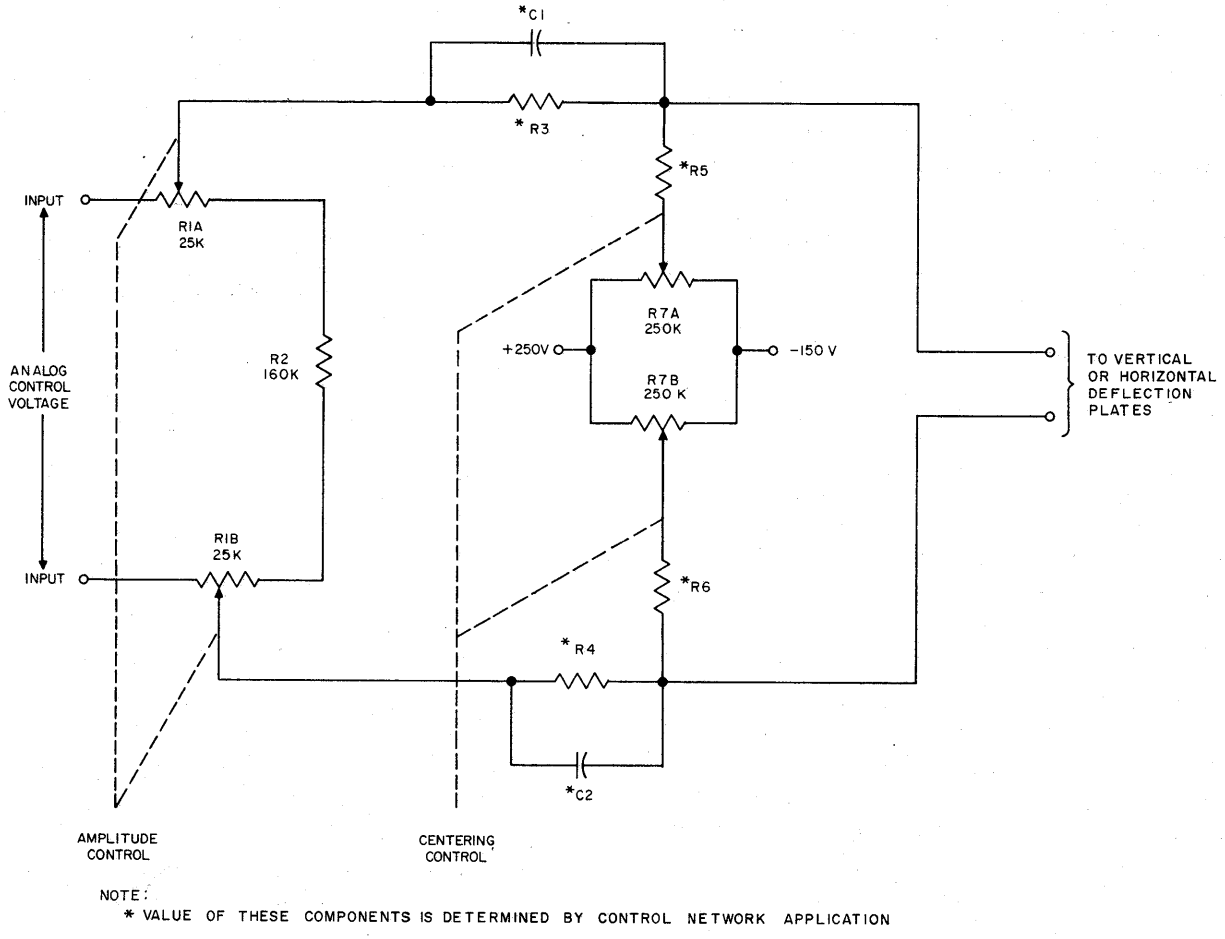


Figure 4–5. High-Voltage Unit, Typical Centering and Amplitude Control Network, Schematic Diagram

TABLE 4–5. HIGH-VOLTAGE UNIT, CENTERING AND AMPLITUDE CONTROL NETWORK, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of frequency compensation network (with R3)
C2	Part of frequency compensation network (with R4)
R1	Output voltage amplitude control
R2	Limits range of R1
R3	Part of frequency compensation network (with C1)
R4	Part of frequency compensation network (with C2)
R5, R6	Isolating resistors
R7	Centering control

ment of analog control voltage applied to the deflection plates in the range of 75 to 100 percent of the input voltage.

Capacitors C1 and C2 speed up the application of input voltage level transitions to the deflection plates, compensating for the high-frequency losses introduced by the network.

Resistor R7 is a dual section (A and B) potentiometer with a single control shaft. Sections A and B of this potentiometer are connected in parallel between +250V and —150V in such a manner that the variable arms move in opposite directions for a given rotation of the control shaft. The adjustment of this potentiometer ensures display operation around the physical center of the display tube face. The control provides a pair of residual voltages of desired magnitude and polarity to compensate for all centering effects of component value variations within tolerance and variations in physical alignments of SD CRT elements. Resistors R5 and R6 isolate the centering controls from other portions of the network.

4.3.2.2 SD High-Voltage Unit

The SD high-voltage unit is shown schematically in figure 4–6. Table 4–6 lists the associated detail parts and their functions. This high-voltage unit consists of six circuits which provide SD control voltages to the elements listed as follows:

a. SD CRT
   1. Heater cathode voltage
   2. Anode 2 voltage
   3. Matrix
   4. Control grid bias and intensity gate
   5. Focus voltage and defocus gate to anode 1

b. Light gun or area discriminator
   Plate voltages for seven plates of the photoelectric tube in the light gun or area discriminator

c. Convergence current regulator
   A —300V correction voltage

TABLE 4–6. SD HIGH-VOLTAGE UNIT, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Part of voltage divider (with R3)
R2	Matrix current-limiting resistor
R3	Part of voltage divider (with R1)
R4	Load resistor for input intensity gate
R5	Control grid resistor for SD CRT
R6, R7	Voltage divider
R8	Control grid bias adjust for SD CRT
R9	Current-limiting resistor for V2 and V3
R10	Protective resistor preventing plates of V2 and V3 from falling to —3,300V should —300V line fail
R11	Sets lower limit of focus voltage adjustment
R12	Level-setting potentiometer for SD CRT focus anode
R13	Load resistor for input defocus gate
R14, R15, R16	Voltage divider
R17-R24	Voltage divider for light gun and area discriminator elements
C1	Intensity gate coupling capacitor
C2	Intensity control bypass capacitor
C3	Focus control and R11 bypass capacitor
C4	Defocus gate coupling capacitor
C5	Bypass capacitor for R16
T1	Filament transformer for V1, V4, and SD CRT

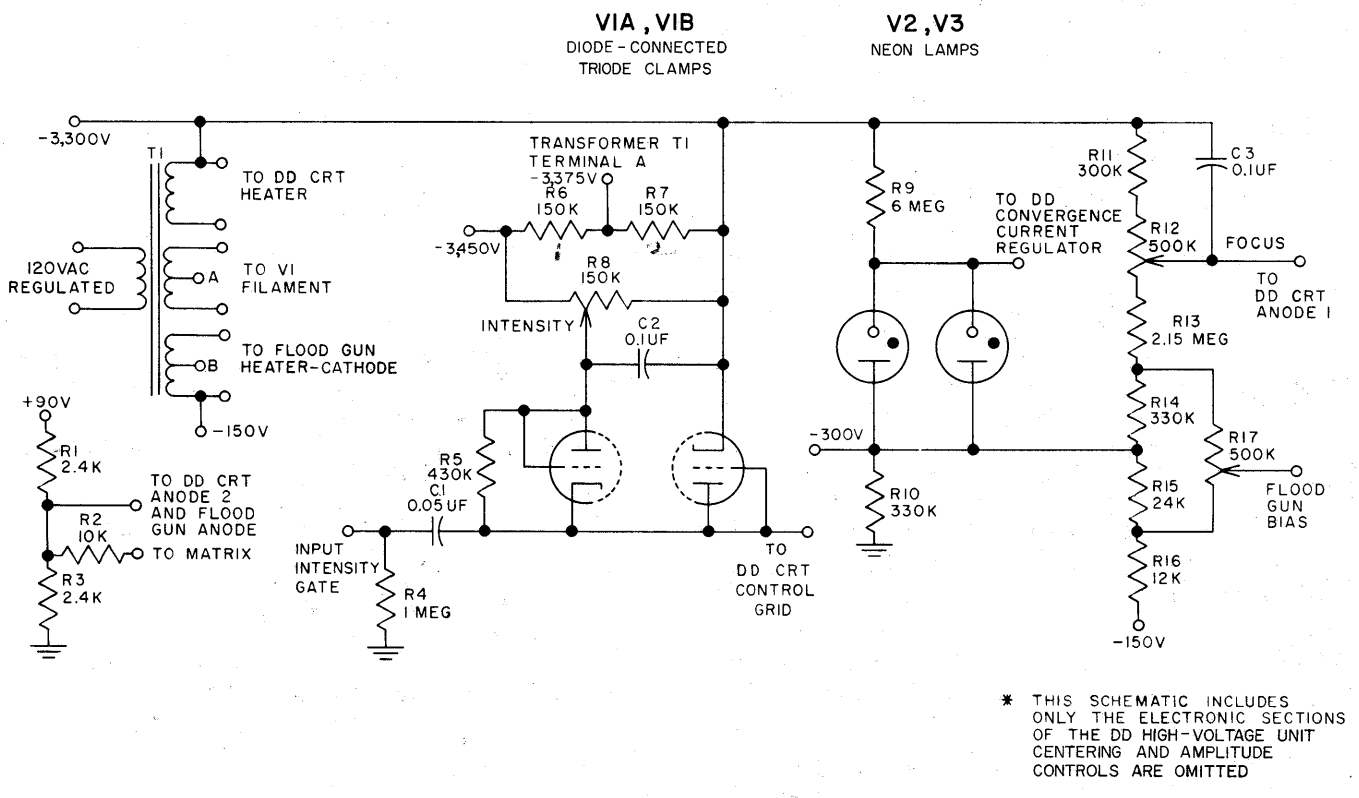
As seen in figure 4–6, foldout, transformer T1 consists of a primary and three secondary windings. Two of the secondary windings provide filament power for clamping diodes V1 and V4. Each winding is center-tapped for the application of suitable reference voltages to prevent filament-to-cathode breakdown. The third secondary winding, referenced at —3,300V, supplies filament voltage for the SD CRT. The accelerating anode and matrix voltage is provided for by the voltage divider consisting of R1 and R3.

The cutoff bias for the SD CRT is provided for by the intensity control circuit. The voltage set by intensity potentiometer R8 is fed through R5 to the control grid of the SD CRT. The bias is variable (0-150V) with respect to the cathode. Capacitor C1 couples the input intensity gate to the control grid. Clamps V1A and V1B limit the excursion of the intensity gate between —3,300V and the bias voltage set by R8. The voltage divider consisting of R6 and R7 provides a reference voltage level of —3,425V for the filament winding of V1.

The focus control circuit provides the voltage necessary to produce a sharply focused electron beam for vector generation. The potential at the moving arm of R12 is adjustable between —2,700V and —2,300V. Proper adjustment of R12 produces a minimum diameter dot image on the face of the SD CRT and ensures unimpeded passage through the matrix. This potential is applied through a voltage divider, consisting of resistors R14, R15, and R16, to the focus anode of the SD CRT. The defocus gate (applied each time a character is selected) is developed across input load resistor R13. Capacitor C4 couples this gate to the focus anode, superimposing the positive focus gate on the fixed bias determined by R12. Clamping diodes V4A and V4B prevent the focus anode from becoming more negative than the fixed focus level when the defocus gate is removed. Resistors R15 and R16 form a voltage divider which provides the required reference level for the V4 filament winding. Resistors R17 through R24 form a bleeder network which provides the required multiplier plate potentials for the light gun and area discriminator. The correction voltage for the convergence current regulator is provided by voltage regulator V2 and V3.

4.3.2.3 DD High-Voltage Unit

The DD high-voltage unit is shown schematically in figure 4–7. Table 4–7 lists the associated detail parts and their functions. The DD high-voltage unit consists of five circuits which provide DD control voltages to the



* THIS SCHEMATIC INCLUDES ONLY THE ELECTRONIC SECTIONS OF THE DD HIGH-VOLTAGE UNIT CENTERING AND AMPLITUDE CONTROLS ARE OMITTED

Figure 4–7. DD High-Voltage Unit, Partial Schematic Diagram

DD CRT and to the convergence current regulator as follows:

a. DD CRT
   1. Electron gun voltages
   2. Flood gun voltages
   3. Matrix voltage

b. Convergence current regulator
   Compensation voltage for accelerating potential changes

As seen in figure 4–7, transformer T1 consists of a primary and three secondary windings. The functions of the three secondary windings are as follows. One winding provides filament voltage for clamping diode V1, the second winding, referenced at —150V, supplies heater voltage for the DD CRT flood gun. The third winding, referenced at —3,300V, provides the heater voltage for the DD CRT. The V1 filament winding in the T1 secondary is center-tapped to prevent filament-to-cathode breakdown in V1A and V1B.

The voltage divider, consisting of resistors R1 and R3, provides +45V for the flood gun anode, the accelerating anode (anode 2), and the matrix of the DD CRT.

The voltage applied to the control grid of the DD CRT is adjusted to bias the tube past cutoff. This voltage is determined by the setting of potentiometer R8 and is applied to the DD CRT control grid through R5. The bias is variable (0 to —150V) with respect to the cathode. Capacitor C1 couples the intensity input gate to the control grid of the DD CRT. Diode-connected triodes V1A and V1B clamp the intensity gate between —3,300V and the bias setting of R8. The voltage divider, consisting of R6 and R7, provides a reference voltage level of —3,375V for the filament winding of V1.

The voltage applied to anode 1 of the DD CRT determines the cross-sectional area of the electron beam. The magnitude of this voltage is determined by the setting of potentiometer R12 (between —2,700 and —2,300V). This potentiometer is adjusted to make the cross-sectional area of the electron beam greater than any character on the matrix. Potentiometer R17, adjustable between —100V and —590V, determines the number of electrons permitted to reach the storage mesh element in the DD CRT.

4.3.2.4 Auxiliary High-Voltage Unit

The auxiliary high-voltage unit is used with the DD CRT's in the auxiliary display consoles. Its function and operation in the auxiliary consoles is identical with that of the DD high-voltage unit in the DD indicator sections. For a detailed explanation of the auxiliary high-voltage unit, refer to paragraph 4.3.2.3.

4.3.2.5 Projector High-Voltage Unit

The projector console high-voltage unit is similar in function and operation to the SD high-voltage unit in the SD console. The electronic sections in either of these high-voltage units are identical. The SD high-voltage unit is associated with the 19-inch SD CRT, and the projector high-voltage unit is associated with the 7-inch SD CRT. Thus, the difference is in the value of several of the detail parts in the amplitude and centering control networks associated with each high-voltage unit. For the projector console high-voltage unit schematic diagram, and detailed operation analysis, refer to figure 4–7, and paragraph 4.3.2.3, respectively.

TABLE 4–7. DD HIGH-VOLTAGE UNIT, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Intensity gate coupling capacitor
C2	Intenisty control bypass capacitor
C3	Focus control and R11 bypass capacitor
R1	Part of voltage divider (with R3)
R2	Matrix current-limiting resistor
R3	Part of voltage divider (with R1)
R4	Load resistor for input intensity gate
R5	Grid return for DD CRT
R6, R7	Voltage divider
R8	Intensity control for DD CRT
R9	Current-limiting resistors for V2 and V3
R10	Protective resistor preventing plates of V2 and V3 from rising to —3,300V if —300V line fails
R11	Determines lower limit of focus adjustment
R12	Focus control for DD CRT
R13-R16	Voltage divider
R17	Flood gun bias control
T1	Filament transformer for V1, flood gun, and DD CRT

4.4 LOW-VOLTAGE POWER SUPPLY

4.4.1 Definition and Description

The display low-voltage power supply is a nonlogic circuit that supplies three d-c voltages for the relay control circuits in the projector console.

4.4.2 Principles of Operation

Figure 4–8 is the schematic diagram for the low-voltage power supply. Table 4–8 lists the associated detail parts and their functions. The circuit consists of a power transformer with two secondary windings and associated rectifiers and filter components to produce the necessary d-c low-voltage outputs.

Secondary winding A provides 32Vac which is rectified by a bridge network consisting of CR1 to CR4. The output from the bridge rectifier is filtered by L1 and C1. The resultant 24Vdc output is used to actuate the many varied and independent solenoids and relays in the projection control circuit.

TABLE 4–8. LOW-VOLTAGE POWER SUPPLY, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of filter network (with L1)
CR1-CR12	Selenium rectifiers in bridge networks
F1	Line fuse
L1	Filter choke, part of filter network (with C1)
T1	Power transformer

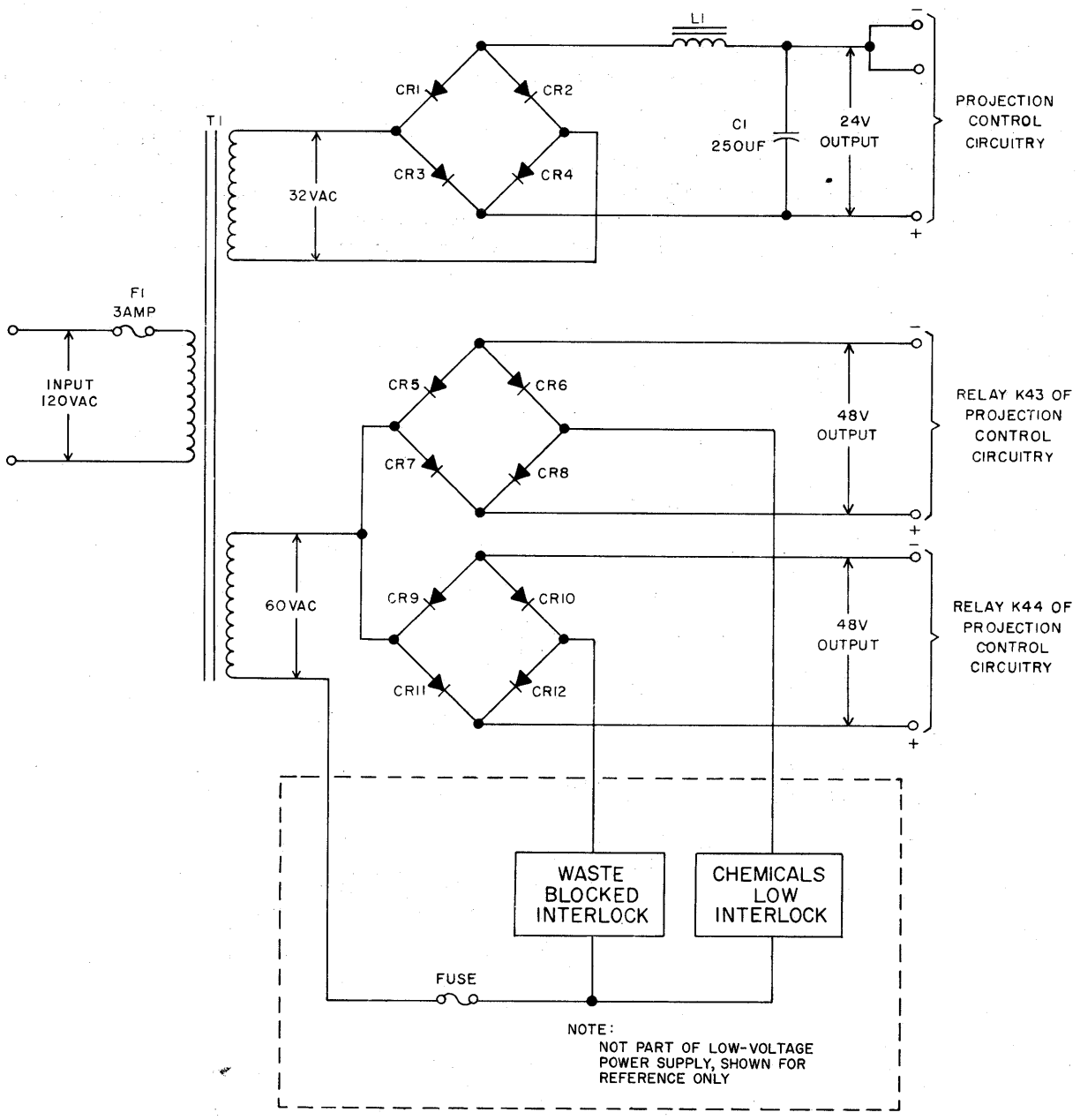


Figure 4–8. Low-Voltage Power Supply, Schematic Diagram

Secondary winding B supplies 60Vac to two bridge rectifiers, the individual outputs of which are 48Vdc. One output is employed to energize an alarm relay and interlock switch indicating insufficient chemical levels. The other functions in the same manner to indicate a blocked waste drain.

4.5 MEMORY ALARM, —150V

4.5.1 Definition and Description

The —150V memory alarm is a nonlogic circuit which actuates a visual and audible alarm at the duplex maintenance console to alert personnel that a condition is present which may adversely affect the operation of the computer.

In the 256^2 memory array, the read and write current pulses are supplied by the core current driver matrices. In order to ensure optimum operation, the read and write current pulses must be kept within close tolerance in both timing and amplitude. The one factor which may simultaneously affect both of these current pulses is the regulation of the supply voltages to the control circuits. In order to ensure that the voltage regulation of the —150V supply is always within ±1.5 percent, the —150V memory alarm is utilized in the memory unit. This circuit actuates a visual and audible alarm wherever the —150 supply voltage varies more than ±1.5 percent.

4.5.2 Principles of Operation

The schematic diagram of the —150V memory alarm circuit is shown in figure 4–9. As noted in this figure, meter relay K1, which is the main component of the circuit, contains high and low coils in addition to a moving coil. The moving coil of this relay, which actuates the moving pointer in the same manner as occurs in a standard galvanometer, is connected to the —150V test source through R1, R2, and normally closed contacts 5 and 6 of relay K2. The current flow through the moving coil is adjusted by R1 so that when the test voltage is exactly —150V the moving pointer will be centered on the meter scale midway between the LO and HI contact points. However, if the —150V test voltage varies ±1.5 percent from the nominal value, the current through the moving coil will change sufficiently to close the appropriate set of contacts. When either set of contacts close, the associated hold coil circuit is energized from a —48V source through the pick coil of relay K2. The meter relay hold coils are proportioned so that their fields will attract the moving pointer directly in order

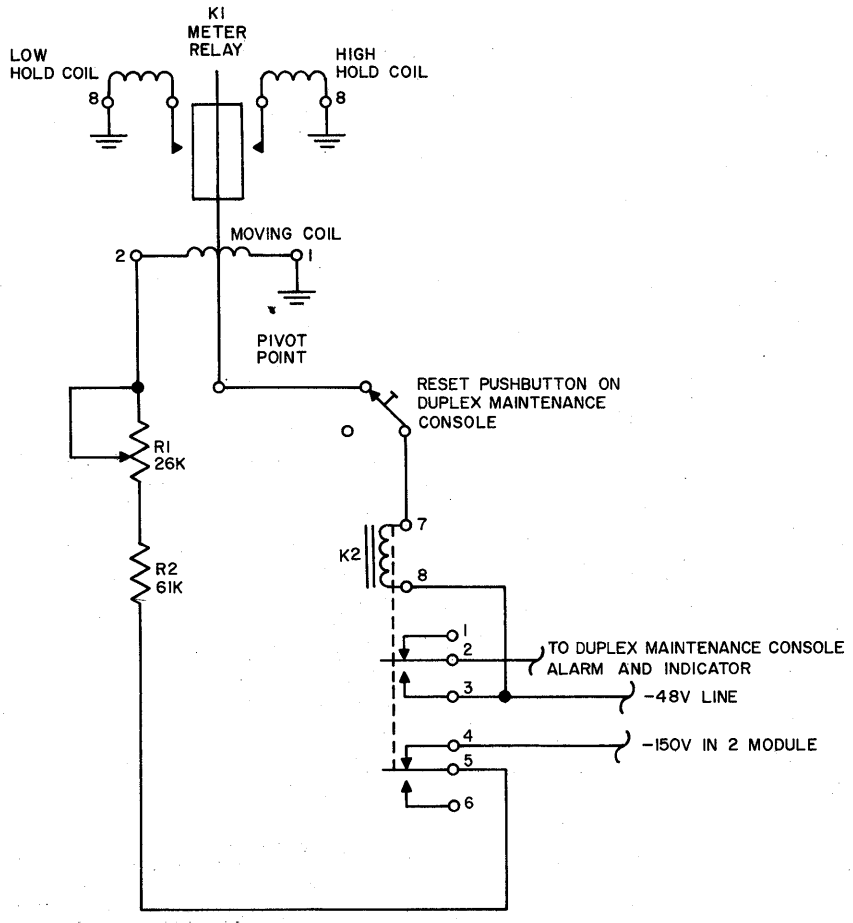


Figure 4–9. Memory Alarm, —150V, Schematic Diagram

to keep the contact closed once it has been made. Since relay K2 is picked when either the HI or LO contacts are closed, contacts 4 and 5 will open to disconnect the —150V test source, and contacts 2 and 3 will close to energize a buzzer and a filament-type lamp in the duplex maintenance console. Thus, when the regulation of the test voltage varies more than 1.5 percent, both an audible and a visual alarm will be generated. These alarm circuits will remain energized until the normally closed reset pushbutton on the duplex maintenance console is depressed, momentarily opening the hold circuit. Relay K2 will be dropped so that the alarms will be de-energized, and the —150V test voltage will again be supplied to the meter relay moving coil. If the test voltage has changed (either automatically after a transient condition or due to manual intervention) and is now within tolerance, the circuit will remain reset until another voltage variation is detected.

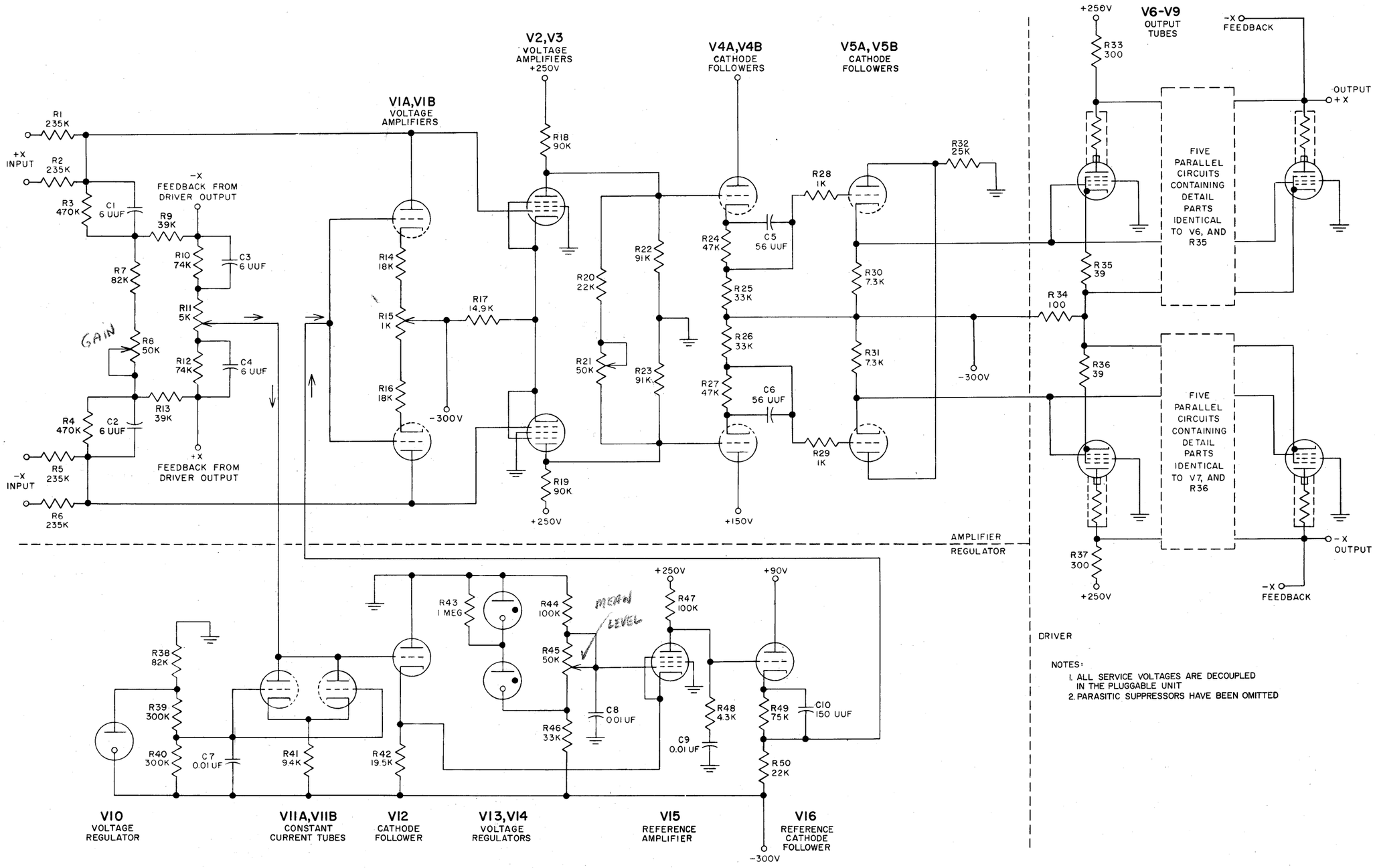


Figure 3-6. Analog Line Driver, Schematic Diagram

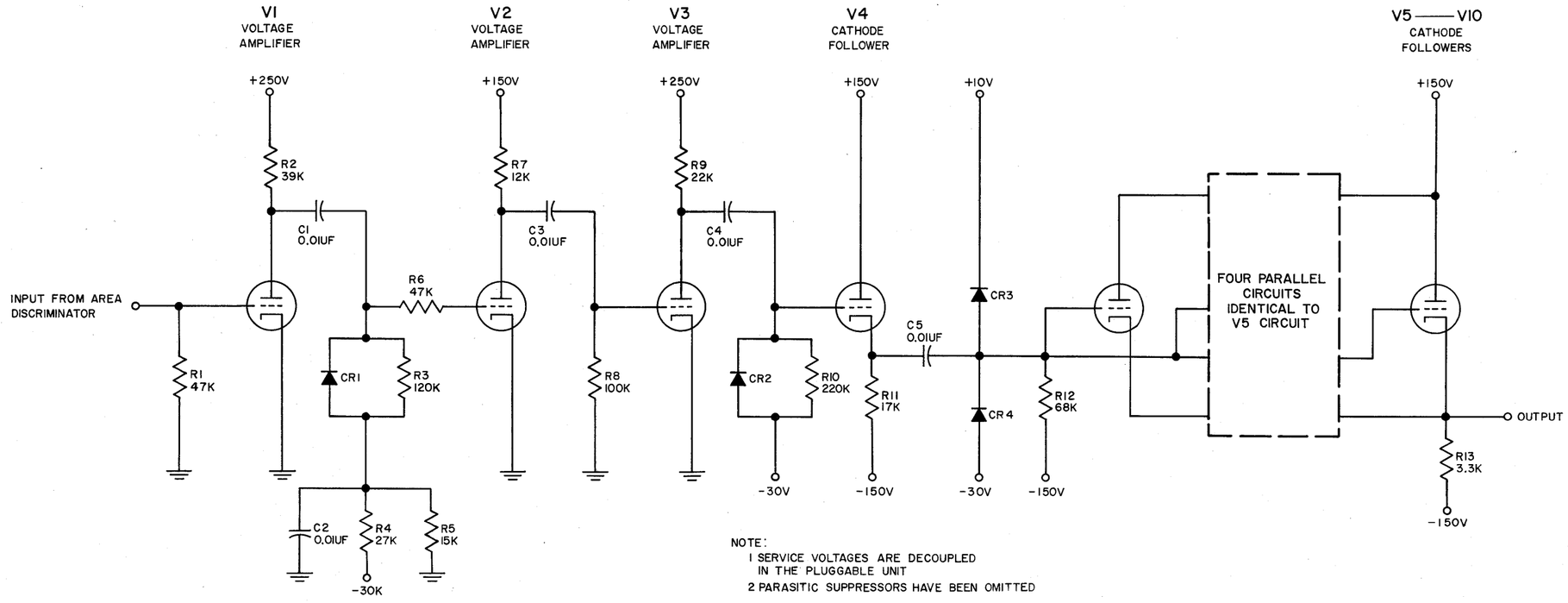
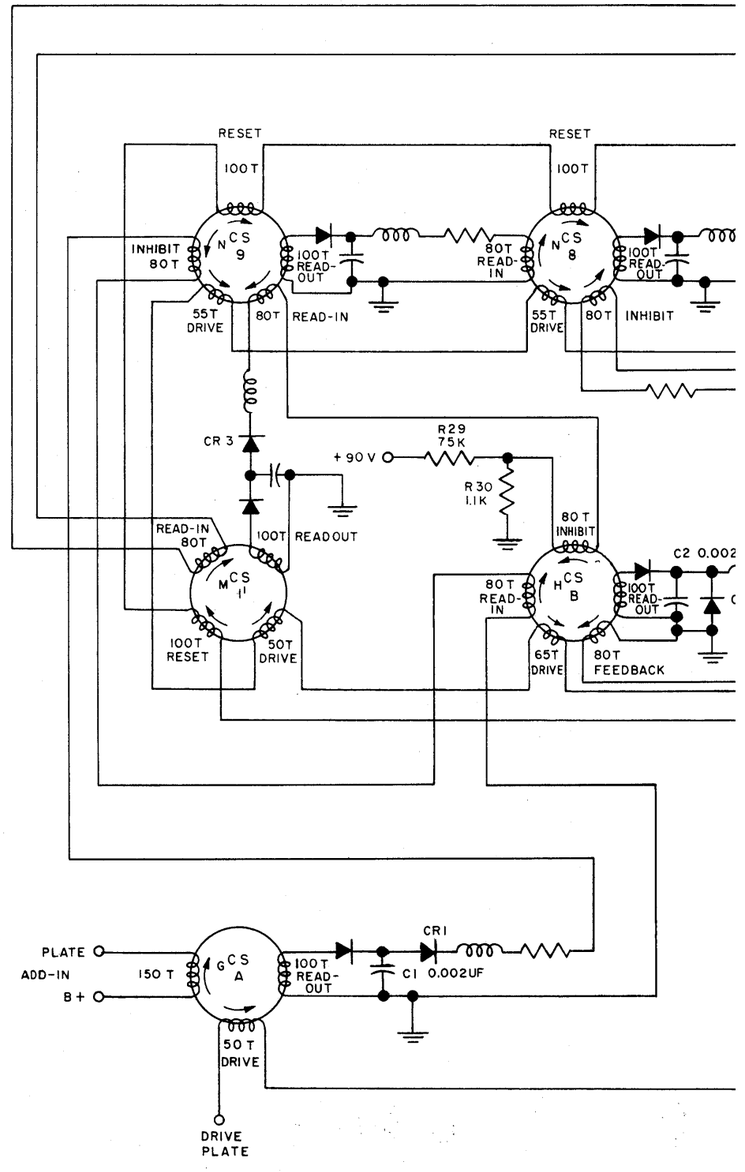


Figure 3–10. Area Discriminator Amplifier, Model A, Schematic Diagram


RESET
100T
RESET
100T
INHIBIT
80T
N CS 9
100T READ-OUT
80T READ-IN
N CS 8
100T READ-OUT
55T DRIVE
80T
READ-IN
55T DRIVE
80T
INHIBIT
CR 3
+90V
R29 75K
R30 1.1K
80T INHIBIT
READ-IN 80T
100T READOUT
C2 0.002
M CS 11
H CS B
80T READ-IN
100T READ-OUT
100T RESET
50T DRIVE
65T DRIVE
80T FEEDBACK
CR1
PLATE
ADD-IN
B+
150T
G CS A
100T READ-OUT
C1 0.002UF
50T DRIVE
DRIVE PLATE

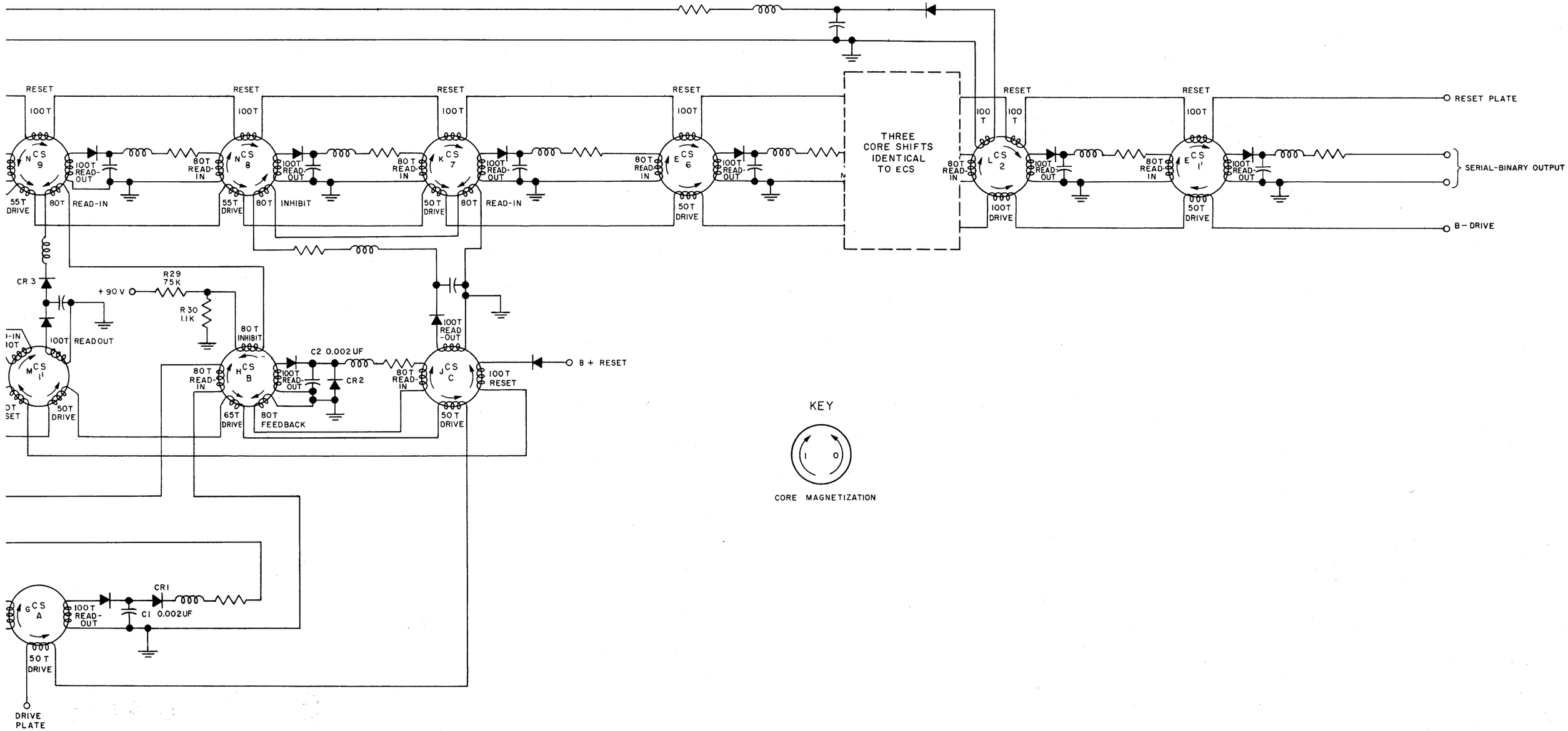
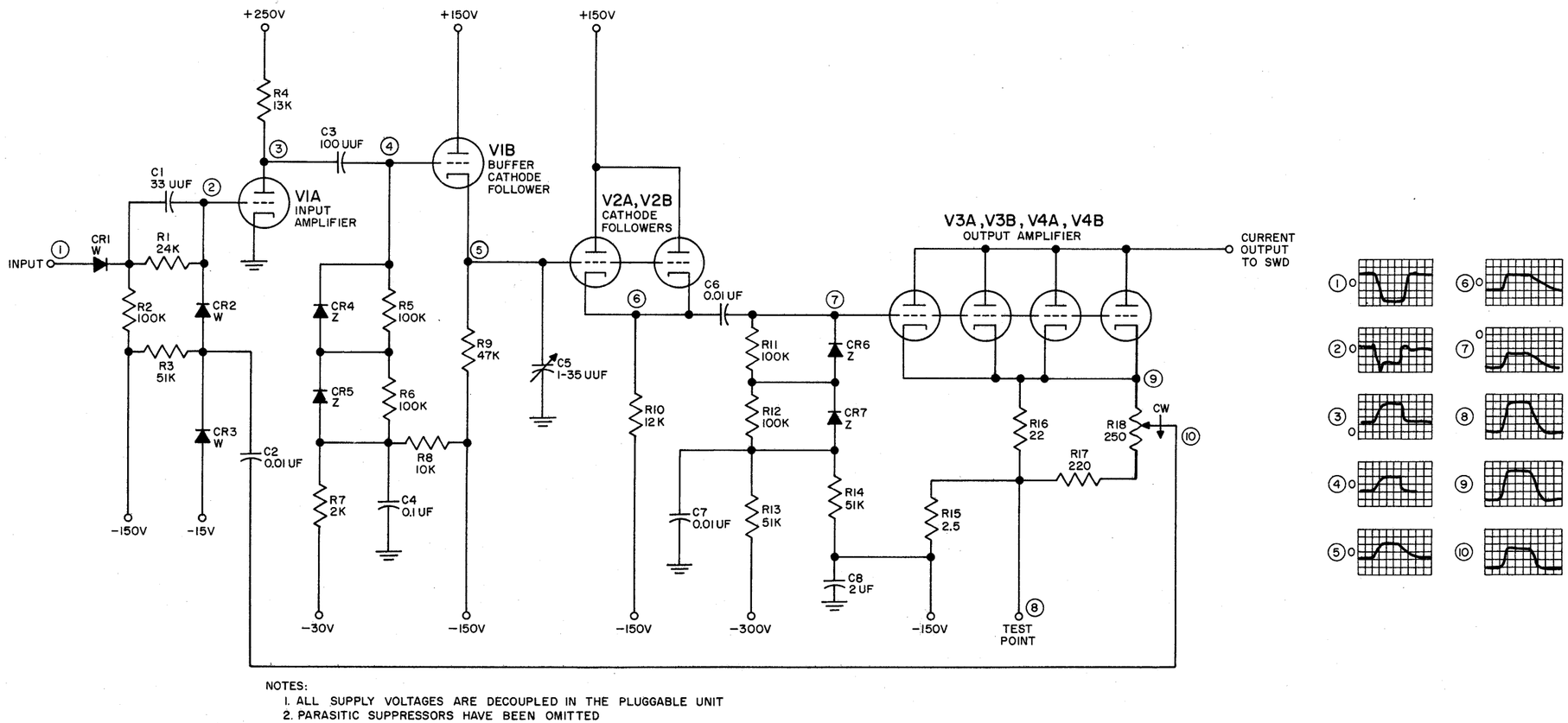
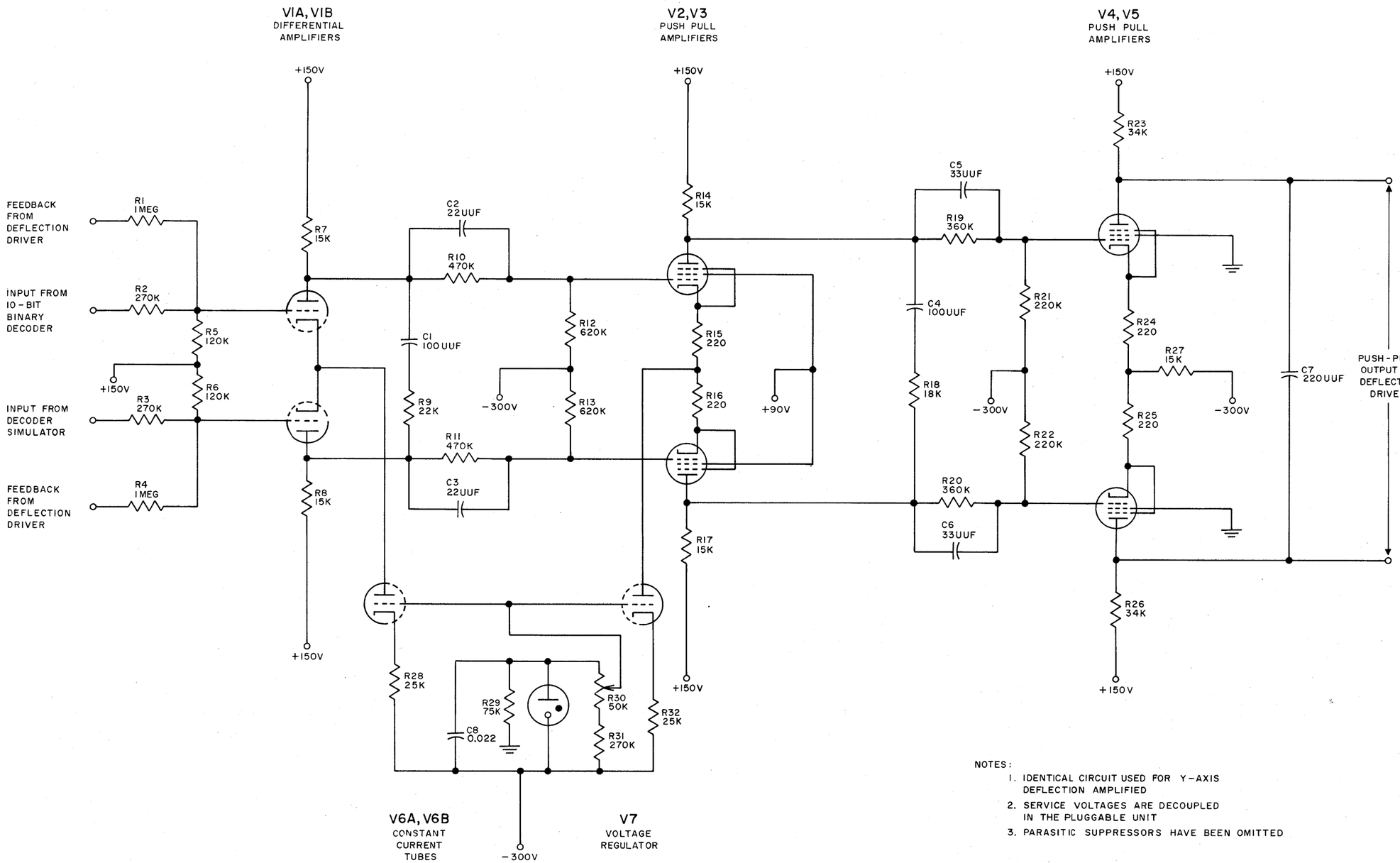


Figure 3–31. Complement Core Counter, Schematic Diagram



NOTES:
1. ALL SUPPLY VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

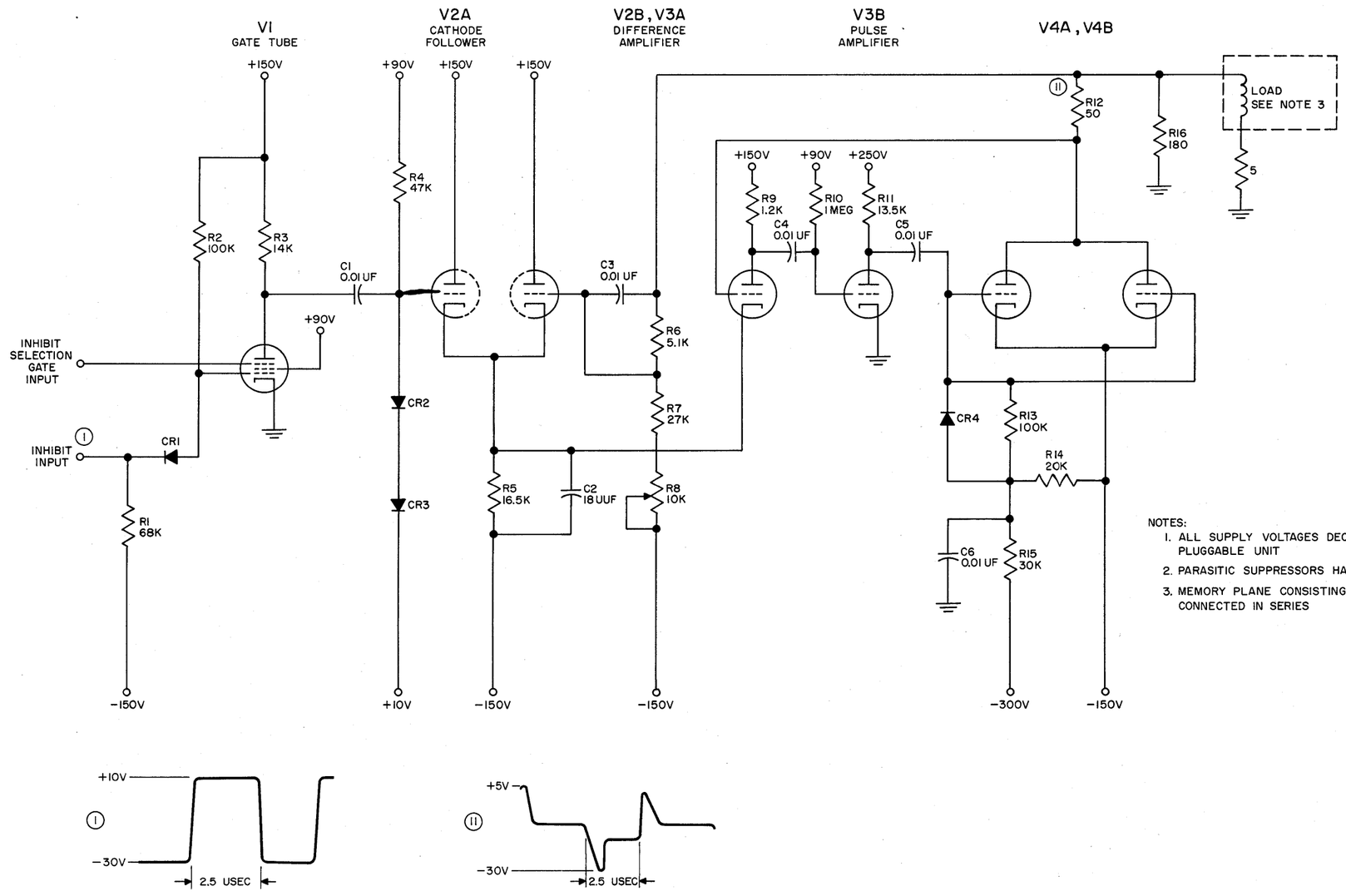
Figure 3-56. Current Regulator, Model A, Schematic Diagram



NOTES:

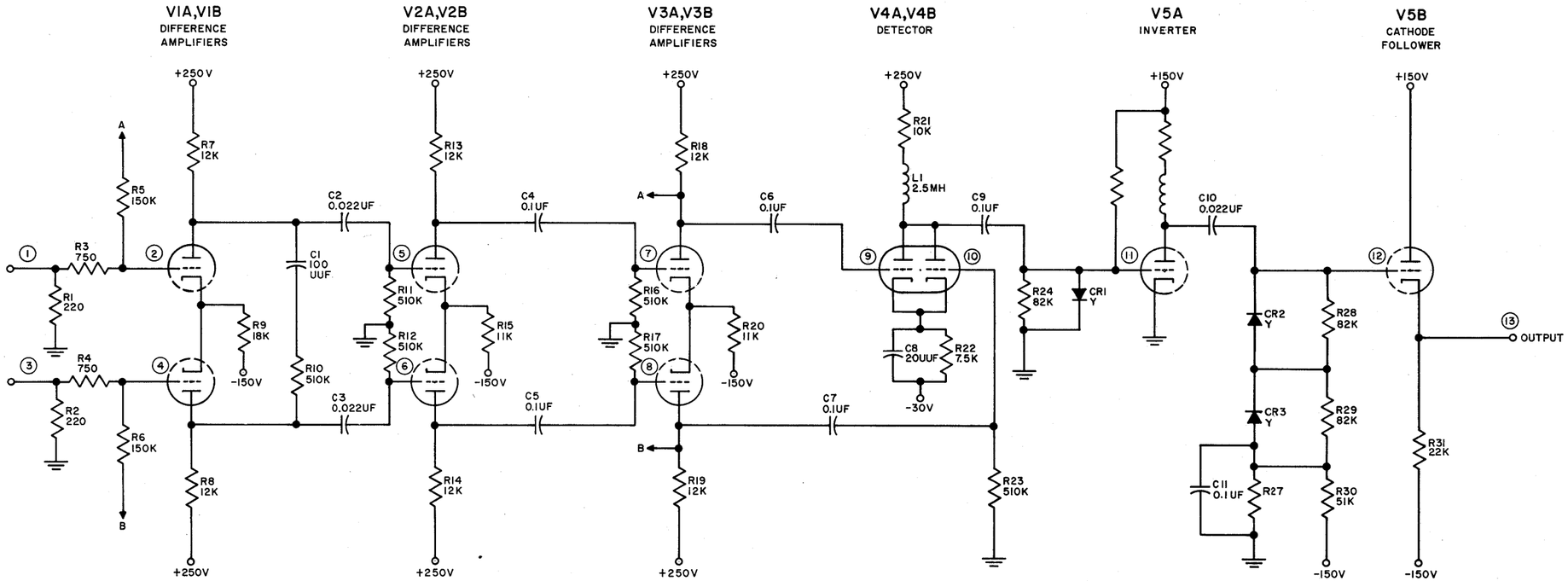
1. IDENTICAL CIRCUIT USED FOR Y-AXIS DEFLECTION AMPLIFIED
2. SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
3. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

Figure 3-64. Deflection Amplifier, X-Axis Portion, Display System, Schematic Diagram



NOTES:
1. ALL SUPPLY VOLTAGES DECOUPLED IN PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED
3. MEMORY PLANE CONSISTING OF 64 X 64 CORES CONNECTED IN SERIES

Figure 3-73. Digit Plane Driver, Model A, Schematic Diagram



NOTES:
1. ALL SUPPLY VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

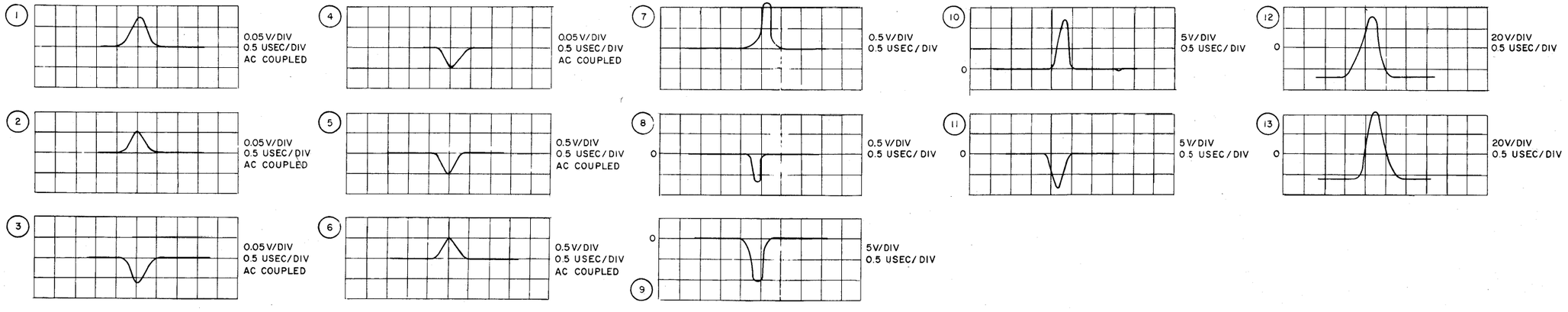
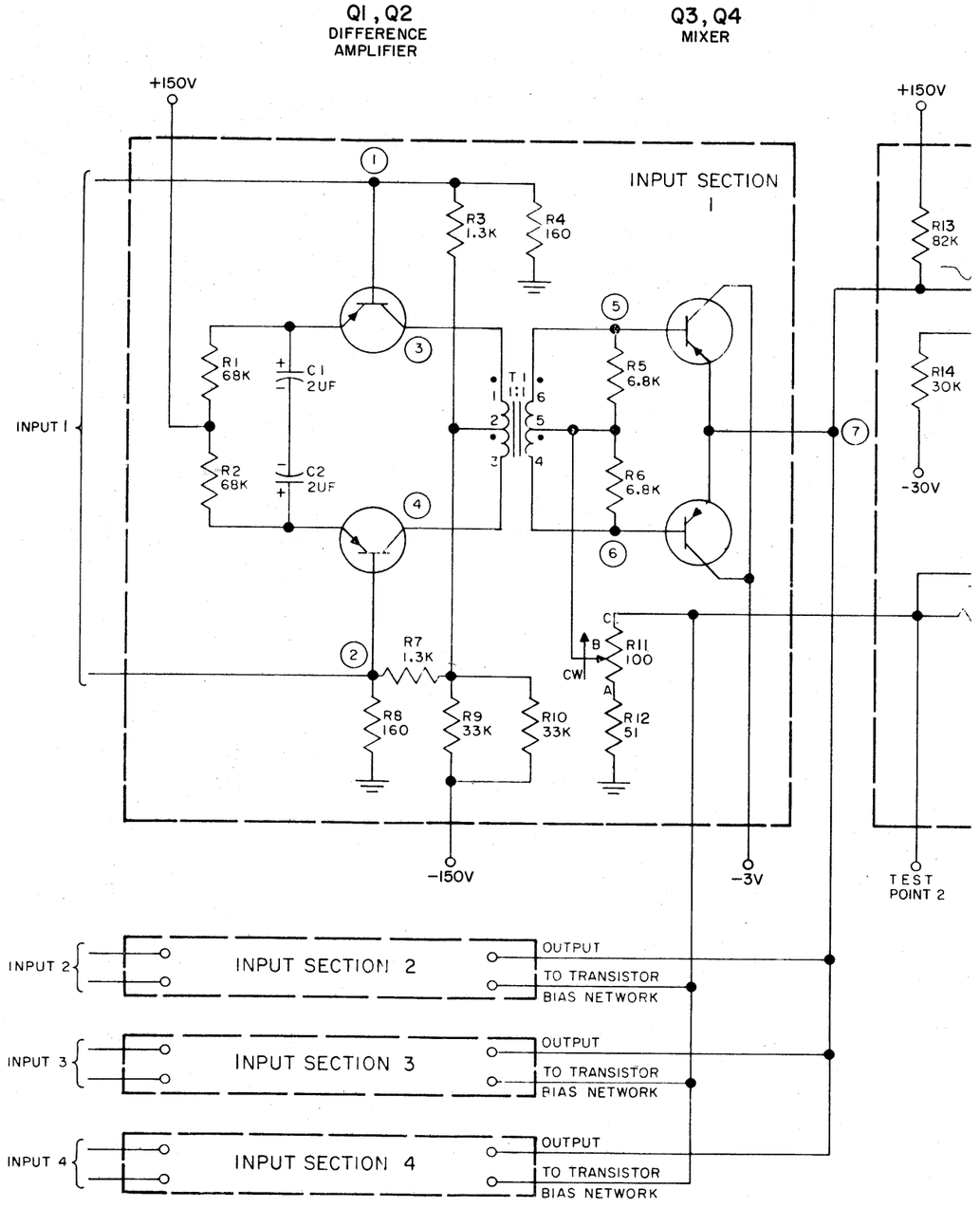
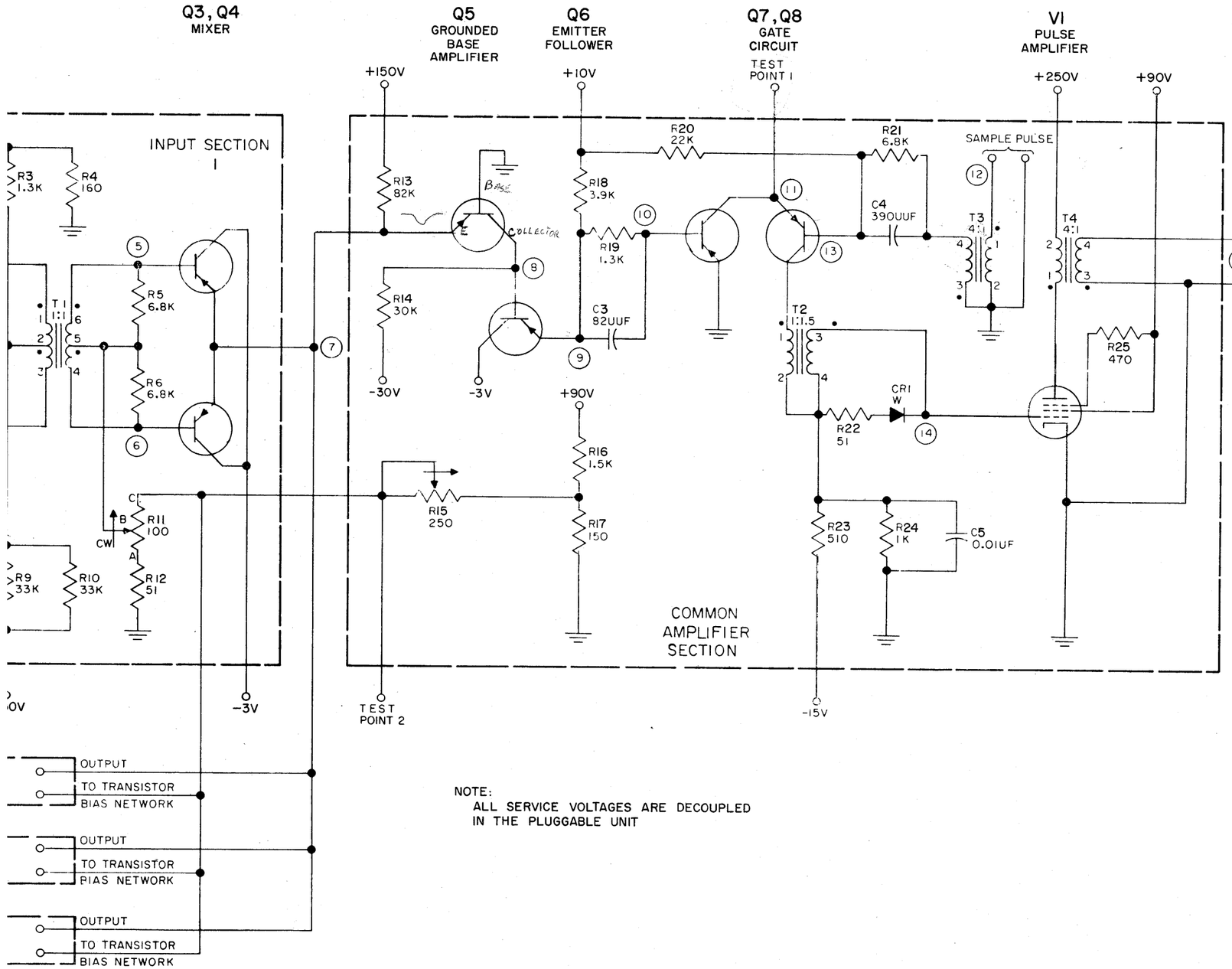
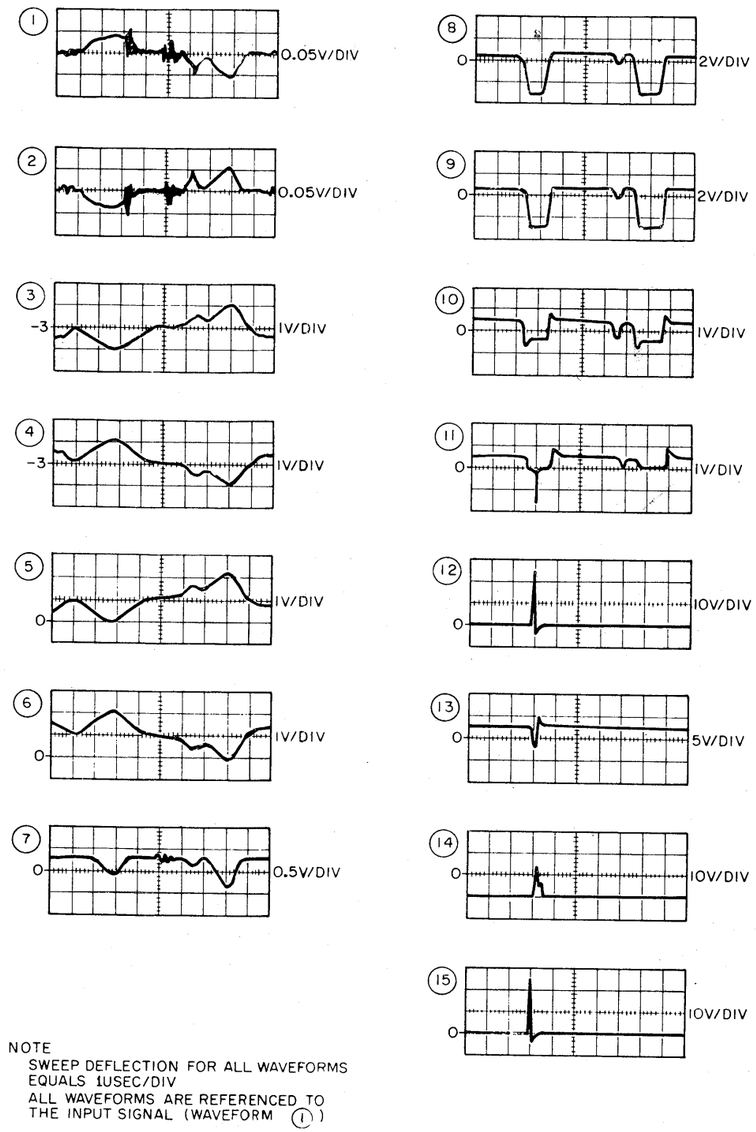


Figure 3-185. Sense Amplifier, Model B, Schematic Diagram


Q1, Q2
DIFFERENCE
AMPLIFIER
Q3, Q4
MIXER
+150V
INPUT SECTION
1
INPUT 1
R1
68K
R2
68K
C1
2UF
C2
2UF
R3
1.3K
R4
160
T1
1:1
R5
6.8K
R6
6.8K
R7
1.3K
R8
160
R9
33K
R10
33K
R11
100
R12
51
CCW
CW
R13
82K
R14
30K
-30V
-150V
-3V
TEST
POINT 2
INPUT 2
INPUT SECTION 2
OUTPUT
TO TRANSISTOR
BIAS NETWORK
INPUT 3
INPUT SECTION 3
OUTPUT
TO TRANSISTOR
BIAS NETWORK
INPUT 4
INPUT SECTION 4
OUTPUT
TO TRANSISTOR
BIAS NETWORK

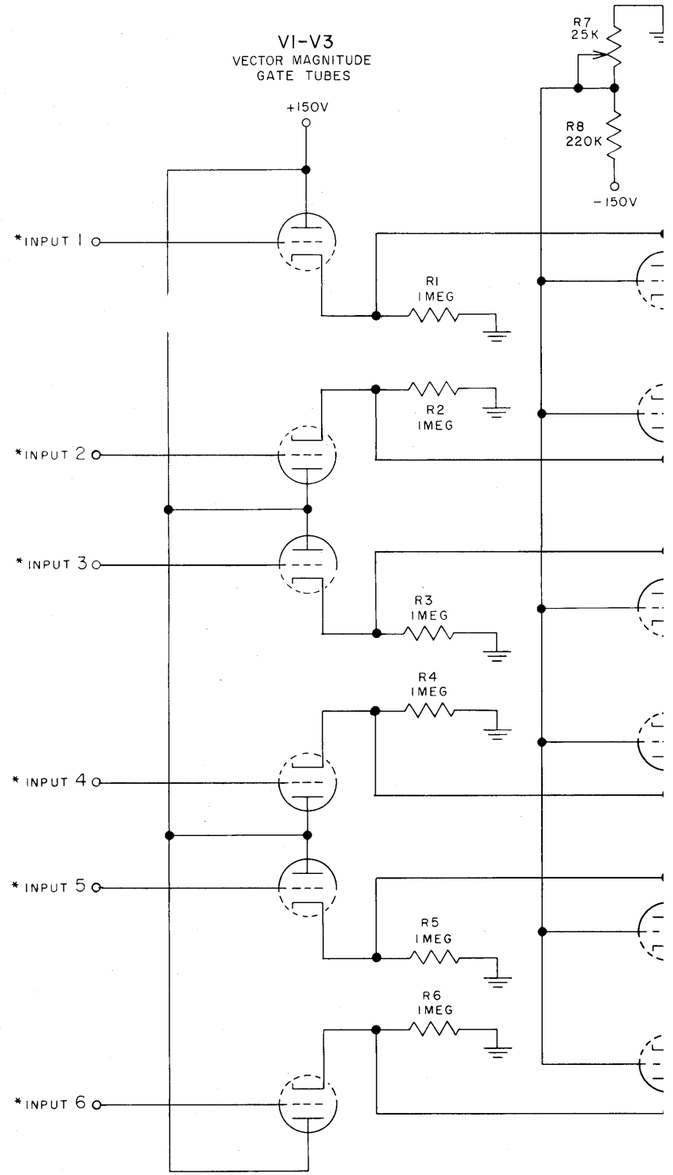


NOTE:
ALL SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT



NOTE
SWEEP DEFLECTION FOR ALL WAVEFORMS EQUALS 1USEC/DIV
ALL WAVEFORMS ARE REFERENCED TO THE INPUT SIGNAL (WAVEFORM (1))

Figure 3–188. Sense Amplifier, Model C, Schematic Diagram


V1-V3
VECTOR MAGNITUDE
GATE TUBES
+150V
R7
25K
R8
220K
-150V
*INPUT 1
R1
1MEG
R2
1MEG
*INPUT 2
*INPUT 3
R3
1MEG
R4
1MEG
*INPUT 4
*INPUT 5
R5
1MEG
R6
1MEG
*INPUT 6

V1-V3
VECTOR MAGNITUDE
GATE TUBES

V4-V6
CURRENT
SOURCE TUBES

V7-V12
VECTOR-SIGN
GATE TUBES

+150V
-150V
+250V
R7 25K
R8 220K
FROM SWEEP GENERATOR
R1 IMEG
R2 IMEG
R3 IMEG
R4 IMEG
R5 IMEG
R6 IMEG
R9 5K
R10 5K
R11 5K
R12 5K
R13 5K
R14 5K
R15 15K
R16 15K
R17 15K
R18 15K
R19 15K
R20 15K
R21 56K
R22 56K
CR1
CR2
CR3
CR4
* INPUT A VECTOR SIGN
* INPUT B VECTOR SIGN
R23 8.2K
R24 8.2K
R25 16.4K
R26 8.2K
R27 16.4K
R28 8.2K
R29 16.4K
R30 8.2K
R31 16.4K
R32 8.2K
R33 50K
R34 8.2K
R35 8.2K
R36 16.4K
R37 8.2K
R38 16.4K
R39 8.2K
R40 16.4K
R41 8.2K
R42 16.4K
R43 8.2K
R44 50K
$\dot{X}$ OUTPUT

NOTES:
1. ALL SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT.
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED.

Figure 3–217. Vector Generator, X-Axis Decoder Section, Schematic Diagram

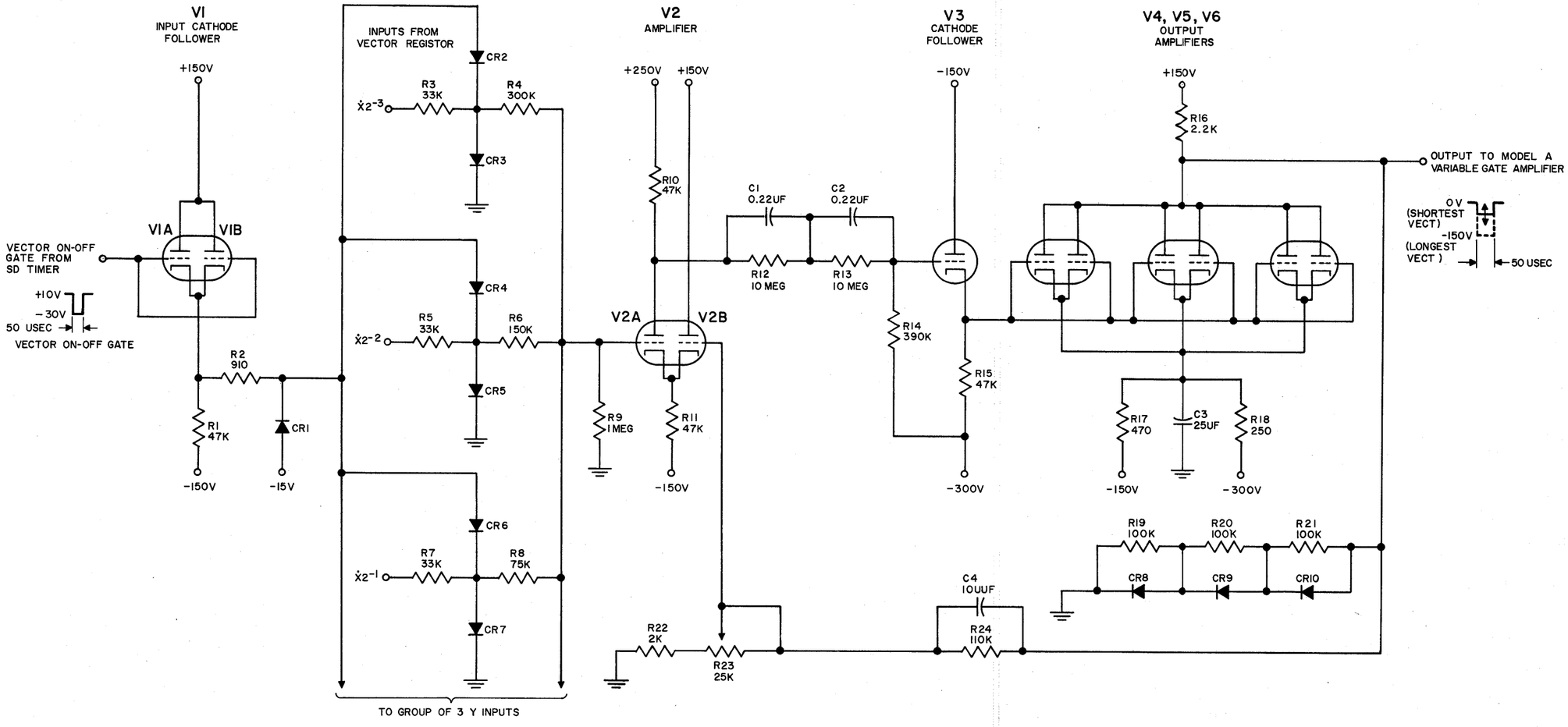
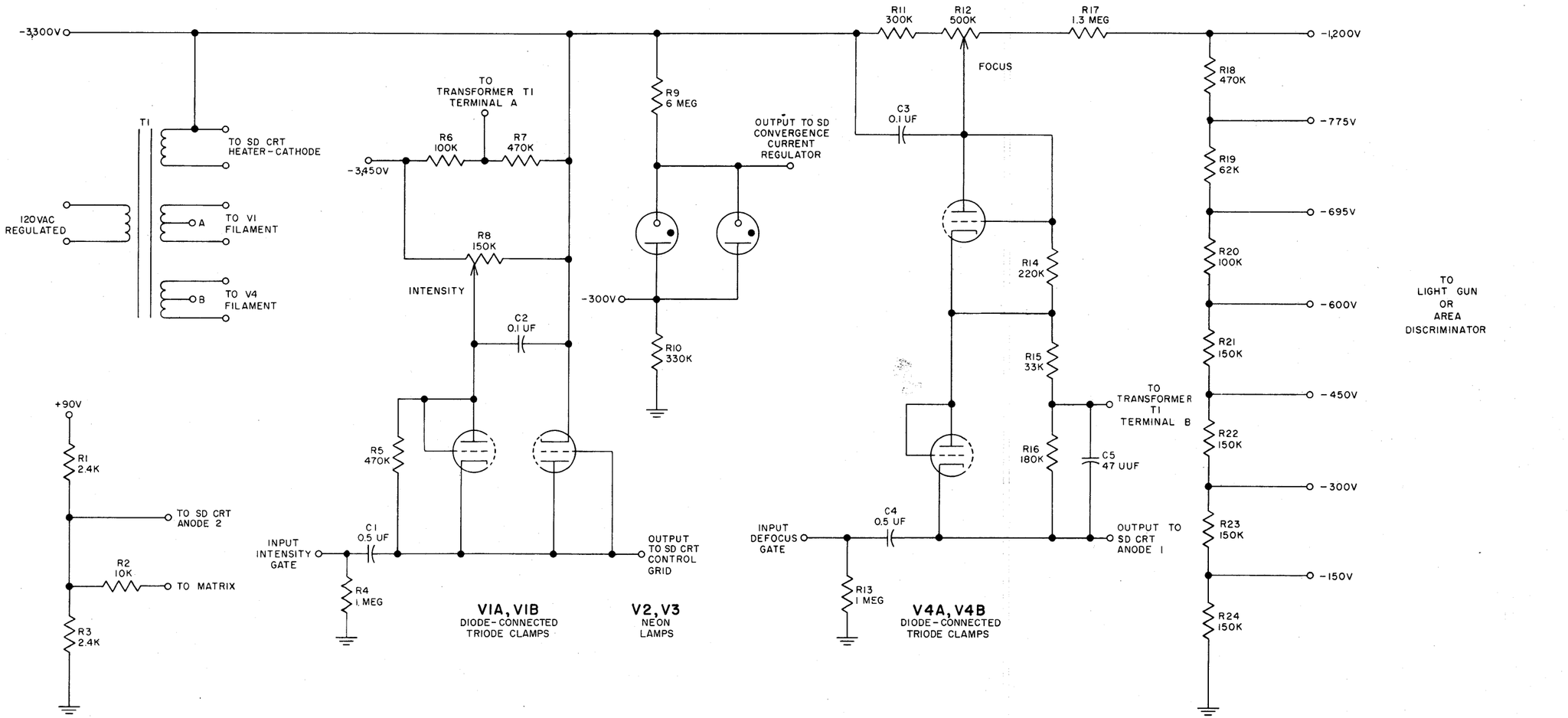


Figure 3–219. Vector Intensity Generator, Schematic Diagram



* THIS SCHEMATIC INCLUDES ONLY THE ELECTRONIC SECTION OF THE SD HIGH-VOLTAGE UNIT. CENTERING AND AMPLITUDE CONTROLS ARE OMITTED.

Figure 4-6. SD High-Voltage Unit, Partial Schematic Diaram